

# **Exhibit 1**

**UNITED STATES DISTRICT COURT  
FOR THE EASTERN DISTRICT OF TEXAS  
MARSHALL DIVISION**

TIVO INC.,

Plaintiff and Counter-  
Defendant,

vs.

SAMSUNG ELECTRONICS CO., LTD.,  
and SAMSUNG ELECTRONICS  
AMERICA, INC.,

Defendants and Counter-  
Claimants.

Case No. 2:15-CV-1503

**JURY TRIAL DEMANDED**

**SAMSUNG'S [FIRST AMENDED](#) INVALIDITY CONTENTIONS**

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## **I. INTRODUCTION**

Pursuant to Rule 3-3 of the Local Patent Rules (“P.R.”) of the Eastern District of Texas, Defendants and Counter-Claimants Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively referred to as “Samsung”) hereby provide their [First Amended](#) Invalidity Contentions with respect to the claims identified by Plaintiff TiVo Inc. (“TiVo” or “Plaintiff”) in its Disclosure of Asserted Claims and Infringement Contentions under Patent Rule 3-1 served on February 8, 2016.<sup>1</sup> TiVo asserted claims of four patents: United States Patent No. 6,233,389 (“the ’389 Patent”); United States Patent No. 6,792,195 (“the ’195 Patent”); United States Patent No. 7,558,472 (“the ’472 Patent”); and United States Patent No. 8,457,476 (“the ’476 Patent”) (collectively referred to as “the TiVo patents-in-suit”). According to TiVo, the current asserted claims are claims 1, 2, 3, 5-7, 12, 13, 18-23, 31-34, 36-38, 43, 44, 49-53 and 61 of the ’389 Patent; claims 58-60, 64, 73, 75-79, 83, 92, 94-96, 119, and 121-122 of the ’195 Patent; claims 1, 12-16, 20, 22, 23, 30, and 32 of the ’472 Patent; and claims 1, 6-11, 13, and 14 of the ’476 Patent (collectively referred to as “the asserted claims”).

Pursuant to P.R. 3-3 and 3-4, Samsung hereby provides disclosures and related documents pertaining only to the asserted claims as identified by Plaintiff in its Infringement

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<sup>1</sup> The Patent Rules, and the Docket Control Order jointly submitted by TiVo and Samsung, contemplate that these Invalidity Contentions would be prepared and served in response to TiVo’s Infringement Contentions. However, TiVo’s Infringement Contentions are insufficient because they lack proper and complete disclosure as to how TiVo contends that Samsung allegedly infringes the asserted claims. With respect to certain of the deficiencies in TiVo’s infringement contentions, Samsung has moved the Court to compel TiVo to comply with P.R. 3-1 (Dkt. No. 51). Due to TiVo’s failure to provide proper and complete disclosure of its Infringement Contentions under P.R. 3-1, Samsung reserves the right to seek leave from the Court to modify, amend, and/or supplement these Invalidity Contentions should TiVo be allowed by the Court to correct, clarify, amend, and/or supplement its Infringement Contentions, or its inherent claim constructions, or following the Court’s claim construction.

Contentions.<sup>2</sup> With respect to each asserted claim and based on the investigation to date, Samsung hereby: (a) identifies each currently known item of prior art that either anticipates or renders obvious each asserted claim; (b) specifies whether such prior art anticipates each asserted claim or renders it obvious; (c) submits a chart identifying where each element in each asserted claim is disclosed, described, or taught in the prior art, including for each element that is governed by 35 U.S.C. § 112 ¶ 6, the identity of the structure(s), act(s), or material(s) in each item of prior art that performs the claimed function; and (d) identifies the grounds for invalidating asserted claims based on indefiniteness under 35 U.S.C. § 112 ¶ 2 or enablement or written description under 35 U.S.C. § 112 ¶ 1. Samsung further relies on and incorporates all prior art references cited in the TiVo patents-in-suit and their respective prosecution histories.

In addition, pursuant to P.R. 3-4(a) and (b) and based on its investigation to date, Samsung hereby produces documents currently in its possession, custody, or control required to accompany these Invalidity Contentions.

## **II. RESERVATION OF RIGHTS**

Consistent with P.R. 3-6, the Court's Docket Control Order, and in view of the following, Samsung reserves the right to supplement or otherwise amend these Invalidity Contentions.

First, the information and documents that Samsung produces are based on information currently available to Samsung and subject to further revision. For example, Samsung has diligently attempted to obtain invalidity contentions and prior art from the Prior TiVo Litigations,<sup>3</sup> as well as additional prior art. Specifically, on the parties' February 8, February 18,

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<sup>2</sup> Samsung reserves the right to modify, amend, or supplement these Invalidity Contentions to show the invalidity of any additional claims that the Court may allow TiVo to later assert.

<sup>3</sup> *E.g.*, *TiVo v. EchoStar*, Civil Action No. 2:04-cv-01 (E.D. Tex.); *TiVo Inc. v. AT&T Inc.*, Civil Action No. 2:09-cv-259 (E.D. Tex.); *TiVo Inc. v. Verizon Communications, Inc.*, Civil Action No. 2:09-cv-257 (E.D. Tex.); *Motorola Mobility, Inc. v. TiVo Inc.*, Civil Action No. 5:11-

February 26, and March 3, 2016 meet-and-confers, and in Samsung's March 10 correspondence, Samsung requested documents from the Prior TiVo Litigations in TiVo's possession that did not contain confidential information, specifically requesting documents relevant to the P.R. 3-4 deadline.

After TiVo failed to produce these documents following the opening of discovery, Samsung repeatedly attempted to follow up with TiVo, again specifically requesting documents relevant to the upcoming P.R. 3-4 deadline. (*See* 3/15/16, 3/17/16, 3/22/16, and 3/23/16 Ltrs fr Alper to Werner.) TiVo's March 24, 2016 response did not address when TiVo would produce the requested documents. On the parties' March 25, 2016 meet and confer, TiVo stated that it aimed to produce non-confidential documents from the Prior TiVo Litigations and invalidity contentions (lacking third party confidential information) by early the following week (the week of March 28, 2016).

Thus, TiVo did not produce until March 30, 2016 what it professed to be invalidity contentions lacking third party confidential information,<sup>4</sup> yet TiVo still has not produced the majority of non-confidential prior art cited in these invalidity contentions. (*See* 4/25/16 Ltr fr Alper to Werner.) Further, TiVo has not produced the invalidity contentions from the Prior TiVo Litigations containing material designated confidential by third parties or any prior art containing such material designated a third party as confidential, which Samsung expects will be timely produced pursuant to the Protective Order entered April 21, 2016. (Dkt. 55.)

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cv-053 (E.D. Tex.); *TiVo Inc. v. Cisco Systems, Inc.*, Civil Action No. 2:12-cv-00311 (E.D. Tex.).

<sup>4</sup> TiVo has still not produced EchoStar's invalidity contentions, stating that none exist. (*See* 4/13/16 email from Alper to Werner regarding 4/12/16 meet and confer.) Samsung attempted to obtain these contentions from EchoStar via a subpoena served on March 28, 2016, but EchoStar has not been able to locate invalidity contentions, in charts or interrogatory responses.

Given TiVo's refusal to produce this material, Samsung has also diligently attempted to obtain prior art from the following third parties via subpoenas: Texas Instruments (served March 29, 2016), Verizon (served March 25, 2016), Anthony Wood of Roku and formerly of ReplayTV (served March 28, 2016), STM Microelectronics (served April 21, 2016), Broadcom (served April 21, 2016), and Microsoft Corp. (served April 22, 2016). To date, the third-party subpoena recipients were either unable to produce responsive documents without a Protective Order<sup>5</sup> or are still working to locate relevant documents.<sup>6</sup> Samsung has not yet completed its discovery from these and other third parties who likely have information concerning the prior art identified herein and additional prior art. Such discovery likely will reveal information that affects the disclosures and contentions herein.

Second, Samsung's invalidity contentions are based on the conception and/or reduction to practice dates that TiVo provided in its P.R. 3-1 disclosures. Samsung reserves the right to supplement these contentions based on the alleged invention dates provided by TiVo for the first time in its responses to Samsung's First Set of Interrogatories, served by TiVo on April 18, 2016.

Third, Samsung's invalidity contentions are based on TiVo's P.R. 3-1(c) infringement contentions served February 8, 2016. As set forth in Samsung's February 19 and March 16, 2016 letters to TiVo, as well as on the parties' March 25, 2016 meet and confer and in Samsung's pending motion to compel (Dkt. 51), and as detailed in footnote 1, *supra*, TiVo's infringement contentions fail to put Samsung on notice of TiVo's infringement allegations as required by P.R. 3-1(c). Samsung reserves the right to supplement its invalidity contentions,

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<sup>5</sup> The Court entered the Protective Order (Dkt. 55) on April 21, 2016.

<sup>6</sup> [Texas Instruments served a document production in response to Samsung's subpoena on all parties on April 29, 2016. See TI-0000001-TI-0016157.](#)

including identifying and charting additional prior art, if and when TiVo supplements its infringement contentions.

Fourth, Samsung reserves the right to revise its ultimate contentions concerning the invalidity of the asserted claims, which contentions may change depending upon the Court's construction of the asserted claims, any findings as to the priority date of the asserted claims, and/or positions that Plaintiff or its expert witness(es) may take concerning claim construction, infringement, and/or invalidity issues. Prior art not included in this disclosure, whether known or not known to Samsung, may become relevant. In particular, Samsung is currently unaware of the extent, if any, to which Plaintiff will contend that limitations of the asserted claims are not disclosed in the prior art identified by Samsung, or will contend that any of the identified references do not qualify as prior art. To the extent that such an issue arises, Samsung reserves the right to identify other well-known components or references that *inter alia* would have made the addition of the allegedly missing limitation to the disclosed device or method obvious.

The identification of any prior art patent or patent publication shall be deemed to include any counterpart patent or application filed, published, or issued anywhere in the world. The citation to any specifications published by standard-setting organizations shall be deemed to include any product that implements such specifications and that would qualify as prior art under 35 U.S.C. § 102, *e.g.*, under Section 102(a), 102(b), or 102(g).

Samsung's invalidity claim charts cite to particular teachings and disclosures of the prior art as applied to features of the asserted claims. However, persons having ordinary skill in the art generally may view an item of prior art in the context of other publications, literature, products, and understanding. As such, the cited portions are only examples, and Samsung reserves the right to rely on uncited portions of the prior art references and on other publications

and expert testimony as aids in understanding and interpreting the cited portions, as providing context thereto, and as additional evidence that the prior art discloses a claim limitation.

Samsung further reserves the right to rely on uncited portions of the prior art references, other publications, and testimony to establish bases for combinations of certain cited references that render the asserted claims obvious. Further, for any combination, Samsung reserves the right to rely additionally on information generally known to those skilled in the art and/or common sense.

The references discussed in the claim charts may disclose the elements of the asserted claims explicitly and/or inherently, and/or they may be relied upon to show the state of the art in the relevant period. The suggested obviousness combinations are provided in the alternative to Samsung's anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not by itself anticipatory.

For purposes of these Invalidity Contentions, Samsung identifies prior art references and provides element-by-element claim charts based in part on the apparent constructions of the asserted claims advanced by TiVo in its Infringement Contentions. Nothing stated herein shall be treated as an admission or suggestion that Samsung agrees with TiVo regarding either the scope of any of the asserted claims or the claim constructions advanced by it in its Infringement Contentions or anywhere else. Instead, the citation of prior art herein and the accompanying exhibits are being disclosed as, and should be construed as, nothing more than Samsung's Invalidity Contentions. These documents are not intended to reflect Samsung's claim construction contentions, which will be disclosed in due course in accordance with the Court's Docket Control Order (Dkt. No. 42) jointly submitted by the parties.



Samsung further reserves the right to assert that the TiVo patents-in-suit are unenforceable due to inequitable conduct at least on the grounds that any of the prior art references identified herein were material and withheld with an intent to deceive the patent office.

Pursuant to P.R. 3-3 and 3-4, Samsung hereby provides disclosures and related documents pertaining only to the asserted claims as identified by Plaintiff in its Infringement Contentions.<sup>7</sup>

### **III. IDENTIFICATION OF PRIOR ART PURSUANT TO P.R. 3-3(A)**<sup>8</sup>

Pursuant to P.R. 3-3(a), and subject to Samsung's reservation of rights, Samsung identifies each item of prior art that anticipates or renders obvious one or more of the asserted claims in the tables below. The tables below provide (a) the identity of each prior art patent, including identifying each patent by its patent number, country of origin, and date of issue; (b) the identity of each non-patent prior art publication including, where possible, its title, date of publication, and author and/or publisher; (c) the identity of each item of prior art under 35 U.S.C. § 102(b) including, where possible, the name of the item offered for sale or publicly used or known, the date the offer or use took place or the information became known, and the identity of the person or entity which made the use or made and received the offer, or the person or entity which made the information known or to whom it was made known; and (d) the identity of each item of prior art under 35 U.S.C. § 102(g) including, where possible, the identities of the

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<sup>7</sup> Samsung reserves the right to modify, amend, or supplement these Invalidity Contentions to show the invalidity of any additional claims that the Court may allow Plaintiff to later assert.

<sup>8</sup> Samsung incorporates by reference evidence and other documentation relating to the prior art, and prior uses identified in the invalidity contentions served by the accused infringers in the Prior TiVo Litigations.

person(s) or entities involved in and the circumstances surrounding the making of the invention before the patent applicant.

Samsung reserves the right to assert that the asserted claims are invalid under 35 U.S.C. §102(f) in the event Samsung obtains evidence that the named inventors of any of the asserted patents did not invent (either alone or in conjunction with others) the subject matter claimed in any of the asserted patents on which they are named as inventors. Should Samsung obtain such evidence, it will provide the name of the person(s) from whom and the circumstances under which the invention or any part of it was derived.

Samsung further intends to rely on inventor and party admissions concerning the scope of the prior art relevant to the TiVo patents-in-suit found in, *inter alia*: the patent prosecution history for the TiVo patents-in-suit and related patents and/or patent applications; any deposition testimony of the named inventors on the TiVo patents-in-suit; and the papers filed and any evidence submitted by Plaintiff in conjunction with this litigation.

Discovery is ongoing, and Samsung's prior art investigation and third-party discovery is therefore not yet complete. Samsung reserves the right to present additional items of prior art under 35 U.S.C. § 102(a), (b), (e), and/or (g), and/or § 103 located for the reasons outlined above. For example, Samsung has issued subpoenas to third parties believed to have knowledge, documentation and/or corroborating evidence concerning some of the prior art listed in the tables below and/or additional prior art, and Samsung may serve additional such third-party subpoenas. These third parties include without limitation the authors, inventors, or assignees of the references listed in these disclosures. In addition, Samsung reserves the right to assert invalidity under 35 U.S.C. § 102(c), (d), or (f) to the extent that discovery or further investigation yield information forming the basis for such invalidity.

**A. Identification of Prior Art Pursuant to P.R. 3-3(a) for the '389 Patent****1. Prior Art Patents and Applications**

The following prior art references anticipate and/or render obvious the asserted claims of the '389 patent and describe the state of the art:

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent No. 5,057,932 to Lang	15-Oct-91	Lang_932
U.S. Patent No. 5,126,982 to Yifrach	30-Jun-92	Yifrach_982
U.S. Patent No. 5,132,992 to Yurt et al	21-Jul-92	Yurt_992
U.S. Patent No. 5,164,839 to Lang	17-Nov-92	Lang_839
U.S. Patent No. 5,241,428 to Goldwasser et al	31-Aug-93	Goldwasser_428
U.S. Patent No. 5,329,320 to Yifrach	12-Jul-94	Yifrach_320
U.S. Patent No. 5,371,551 to Logan et al	06-Dec-94	Logan_551
U.S. Patent No. 5,442,390 to Hooper et al	15-Aug-95	Hooper_390
U.S. Patent No. 5,438,423 to Lynch et al	01-Aug-95	Lynch_423
U.S. Patent No. 5,473,744 to Allen et al	05-Dec-95	Allen_744
U.S. Patent No. 5,513,011 to Matsumoto et al.	30-Apr-96	Matsumoto_011
U.S. Patent No. 5,557,724 to Sampat et al.	17-Sep-96	Sampat_724
U.S. Patent No. 5,559,999 to Maturi et al	24-Sep-96	Maturi_999
U.S. Patent No. 5,584,006 to Reber et al	10-Dec-96	Reber_006
U.S. Patent No. 5,614,940 to Cobbley et al	21-Oct-94	Cobbley_940
U.S. Patent No. 5,659,539 to Porter et al	19-Aug-97	Porter_539
U.S. Patent No. 5,696,868 to Kim et al	09-Dec-97	Kim_868
U.S. Patent No. 5,701,383 to Russo et al	23-Dec-97	Russo_383
U.S. Patent No. 5,719,786 to Nelson et al	17-Feb-98	Nelson_786
U.S. Patent No. 5,721,815 to Ottesen et al	24-Feb-98	Ottesen_815
U.S. Patent No. 5,721,878 to Ottesen et al	24-Feb-98	Ottesen_878
U.S. Patent No. 5,729,280 to Inoue et al	17-Mar-98	Inoue_280

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent No. 5,774,186 to Brodsky et al	30-Jun-98	Brodsky_186
U.S. Patent No. 5,815,689 to Shaw et al	4-Oct-98	Shaw_689
U.S. Patent No. 5,822,493 to Uehara et al	13-Oct-98	Uehara_493
U.S. Patent No. 5,898,695 to Fuji et al	27-Apr-99	Fuji_695
U.S. Patent No. 5,930,444 to Camhi et al	27-Jul-99	Camhi_444
U.S. Patent No. 5,949,948 to Krause et al	7-Sep-99	Krause_948
U.S. Patent No. 5,956,716 Kenner et al	21-Sep-99	Kenner_716
U.S. Patent No. 5,973,679 to Abbott et al	26-Oct-99	Abbot_679
U.S. Patent No. 5,978,855 to Metz et al	2-Nov-99	Metz_855
U.S. Patent No. 5,990,881 to Inoue et al	23-Nov-99	Inoue_881
U.S. Patent No. 5,999,691 to Takagi et al	7-Dec-99	Takagi_691
U.S. Patent No. 6,002,832 to Yoneda	14-Dec-99	Yoneda_832
U.S. Patent No. 6,005,564 to Ahmad et al	21-Dec-99	Ahmad_564
U.S. Patent No. 6,018,612 to Thomason et al	25-Jan-00	Thomason_612
U.S. Patent No. 6,064,792 to Fox et al	16-May-00	Fox_792
U.S. Patent No. 6,081,750 to Hoffberg et al	27-Jun-00	Hoffberg_750
U.S. Patent No. 6,112,226 to Weaver et al	29-Aug-00	Weaver_226
U.S. Patent No. 6,138,221 to Korst et al	24-Oct-00	Korst_221
U.S. Patent No. 6,167,083 to Sporer et al	26-Dec-01	Sporer_083
U.S. Patent No. 6,169,842 to Pijnenburg et al	02-Jan-01	Pijnenburg_842
U.S. Patent No. 6,169,843 to Lenihan et al	02-Jan-01	Lenihan_843
U.S. Patent No. 6,169,844 to Arai	02-Jan-01	Arai_844
U.S. Patent No. 6,172,712 to Beard et al	09-Jan-01	Beard_712
U.S. Patent No. 6,181,706 to Anderson et al	30-Jan-01	Anderson_706
U.S. Patent No. 6,226,447 to Sasaki et al	01-May-01	Sasaki_447
U.S. Patent No. 6,285,746 to Duran et al	04-Sep-01	Duran_746

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent No. 6,209,041 to Shaw et al	27-Mar-01	Shaw_041
U.S. Patent No. 6,304,714 to Krause et al	16-Oct-01	Krause_714
U.S. Patent No. 6,334,022 to Ohba et al	25-Dec-01	Ohba_022
U.S. Patent No. 6,370,323 to Adolph et al	09-Apr-02	Adolph_323
U.S. Patent No. 6,385,386 to Aotake	07-May-02	Aotake_386
U.S. Patent No. 6,445,738 to Zdepski et al	03-Sep-02	Zdepski_738
U.S. Patent No. 6,480,667 to OConnor	12-Nov-02	OConnor_667
U.S. Patent No. 6,490,000 to Schaefer et al	03-Dec-02	Schaefer_000
U.S. Patent No. 6,944,185 to Patki et al	13-Sep-05	Patki_185
U.S. Patent No. 7,272,298 to Lang et al	18-Sep-07	Lang_298
U.S. Patent No. 5,844,478 to Blatter et al.	1-Dec-98	Blatter_478
U.S. Patent No. 5,909,559 to So	1-Jun-99	So_559
U.S. Patent No. 5,619,337 to Naimpally	8-Apr-97	Naimpally_337
U.S. Patent No. 6,369,855 to Chauvel et al.	9-Apr-02	Chauvel_855
U.S. Patent No. 5,812,976 to Ryan	22-Sep-98	Ryan_976
U.S. Patent No. 5,889,949 to Charles	30-Mar-99	Charles_949
U.S. Patent No. 6,425,054 to Nguyen	23-Jul-02	Nguyen_054
U.S. Patent No. 5,684,804 to Baronetti et al.	04-Nov-97	Baronetti_804
U.S. Patent No. 6,058,459 to Owen et al.	02-May-2000	Owen_459
U.S. Patent No. 5,801,785 to Crump et al.	01-Sep-98	Crump_785
U.S. Patent No. 5,661,665 by Glass et al.	26-Aug-97	Glass_665
U.S. Patent No. 6,330,675 to Wiser et al.	11-Dec-01	Wiser_675
U.S. Patent No. 5,913,038 to Griffiths	15-Jun-99	Griffiths_038
U.S. Patent No. 5,809,538 to Pollman	15-Sep-98	Pollman_538
U.S. Patent No. 5,598,542 to Leung	28-Jan-97	Leung_542
U.S. Patent No. 6,282,045 to Glover	28-Aug-01	Glover_045

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent No. 6,134,638 to Olarig	17-Oct-00	Olarig_638
U.S. Patent Pub. No. 2002/0057892 to Mano	16-May-02	Mano_892
U.S. Patent No. 5,970,220 to Bolash et al.	19-Oct-99	Bolash_220
U.S. Patent No. 5,990,875 to Bi et al.	23-Nov-99	Bi_875
U.S. Patent No. 5,708,819 to Dunnihoo	13-Jan-98	Dunnihoo_819
U.S. Patent No. 6,385,711 to Colligan	07-May-02	Colligan_711
European Patent No. EP 0594241 by Thomason et al	06-May-99	Thomason_241
European Patent Application No. EP 0785675 by Yamada et al	23-Jul-97	Yamada_675
European Patent Application No. EP0762756A2 by Sasaki et al	17-Jun-1998	Sasaki_756
European Patent No. EP 1376449 to Shin et al.	02-Mar-05	Shin_449

## 2. Prior Art Publications

The following prior art references anticipate and/or render obvious the asserted claims of the '389 patent and describe the state of the art:<sup>9</sup>

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication/ Use Date</b>	<b>Referenced As</b>
David P. Anderson et al.	A File System for Continuous Media	No later than Nov 1992	Anderson
Kageyama et al.	A Free Time Shift DVD Video Recorder	No later than Aug 1997	Kageyama
Patrick Wai-Ho Chan	A Mobile System for Distributed Multimedia Applications	No later than 1996	Chan

<sup>9</sup> As detailed in § II Reservation of Rights, TiVo continues to unreasonably delay and withhold production of many prior art references, invalidity charts, and other portions of prior invalidity contentions, and has yet to produce confidential prior art materials and contentions.

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication/ Use Date</b>	<b>Referenced As</b>
David J. Wetherall	An Interactive Programming System for Media Computation	No later than Sep 1994	Wetherall
Christopher Lindblad	A Programming System for the Dynamic Manipulation of Temporally Sensitive Data	No later than 1994	Lindblad
Demura et al.	A Single-Chip MPEG2 Video Decoder LSI	No later than Feb 1994	Demura
Cline et al.	DirectShow RTP Support for Adaptivity in Networked Multimedia Applications	No later than Jun 1998	Cline
R. Johnston et al	A Digital Television Sequence Store	No later than May 1978	Johnston
Jonathan Soo	An Architecture for Networked Multimedia	No later than Aug 1995	Soo
Hanna et al.	Demultiplexer IC for MPEG2 Transport Streams	No later than Aug 1995	Hanna
Philipp Ackermann	Developing Object-Oriented Multimedia Software	No later than 1996	Ackermann
Texas Instruments	TMS320AV7110 Integrated Digital Set-top Box Decoder Functional Specification	No later than July 6, 1998	AV7110
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7110 Integrated Digital Set-top Box Decoder Product Preview</a>	<a href="#">No later than Sep 1997</a>	<a href="#">AV7110 Preview<sup>10</sup></a>
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7100 Integrated Digital Set-top Digital Signal Processor</a>	<a href="#">No later than Oct 1997</a>	<a href="#">AV7100 Preview<sup>11</sup></a>
Rothermel et al.	An adaptive protocol for synchronizing media streams	No later than Sep 1997	Rothermel

<sup>10</sup> See [TI-0003066-TI-0003165 \(AV7110 Preview\)](#); [TI-0000001-TI-0016157 \(related materials\)](#).

<sup>11</sup> See [TI-0002936-TI-0002997 \(AV7100 Preview\)](#); [TI-0000001-TI-0016157 \(related materials\)](#).

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication/ Use Date</b>	<b>Referenced As</b>
Ron Wilson	DTV makes it big entrance	No later than Feb 25, 1998	Wilson
Neuman et al.	How to reduce memory in DVD systems	No later than Aug 25, 1997	Neuman
John Parsons	Digital video architecture for OS-2 2.1	No later than Feb 1994	Parsons
Bescós et al.	From Multimedia Stream Models to GUI Generation	No later than March 1997	Bescós
Asthana et al.	Kaleido: A System for Dynamic Composition and Processing of Multimedia Flows by	No later than Oct 1995	Kaleido
Miller et al.	An Integrated Input/Output System for Kernel Data Streaming	No later than Jan 24, 1998	Miller
Christopher J. Lindblad et al.	The VuSystem: A Programming System for Compute-Intensive Multimedia	No later than Sep 1996	VuSystem
Coulson	Micro-Kernel Support for Continuous Media in Distributed Systems	No later than 1994	Coulson
Jeffay	Kernel Support for Live Digital Audio and Video	No later than 1992	Jeffay
Bove	Cheops: A Reconfigurable Data- Flow System for Video Processing	No later than 1995	Bove
Wanda Gass	Architecture Trends of MPEG Decoders for Set-Top Box	No later than January 1997	Gass
Steven Niemczyk	Stream Objects: Dynamically- Segmented Scalable Media Over the Internet	No later than Jun 1996	Niemczyk
Ruihong Wang	Design of a Storage and Retrieval Model for Multimedia Data	No later than 1994	Wang



<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication/ Use Date</b>	<b>Referenced As</b>
Thomas Peuker	An Object-Oriented Architecture for the Real-Time Transmission of Multimedia Data Streams	No later than Mar 17, 1997	Peuker
Ramakrishnan et al.	Operating System Support for a Video-On-Demand File Service	No later than Nov 1993	Ramakrishnan
Rangan et al.	Designing File Systems for Digital Video and Audio"	No later than Oct 1991	Rangan
K. Almeroth et al.	On the Use of Multicast Delivery to Provide a Scalable and Interactive Video-On-Demand Service by	No later than Aug 1996	Almeroth Multicast
S. Gibbs et al.	Multimedia Programming: Objects, Environments, and Frameworks	No later than 1995	Gibbs_Multimedia
Patel et al.	Synchronized Continuous Playback through the World Wide Web	No later than 1996	Patel
C. Alexandrou	Multimedia Data Exchange Agent: an Object Behavioral Pattern for Multimedia Programming.	Not later than 1997	Alexandrou
Rowe et al.	MPEG Video in Software: Representation, Transmission, and Playback	No later than 1994	Rowe
K. Almeroth et al.	The Interactive Multimedia Jukebox (IMJ): A New Paradigm for the On-Demand Delivery of Audio/Video	No later than Apr 1998	Almeroth IMJ
Holfelder	MBone VCR - Video Conferencing Recording on the MBone	No later than Apr 1997	Holfelder
Kurioka et al.	Television Home Server for Integrated Services - Toward the Realization of ISDB Anytime Services	No later than Jan 1998	Kurioka

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication/ Use Date</b>	<b>Referenced As</b>
David Clark et al.	Aurora at MIT - Final Report on MIT's Participation in the Aurora Gigabit Testbed	No later than 1995	Clark
Coelho et al.	DirectX, RDX, RSX, and MMX Technology	No later than Dec 1997	Coelho
Legault et al.	Professional Video Under 32-Bit Windows Operating Systems	No later than Dec 1996	Legualt
Bacher et al.	Content-based Indexing of Captioned Video on the ViewStation	No later than Oct 1995	Bacher
J. Adam et al.	Experience with the VuNet - A Network Architecture for a Distributed Multimedia System	No later than 1994	Adam
Lars Wolf	Resource Management for Distributed Multimedia Systems	No later than 1996	Wolf
Chatterjee	Microsoft ActiveMovie: a new media architecture	No later than Feb 1997	Chatterjee
Gibbs et al.	Audio/Video Databases: An Object-Oriented Approach	No later than 1993	Gibbs
Anderson et al.	Support for Continuous Media in the Dash System	No later than 1989	Anderson DASH
Eric H.J. Persoon	SMASH – a concept for advanced use of storage in the home	No later than Mar 1998	Persoon
Eric Persoon	Set Top Unit with (SMASH) Storage	No later than Dec 4, 1996	SMASH System
ReplayTV	ReplayTV 4000 Series User Guide	No later than 2001	RTV4000 Guide
Watlington et al	Stream-Based Computing and Future Television	No later than 1995	Watlington
Ennis	Open Digital media Solutions Using Windows NT	No later than Sep 16, 1996	Ennis

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication/ Use Date</b>	<b>Referenced As</b>
Andy Santoni	PC 98 spec pushes CPU speeds, moves away from ISA bus	No later than Apr 21, 1997	Santoni
Brooke Crothers et al.	Microsoft Touts Need for Multimedia Bus	No later Mar 27, 1995	Crothers
Purcell	The Mpact 2 VLIW Media Processor Improves Multimedia Performance in PCs	No later than Mar 1998	Mpact2
Owen et al.	An Enhanced DSP Architecture for the Seven Multimedia Functions: The Mpact 2 Media Processor	No later than May 1997	Mpact2
ESS Technology, Inc.	ESS3301 A/V Transport Demultiplexer, Descrambler Product Brief	No later than 1998	ESS Products
ESS Technology, Inc.	ESS3308 MPEG2 Audio/Video Decoder Product Brief	No later than 1998	ESS Products
LSI Logic	L64007 MPEG-2, DVB, JSAT Transport Demultiplexer Technical Manual	No later than Jan 16, 1997	LSI Logic Chipset
LSI Logic	L64005 Enhanced MPEG-2 Audio/Video Decoder Technical Manual	No later than May 1998	LSI Logic Chipset
LSI Logic	L64704 Satellite Decoder Technical Manual	No later than May 1997	LSI Logic Chipset
Aaron Hawes	The Design of an IVDS World Wide Web Browser Architecture	No later than Dec 1997	LSI Logic Chipset
Lee et al.	MediaStation 5000: Integrating Video and Audio	No later than 1994	MediaStation5000
Lee et al.	Applying Multimedia to Medical Imaging	No later than Apr 1996	MediaStation5000
Philips	Tri-Media TM-1100 Datasheet	No later than 1998	Philips TM-1 chip

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication/ Use Date</b>	<b>Referenced As</b>
Rathnam et al.	An Architectural Overview of the Programmable Multimedia Processor, TM-1	No later than 1996	Philips TM-1 chip
STMicro	STi5500: Set Top Box Backend Decoder with Integrated Host Processor	No later than Oct 1997	STi5500
Chris Carter	ICs for Next Generation Set-top Boxes	No later than Dec 1997	STi5500
STMicro	SGS-THOMSON Launches STi5500, After Delivering 10 Millionth MPEG Decoder	No later than Apr 21, 1997	STi5500
STMicro	Two European IT Prizes Awarded to STMicroelectronics	No later than Nov 26, 1998	STi5500
STMicro	STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than July 1998	STi5510
Toshiba	Toshiba: TC81220F MPEG2 Video Audio Decoder, Transport Stream Processor RISC 32-bit MIPS System CPU	No later than 1998	Toshiba TC81220F
Yamada et al.	A Flexible MPEG2 Decoder LSI with a Special Transport Stream RISC Processor	No later than Mar 1998	Toshiba TC81220F
C-Cube Microsystems	AViA-DMX MPEG-2 Transport Demultiplexer AViA-GTX Graphics Transport I/O User's Manual	Not later than Dec 1996	Avia DMX-GTX User Manual

### **3. Non-Patent/Publication References**

Samsung also contends that the asserted claims of the '389 patent are invalid for public use and/or offers for sale of products and services that anticipate the asserted claims of the '389 patent under 35 U.S.C. § 102(b) and/or the purported invention of the asserted claims was made in this country by another inventor who had not abandoned, suppressed, or concealed it under 35

U.S.C. § 102(g). Samsung contends that the following description and events are stated on information and belief, and are supported by the information and documents that will be produced by Samsung, TiVo, and/or third parties.<sup>12</sup> As discovery has only just begun, Samsung continues to investigate these events.

System Name	Use/Knowledge/Offer Date	Primary Publisher
Texas Instruments <a href="#">AV7100 &amp; AV7110</a>	No later than 1996 <i>See, e.g.,</i> AV7110- <del>Specification</del> , <a href="#">AV7110 Preview</a> , <a href="#">AV7100 Preview</a> , Chauvel 855, Gass	Texas Instruments
Microsoft ActiveMovie/DirectShow	No later than 1996 <i>See, e.g.,</i> Coelho, Griffiths, Ennis, Legault, Glass, Chatterjee	Microsoft
Loronix CCTVware Enterprise and Loronix CCTVware Solo	At least by 1996	Loronix Information Systems
Replay TV DVR	At least by November 1997  Public Use: At least by January 1999  <i>See, e.g.,</i> RTV4000 System	ReplayTV
VuSystem	No later than 1994 <i>See, e.g.,</i> VuSystem	MIT / Christopher Lindblad
STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than June 1998 <i>See, e.g.,</i> STi5510	STMicroelectronics

<sup>12</sup> As detailed in § II Reservation of Rights, TiVo continues to unreasonably delay and withhold production of many prior art references, invalidity charts, and other portions of prior invalidity contentions, and has yet to produce confidential prior art materials and contentions.

<b>System Name</b>	<b>Use/Knowledge/Offer Date</b>	<b>Primary Publisher</b>
ESS Products ( <i>e.g.</i> , ESS3308 MPEG2 Audio/Video Decoder)	No later than 1998  <i>See, e.g.</i> , ESS Products	ESS Technology, Inc.
LSI Logic Chipset ( <i>e.g.</i> , L64005 Enhanced MPEG-2 Audio/Video Decoder)	No later than May 1998  <i>See, e.g.</i> , LSI Logic Chipset	LSI Logic
MediaStation5000	No later than Dec 1994  <i>See, e.g.</i> , MediaStation 5000	Univ of Washington/Texas Instruments
Toshiba TC81220F MPEG2 Video Audio Decoder, Transport Stream Processor RISC 32-bit MIPS System CPU	No later than Mar 1998  <i>See, e.g.</i> , Toshiba TC81220F	Toshiba
AViA-DMX MPEG-2 Transport Demultiplexer AViA-GTX Graphics Transport I/O	No later than Dec 1996  <i>See, e.g.</i> , Avia DMX-GTX	C-Cube Microsystems
Tri-Media TM-1100	No later than 1996  <i>See, e.g.</i> , Philips TM-1 chip	Philips

**B. Identification of Prior Art Pursuant to P.R. 3-3(a) for the '195 Patent**

**1. Prior Art Patents and Applications**

The following prior art references anticipate and/or render obvious the asserted claims of the '195 patent and describe the state of the art:

<b>Patent</b>	<b>Date of Issue / Publication</b>	<b>Referenced As</b>
U.S. Patent No. 5,973,679 Abbott et al	26-Oct-99	Abbott_679
U.S. Patent No. 5,825,354 to Ahmad et al	20-Oct-98	Ahmad_354

<b>Patent</b>	<b>Date of Issue / Publication</b>	<b>Referenced As</b>
U.S. Patent No. 6,181,706 to Anderson et al	30-Jan-01	Anderson_706
U.S. Patent No. 6,005,599 to Asai et al	21-Dec-99	Asai_599
U.S. Patent No. 5,774,186 to Brodsky et al	30-Jun-98	Brodsky_186
U.S. Patent No. 5,930,444 to Camhi et al	27-Jul-99	Camhi_444
U.S. Patent No. 6,014,706 to Cannon et al	11-Jan-00	Cannon_706
U.S. Patent No. 6,901,209 to Cooper et al	31-May-05	Cooper_209
U.S. Patent No. 7,058,721 to Ellison et al	6-Jun-06	Ellison_721
U.S. Patent No. 6,236,801 to Engle et al	22-May-01	Engle_801
U.S. Patent No. 5,845,240 to Fielder	1-Dec-98	Fielder_240
U.S. Patent No. 5,898,695 to Fujii et al	27-Apr-99	Fujii_695
U.S. Patent No. 5,568,274 to Fujinami et al	22-Oct-96	Fujinami_274
U.S. Patent No. 5,241,428 to Goldwasser et al	31-Aug-93	Goldwasser_428
U.S. Patent No. 6,188,650 to Hamada et al	13-Feb-01	Hamada_650
U.S. Patent No. 6,005,600 to Hill	21-Dec-99	Hill_600
U.S. Patent No. 6,263,152 to Hisatomi et al	17-Jul-01	Hisatomi_152
U.S. Patent No. 5,442,390 to Hooper et al	15-Aug-95	Hooper_390
U.S. Patent No. 5,414,455 to Hooper et al	9-May-95	Hooper_455
U.S. Patent No. 5,729,280 to Inoue et al	17-Mar-98	Inoue_280
U.S. Patent No. 5,706,388 to Isaka	6-Jan-98	Isaka_388
U.S. Patent No. 6,115,536 to Iwasaki	5-Sep-00	Iwasaki_536
Japanese Patent Application Publication No. JP 06-245157 to Katayama et al	02-Sep-94	Katayama_JP157
U.S. Patent No. 6,466,733 to Kim	15-Oct-02	Kim_733
U.S. Patent No. 5,696,868 to Kim et al	9-Dec-97	Kim_868
Japanese Patent Application Publication No. JP 06-284364 to Koji	07-Oct-94	Koji_JP364
U.S. Patent No. 6,304,714 to Krause et al	16-Oct-01	Krause_714

<b>Patent</b>	<b>Date of Issue / Publication</b>	<b>Referenced As</b>
U.S. Patent No. 5,949,948 to Krause et al	7-Sep-99	Krause_948
U.S. Patent No. 6,169,843 to Lenihan et al	2-Jan-01	Lenihan_843
U.S. Patent No. 5,371,551 to Logan et al	6-Dec-94	Logan_551
U.S. Patent No. RE36,801 to Logan	01-Aug-00	Logan_801
U.S. Patent No. 5,438,423 to Lynch et al	1-Aug-95	Lynch_423
Japanese Patent Application Publication No. JP 06-178258 to Masahiko	24-Jun-94	Masahiko_JP258
U.S. Patent No. 5,559,999 to Maturi et al	24-Sep-96	Maturi_999
U.S. Patent No. 5,345,430 to Moe	6-Sep-94	Moe_430
U.S. Patent No. 5,719,786 to Nelson et al	17-Feb-98	Nelson_786
U.S. Patent No. 5,477,263 to O'Callaghan et al	19-Dec-95	O'Callaghan_263
U.S. Patent No. 6,480,667 to O'Connor	12-Nov-02	O'Connor_667
U.S. Patent No. 5,721,815 to Ottesen et al	24-Feb-98	Ottesen_815
U.S. Patent No. 5,721,878 to Ottesen et al	24-Feb-98	Ottesen_878
U.S. Patent No. 5,751,883 to Ottesen et al	12-May-98	Ottesen_883
U.S. Patent No. 5,905,602 to Pak	18-May-99	Pak_602
U.S. Patent No. 5,963,202 to Polish	5-Oct-99	Polish_202
U.S. Patent No. 5,659,539 to Porter et al	19-Aug-97	Porter_539
U.S. Patent No. 5,535,137 to Rossmere et al	9-Jul-96	Rossmere_137
U.S. Patent No. 5,701,383 to Russo et al	23-Dec-97	Russo_383
U.S. Patent No. 5,828,416 to Ryan	27-Oct-98	Ryan_416
U.S. Patent No. 5,465,120 to Schultheiss	7-Nov-95	Schultheiss_120
U.S. Patent No. 5,815,689 to Shaw et al	29-Sep-98	Shaw_689
U.S. Patent No. 6,434,748 to Shen et al	13-Aug-02	Shen_748
Japanese Patent Application Publication JP 8-163500 to Shinichi et al	21-Jun-96	Shinichi_JP500
U.S. Patent No. 5,555,463 to Staron	10-Sep-96	Staron_463



<b>Patent</b>	<b>Date of Issue / Publication</b>	<b>Referenced As</b>
U.S. Patent No. 5,140,435 to Suzuki et al	18-Aug-92	Suzuki_435
U.S. Patent No. 5,999,691 to Takagi et al	7-Dec-99	Takagi_691
European Patent No. EP 0594241 by Thomason et al	06-May-99	Thomason_241
U.S. Patent No. 5,822,493 to Uehara et al	13-Oct-98	Uehara_493
Japanese Patent Application Publication No. JP 08-237592 to Uehara et al	13-Mar-96	Uehara_JP592
U.S. Patent No. 5,933,603 to Vahalia et al	3-Aug-99	Vahalia_603
U.S. Patent No. 5,440,334 to Walters et al	8-Aug-95	Walters_334
U.S. Patent No. 5,815,082 to Weimer	29-Sep-98	Weimer_082
U.S. Patent No. 6,289,172 to Windrem et al	11-Sep-01	Windrem_172
U.S. Patent No. 5,535,008 to Yamagishi et al	9-Jul-96	Yamagish_008
U.S. Patent No. 5,329,320 to Yifrach	12-Jul-94	Yifrach_320
U.S. Patent No. 5,126,982 to Yifrach	30-Jun-92	Yifrach_982
U.S. Patent No. 5,132,992 to Yurt et al	21-Jul-92	Yurt_992

## **2. Prior Art Publications**

The following prior art references anticipate and/or render obvious the asserted claims of the '195 patent and describe the state of the art:<sup>13</sup>

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
David P. Anderson et al.	A File System for Continuous Media	No later than Nov 1992	Anderson
Kageyama et al.	A Free Time Shift DVD Video Recorder	No later than Aug 1997	Kageyama
Patrick Wai-Ho Chan	A Mobile System for Distributed Multimedia Applications	No later than 1996	Chan

<sup>13</sup> As detailed in § II Reservation of Rights, TiVo continues to unreasonably delay and withhold production of many prior art references, invalidity charts, and other portions of prior invalidity contentions, and has yet to produce confidential prior art materials and contentions.

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
C. Herpal et al.	Adaptation and Improvement of CCITT Reference Model 8 Video Coding for Digital Storage Media Applications	No later than 1990	Herpal
G. Fleming	An Economical Solution for Video CD	No later than 1995	Fleming
David J. Wetherall	An Interactive Programming System for Media Computation	No later than Sep 1994	Wetherall
Wu-chi Feng	Buffering Techniques for Delivery of Compressed Video In Video-On-Demand Systems	No later than Sep 30, 1997	Feng
Wu-chi Feng	Providing VCR Functionality in a Constant Quality Video-on-Demand Transportation Service	No later than Jun 1996	Feng
Cline et al.	DirectShow RTP Support for Adaptivity in Networked Multimedia Applications	No later than Jun 1998	Cline
ISO	ISO IEC 11172-1, Information technology - Coding of moving pictures and associated audio for digital storage media at up to about 1.5 Mbits - Part 1	No later than Aug 12, 1993	MPEG-1
ITU-T	ITU-T H.222.0 Generic Coding of Moving Pictures and Associated Audio Information	No later than Nov 1996	MPEG-2
Magnavox	Magnavox User Guide	No later than Nov 1995	Magnavox
Rowe et al.	MPEG Video in Software Representation, Transmission, and Playback	No later than Feb 1994	Rowe
Viswanathan et al.	Pyramid broadcasting for video-on-demand service	No later than Mar 14, 1995	Pyramid Broadcasting
K. Almeroth et al.	On the Use of Multicast Delivery to Provide a Scalable and Interactive Video-on-Demand Service	No later than Aug 1995	Almeroth
ReplayTV	ReplayTV 4000 Series User Guide	No later than 2001	RTV4000 Guide

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
Christopher J. Lindblad et al	The VuSystem - A Programming System for Visual Processing of Digital Video	No later than 1994	Lindblad
Eric H.J. Persoon	SMASH – a concept for advanced use of storage in the home	No later than Mar 1998	Persoon
H. Brody	Information Highway: The Home Front	No later than Aug/Sep 1993	Brody
J. Parsons	Digital video architecture for OS-2 2.1	No later than Feb 1994	Parsons
Kurt Rothermel et al.	An adaptive protocol for synchronizing media streams	No later than Sep 1997	Rothermel
Chih-Ta Sung	On the MPEG audio-video synchronization	No later than Jan 1997	Sung
Herman et al.	A standard model for multimedia synchronization: PREMO synchronization objects	No later than Mar 1998	Herman

### **3. Non-Patent/Publication References**

Samsung also contends that the asserted claims of the '195 patent are invalid for public use and/or offers for sale of products and services that anticipate the asserted claims of the '195 patent under 35 U.S.C. § 102(b) and/or the purported invention of the asserted claims was made in this country by another inventor who had not abandoned, suppressed, or concealed it under 35 U.S.C. § 102(g). Samsung contends that the following description and events are stated on information and belief, and are supported by the information and documents that will be produced by Samsung, TiVo, and/or third parties.<sup>14</sup> As discovery has only just begun, Samsung continues to investigate these events.

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<sup>14</sup> As detailed in § II Reservation of Rights, TiVo continues to unreasonably delay and withhold production of many prior art references, invalidity charts, and other portions of prior invalidity contentions, and has yet to produce confidential prior art materials and contentions.

System Name	Use/Knowledge/Offer Date	Primary Publisher
Magnavox TP2792	At least by 1995 <i>See, e.g.,</i> Magnavox	Magnavox
Replay TV DVR	At least by November 1997  Public Use: At least by January 1999  <i>See, e.g.,</i> RTV4000 System	ReplayTV

**C. Identification of Prior Art Pursuant to P.R. 3-3(a) for the '472 Patent**

**1. Prior Art Patents and Applications**

The following prior art references anticipate and/or render obvious the asserted claims of the '472 patent and describe the state of the art:

Patent	Date of Issue/Publication	Referenced As
U.S. Patent No. 5,057,932 to Lang	15-Oct-91	Lang_932
U.S. Patent No. 5,126,982 to Yifrach	30-Jun-92	Yifrach_982
U.S. Patent No. 5,132,992 to Yurt et al	21-Jul-92	Yurt_992
U.S. Patent No. 5,164,839 to Lang	17-Nov-92	Lang_839
U.S. Patent No. 5,241,428 to Goldwasser et al	31-Aug-93	Goldwasser_428
U.S. Patent No. 5,329,320 to Yifrach	12-Jul-94	Yifrach_320
U.S. Patent No. 5,371,551 to Logan et al	06-Dec-94	Logan_551
U.S. Patent No. 5,442,390 to Hooper et al	15-Aug-95	Hooper_390
U.S. Patent No. 5,438,423 to Lynch et al	01-Aug-95	Lynch_423
U.S. Patent No. 5,473,744 to Allen et al	05-Dec-95	Allen_744
U.S. Patent No. 5,513,011 to Matsumoto et al.	30-Apr-96	Matsumoto_011
U.S. Patent No. 5,557,724 to Sampat et al.	17-Sep-96	Sampat_724
U.S. Patent No. 5,559,999 to Maturi et al	24-Sep-96	Maturi_999
U.S. Patent No. 5,584,006 to Reber et al	10-Dec-96	Reber_006

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent No. 5,614,940 to Cobbley et al	21-Oct-94	Cobbley_940
U.S. Patent No. 5,659,539 to Porter et al	19-Aug-97	Porter_539
U.S. Patent No. 5,696,868 to Kim et al	09-Dec-97	Kim_868
U.S. Patent No. 5,701,383 to Russo et al	23-Dec-97	Russo_383
U.S. Patent No. 5,719,786 to Nelson et al	17-Feb-98	Nelson_786
U.S. Patent No. 5,721,815 to Ottesen et al	24-Feb-98	Ottesen_815
U.S. Patent No. 5,721,878 to Ottesen et al	24-Feb-98	Ottesen_878
U.S. Patent No. 5,729,280 to Inoue et al	17-Mar-98	Inoue_280
U.S. Patent No. 5,774,186 to Brodsky et al	30-Jun-98	Brodsky_186
U.S. Patent No. 5,815,689 to Shaw et al	4-Oct-98	Shaw_689
U.S. Patent No. 5,822,493 to Uehara et al	13-Oct-98	Uehara_493
U.S. Patent No. 5,898,695 to Fuji et al	27-Apr-99	Fuji_695
U.S. Patent No. 5,930,444 to Camhi et al	27-Jul-99	Camhi_444
U.S. Patent No. 5,949,948 to Krause et al	7-Sep-99	Krause_948
U.S. Patent No. 5,956,716 to Kenner et al	21-Sep-99	Kenner_716
U.S. Patent No. 5,973,679 to Abbott et al	26-Oct-99	Abbot_679
U.S. Patent No. 5,978,855 to Metz et al	2-Nov-99	Metz_855
U.S. Patent No. 5,990,881 to Inoue et al	23-Nov-99	Inoue_881
U.S. Patent No. 5,999,691 to Takagi et al	7-Dec-99	Takagi_691
U.S. Patent No. 6,002,832 to Yoneda	14-Dec-99	Yoneda_832
U.S. Patent No. 6,005,564 to Ahmad et al	21-Dec-99	Ahmad_564
U.S. Patent No. 6,018,612 to Thomason et al	25-Jan-00	Thomason_612
U.S. Patent No. 6,064,792 to Fox et al	16-May-00	Fox_792
U.S. Patent No. 6,081,750 to Hoffberg et al	27-Jun-00	Hoffberg_750
U.S. Patent No. 6,112,226 to Weaver et al	29-Aug-00	Weaver_226
U.S. Patent No. 6,138,221 to Korst et al	24-Oct-00	Korst_221

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent No. 6,167,083 to Sporer et al	26-Dec-01	Sporer_083
U.S. Patent No. 6,169,842 to Pijnenburg et al	02-Jan-01	Pijnenburg_842
U.S. Patent No. 6,169,843 to Lenihan et al	02-Jan-01	Lenihan_843
U.S. Patent No. 6,169,844 to Arai	02-Jan-01	Arai_844
U.S. Patent No. 6,172,712 to Beard et al	09-Jan-01	Beard_712
U.S. Patent No. 6,181,706 to Anderson et al	30-Jan-01	Anderson_706
U.S. Patent No. 6,226,447 to Sasaki et al	01-May-01	Sasaki_447
U.S. Patent No. 6,285,746 to Duran et al	04-Sep-01	Duran_746
U.S. Patent No. 6,209,041 to Shaw et al	27-Mar-01	Shaw_041
U.S. Patent No. 6,304,714 to Krause et al	16-Oct-01	Krause_714
U.S. Patent No. 6,334,022 to Ohba et al	25-Dec-01	Ohba_022
U.S. Patent No. 6,370,323 to Adolph et al	09-Apr-02	Adolph_323
U.S. Patent No. 6,385,386 to Aotake	07-May-02	Aotake_386
U.S. Patent No. 6,445,738 to Zdepski et al	03-Sep-02	Zdepski_738
U.S. Patent No. 6,480,667 to OConnor	12-Nov-02	OConnor_667
U.S. Patent No. 6,490,000 to Schaefer et al	03-Dec-02	Schaefer_000
U.S. Patent No. 6,944,185 to Patki et al	13-Sep-05	Patki_185
U.S. Patent No. 7,272,298 to Lang et al	18-Sep-07	Lang_298
U.S. Patent No. 5,909,559 to So	1-Jun-99	So_559
U.S. Patent No. 6,369,855 to Chauvel et al.	9-Apr-02	Chauvel_855
U.S. Patent No. 5,812,976 to Ryan	22-Sep-98	Ryan_976
U.S. Patent No. 5,889,949 to Charles	30-Mar-99	Charles_949
U.S. Patent No. 6,425,054 to Nguyen	23-Jul-02	Nguyen_054
U.S. Patent No. 5,684,804 to Baronetti et al.	04-Nov-97	Baronetti_804
U.S. Patent No. 6,058,459 to Owen et al.	02-May-2000	Owen_459
U.S. Patent No. 5,801,785 to Crump et al.	01-Sep-98	Crump_785

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent No. 5,809,538 to Pollman	15-Sep-98	Pollman_538
U.S. Patent No. 5,598,542 to Leung	28-Jan-97	Leung_542
U.S. Patent No. 6,282,045 to Glover	28-Aug-01	Glover_045
U.S. Patent No. 6,134,638 to Olarig	17-Oct-00	Olarig_638
U.S. Patent Pub. No. 2002/0057892 to Mano	16-May-02	Mano_892
U.S. Patent No. 5,970,220 to Bolash et al.	19-Oct-99	Bolash_220
U.S. Patent No. 5,990,875 to Bi et al.	23-Nov-99	Bi_875
U.S. Patent No. 5,708,819 to Dunnihoo	13-Jan-98	Dunnihoo_819
U.S. Patent No. 6,385,711 to Colligan	07-May-02	Colligan_711
U.S. Patent No. 6,853,385 to MacInnis et al.	08-Feb-05	MacInnis_385
European Patent No. EP 1376449 to Shin et al.	02-Mar-05	Shin_449
European Patent No. EP 0847001 by Cornaby et al.	06-Oct-98	Cornaby_001
European Patent No. EP 0594241 by Thomason et al	06-May-99	Thomason_241
European Patent Application No. EP 0785675 by Yamada et al	23-Jul-97	Yamada_675
European Patent Application No. EP0762756A2 by Sasaki et al	17-Jun-1998	Sasaki_756

## **2. Prior Art Publications**

The following prior art references anticipate and/or render obvious the asserted claims of the '472 patent and describe the state of the art:<sup>15</sup>

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
Purcell	The Mpact 2 VLIW Media Processor Improves Multimedia Performance in PCs	No later than March 1998	Mpact2

<sup>15</sup> As detailed in § II Reservation of Rights, TiVo continues to unreasonably delay and withhold production of many prior art references, invalidity charts, and other portions of prior invalidity contentions, and has yet to produce confidential prior art materials and contentions.

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
Neuman et al.	How to reduce memory in DVD systems	No later than Aug 25, 1997	Neuman
David P. Anderson et al.	A File System for Continuous Media	No later than Nov 1992	Anderson
Kageyama et al.	A Free Time Shift DVD Video Recorder	No later than Aug 1997	Kageyama
Patrick Wai-Ho Chan	A Mobile System for Distributed Multimedia Applications	No later than 1996	Chan
David J. Wetherall	An Interactive Programming System for Media Computation	No later than Sep 1994	Wetherall
Christopher Lindblad	A Programming System for the Dynamic Manipulation of Temporally Sensitive Data	No later than 1994	Lindblad
Cline et al.	DirectShow RTP Support for Adaptivity in Networked Multimedia Applications	No later than Jun 1998	Cline
R. Johnston et al	A Digital Television Sequence Store	No later than May 1978	Johnston
Jonathan Soo	An Architecture for Networked Multimedia	No later than Aug 1995	Soo
Hanna et al.	Demultiplexer IC for MPEG2 Transport Streams	No later than Aug 1995	Hanna
Philipp Ackermann	Developing Object-Oriented Multimedia Software	No later than 1996	Ackermann
Steven Niemczyk	Stream Objects: Dynamically-Segmented Scalable Media Over the Internet	No later than Jun 1996	Niemczyk
Ruihong Wang	Design of a Storage and Retrieval Model for Multimedia Data	No later than 1994	Wang
Thomas Peuker	An Object-Oriented Architecture for the Real-Time Transmission of Multimedia Data Streams	No later than Mar 17, 1997	Peuker



<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
Ramakrishnan et al.	Operating System Support for a Video-On-Demand File Service	No later than Nov 1993	Ramakrishnan
Rangan et al.	Designing File Systems for Digital Video and Audio"	No later than Oct 1991	Rangan
K. Almeroth et al.	On the Use of Multicast Delivery to Provide a Scalable and Interactive Video-On-Demand Service by	No later than Aug 1996	Almeroth Multicast
S. Gibbs et al.	Multimedia Programming: Objects, Environments, and Frameworks	No later than 1995	Gibbs_Multimedia
Patel et al.	Synchronized Continuous Playback through the World Wide Web	No later than 1996	Patel
C. Alexandrou	Multimedia Data Exchange Agent: an Object Behavioral Pattern for Multimedia Programming.	Not later than 1997	Alexandrou
Rowe et al.	MPEG Video in Software: Representation, Transmission, and Playback	No later than 1994	Rowe
K. Almeroth et al.	The Interactive Multimedia Jukebox (IMJ): A New Paradigm for the On-Demand Delivery of Audio/Video	No later than Apr 1998	Almeroth IMJ
Holfelder	MBone VCR - Video Conferencing Recording on the MBone	No later than Apr 1997	Holfelder
Kurioka et al.	Television Home Server for Integrated Services - Toward the Realization of ISDB Anytime Services	No later than Jan 1998	Kurioka
David Clark et al.	Aurora at MIT - Final Report on MIT's Participation in the Aurora Gigabit Testbed	No later than 1995	Clark
Bacher et al.	Content-based Indexing of Captioned Video on the ViewStation	No later than Oct 1995	Bacher

Primary Author or Publisher	Reference Title	Publication / Use Date	Referenced As
J. Adam et al.	Experience with the VuNet - A Network Architecture for a Distributed Multimedia System	No later than 1994	Adam
Anderson et al.	Support for Continuous Media in the Dash System	No later than 1989	Anderson DASH
Owen et al.	An Enhanced DSP Architecture for the Seven Multimedia Functions: The Mpack 2 Media Processor	No later than May 1997	Mpack2
Texas Instruments	TMS320AV7110 Integrated Digital Set-top Box Decoder Functional Specification	No later than July 6, 1998	AV7110
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7110 Integrated Digital Set-top Box Decoder Product Preview</a>	<a href="#">No later than Sep 1997</a>	<a href="#">AV7110 Preview<sup>16</sup></a>
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7100 Integrated Digital Set-top Digital Signal Processor</a>	<a href="#">No later than Oct 1997</a>	<a href="#">AV7100 Preview<sup>17</sup></a>
Demura et al.	A Single-Chip MPEG2 Video Decoder LSI	No later than Feb 1994	Demura
Eric H.J. Persoon	SMASH – a concept for advanced use of storage in the home	No later than Mar 1998	Persoon
Eric Persoon	Set Top Unit with (SMASH) Storage	No later than Dec 4, 1996	SMASH System
Kageyama et al.	A Free Time Shift DVD Video Recorder	No later than Aug 1997	Kageyama
Dutta	Architecture and Design of NX-2700	No later than April 2001	TM-2700
Philips	Nexperia NX-2700	No later than 1999	TM-2700

<sup>16</sup> See [TI-0003066-TI-0003165 \(AV7110 Preview\)](#); [TI-0000001-TI-0016157 \(related materials\)](#).

<sup>17</sup> See [TI-0002936-TI-0002997 \(AV7100 Preview\)](#); [TI-0000001-TI-0016157 \(related materials\)](#).

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
Toshiba	TC81220F MPEG2 Video Audio Decoder, Transport Stream Processor RISC 32-bit MIPS System CPU	No later than 1998	TC81220F
Yoshida	Toshiba Chip Handles DVD	No later than Nov 25, 1996	TC81220F
Electronic News	Toshiba Readies One-Chip Decoder	No later than Nov 18, 1996	TC81220F
PR Newswire	Samsung, Sanyo and Toshiba Select Teralogic's TL750 Processor for Enhanced Digital Set-Top Boxes	No later than Nov 02, 1998	Toshiba
PR Newswire	Toshiba Announces First Microprocessor from TX49 Family	No later than Sep 21, 1998	Toshiba
Selliah Ranthnam et al.	An Architectural Overview of the Programmable Multimedia Processor, TM-1	No later than 1996	TM-1
Selliah Ranthnam et al.	Processing the New World of Interactive Media	No later than March 1998	TM-1
STMicro	Two European IT Prizes Awarded to STMicroelectronics	No later than Nov 26, 1998	STi5500
STMicro	STi5500 Set Top Box/DVD Backend Decoder with Integrated Host Processor Datasheet	No later than Oct 1997	STi5500
Philips	TriMedia TM-1100 Programmable Media Processor	No later than 1998	TM-1100
Sato et al.	A Unified Hybrid Recorder: Combining Hard Disk Drives, Betacam SX, and Analog Betacam	Not later than 1996	Sato
C-Cube Microsystems	AViA-DMX MPEG-2 Transport Demultiplexer AViA-GTX Graphics Transport I/O User's Manual	Not later than 1997	Avia DMX-GTX User Manual
ESS Technology, Inc.	ESS3301 A/V Transport Demultiplexer, Descrambler Product Brief	No later than 1998	ESS Products

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
ESS Technology, Inc.	ESS3308 MPEG2 Audio/Video Decoder Product Brief	No later than 1998	ESS Products
LSI Logic	L64007 MPEG-2, DVB, JSAT Transport Demultiplexer Technical Manual	No later than Jan 16, 1997	LSI Logic Chipset
LSI Logic	L64005 Enhanced MPEG-2 Audio/Video Decoder Technical Manual	No later than May 1998	LSI Logic Chipset
LSI Logic	L64704 Satellite Decoder Technical Manual	No later than May 1997	LSI Logic Chipset
Aaron Hawes	The Design of an IVDS World Wide Web Browser Architecture	No later than Dec 1997	LSI Logic Chipset
Lee et al.	MediaStation 5000: Integrating Video and Audio	No later than 1994	MediaStation5000
Lee et al.	Applying Multimedia to Medical Imaging	No later than Apr 1996	MediaStation5000
Philips	Tri-Media TM-1100 Datasheet	No later than	Philips TM-1 chip
Rathnam et al.	An Architectural Overview of the Programmable Multimedia Processor, TM-1	No later than 1996	Philips TM-1 chip
STMicro	STi5500: Set Top Box Backend Decoder with Integrated Host Processor	No later than Oct 1997	STi5500
Chris Carter	ICs for Next Generation Set-top Boxes	No later than Dec 1997	STi5500
STMicro	SGS-THOMSON Launches STi5500, After Delivering 10 Millionth MPEG Decoder	No later than Apr 21, 1997	STi5500
STMicro	Two European IT Prizes Awarded to STMicroelectronics	No later than Nov 26, 1998	STi5500
STMicro	STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than Oct 1998	STi5510

Primary Author or Publisher	Reference Title	Publication / Use Date	Referenced As
C-Cube	CL9100 Multimode Video Decoder User's Manual	No later than Dec 1994	CL9100
Nguyen et al.	Establish MSP as the Standard for Media Processing	No later than July 25, 1996	Samsung MSP

### 3. Non-Patent/Publication References

Samsung also contends that the asserted claims of the '472 patent are invalid for public use and/or offers for sale of products and services that anticipate the asserted claims of the '472 patent under 35 U.S.C. § 102(b) and/or the purported invention of the asserted claims was made in this country by another inventor who had not abandoned, suppressed, or concealed it under 35 U.S.C. § 102(g). Samsung contends that the following description and events are stated on information and belief, and are supported by the information and documents that will be produced by Samsung, TiVo, and/or third parties.<sup>18</sup> As discovery has only just begun, Samsung continues to investigate these events.

System Name	Use/Knowledge/Offer Date	Primary Publisher/Offeror for Sale
TiVo Series 1	At least as early as March 31, 1999	TiVo
Texas Instruments <a href="#">AV7100 &amp; AV7110</a>	No later than 1996 <i>See, e.g.,</i> AV7110 Specification, <a href="#">AV7110 Preview</a> , <a href="#">AV7100 Preview</a> , Chauvel 855, Gass	Texas Instruments

<sup>18</sup> As detailed in § II Reservation of Rights, TiVo continues to unreasonably delay and withhold production of many prior art references, invalidity charts, and other portions of prior invalidity contentions, and has yet to produce confidential prior art materials and contentions.

<b>System Name</b>	<b>Use/Knowledge/Offer Date</b>	<b>Primary Publisher/Officer for Sale</b>
Loronix CCTVware Enterprise and Loronix CCTVware Solo	At least by 1996	Loronix Information Systems
Replay TV DVR	At least by November 1997  Public Use: At least by January 1999  <i>See, e.g., RTV4000 System</i>	ReplayTV
VuSystem	No later than 1994  <i>See, e.g., VuSystem</i>	MIT / Christopher Lindblad
STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than June 1998  <i>See, e.g., STi5510</i>	STMicroelectronics
ESS Products ( <i>e.g.</i> , ESS3308 MPEG2 Audio/Video Decoder)	No later than 1998  <i>See, e.g., ESS Products</i>	ESS Technology, Inc.
LSI Logic Chipset ( <i>e.g.</i> , L64005 Enhanced MPEG-2 Audio/Video Decoder)	No later than May 1998  <i>See, e.g., LSI Logic Chipset</i>	LSI Logic
MediaStation5000	No later than Dec 1994  <i>See, e.g., MediaStation 5000</i>	Univ of Washington/Texas Instruments
Toshiba TC81220F MPEG2 Video Audio Decoder, Transport Stream Processor RISC 32-bit MIPS System CPU	No later than Mar 1998  <i>See, e.g., Toshiba TC81220F</i>	Toshiba
AViA-DMX MPEG-2 Transport Demultiplexer	No later than Dec 1996	C-Cube Microsystems

<b>System Name</b>	<b>Use/Knowledge/Offer Date</b>	<b>Primary Publisher/Offendor for Sale</b>
AViA-GTX Graphics Transport I/O	<i>See, e.g.,</i> Avia DMX-GTX	
Tri-Media TM-1100	No later than 1996 <i>See, e.g.,</i> Philips TM-1 chip	Philips

#### **4. Asserted Priority Date for the '472 Patent**

In its P.R. 3-1 disclosure, TiVo asserts that “the asserted claims of the '472 Patent are entitled to priority dates of at least as early as, and possibly earlier than, Application No. 09/126,071 [(‘071 Application’)] filed on July 30, 1998,” even though the application for the '472 patent was filed on August 22, 2001, and TiVo did not claim priority to the '071 Application at the time it filed the application for the '472 patent. TiVo has not provided any explanation as to why the '472 patent should be entitled to claim priority to the '071 Application. In response to Samsung’s interrogatory seeking TiVo’s basis for alleging that the asserted claims find support in the written description of the applications to which TiVo alleges the claims are entitled to priority, TiVo objected, stating merely, “[e]very element of each asserted claim of the '472 and '476 patents are supported by the disclosure of the '389 patent.” TiVo’s reliance on the '071 Application as allegedly providing support for the asserted claims of the '472 patent and establishing an earlier priority date for the '472 patent is misplaced and not substantiated.

The asserted claims of the '472 patent are not entitled to the priority date of the '071 Application because the claims recite subject matter not supported by the '071 Application. At least the following exemplary claim elements of the '472 patent’s asserted claims are not supported by the '071 Application:

- “output section including . . . a storage subsystem” (claim 1);
- “decoder subsystem” (claim 1);
- “media manager” (claim 1);
- “host controller” (claim 1);
- “DMA controller” (claim 1);
- “bus arbiter” (claim 1);
- “multimedia data stream processor” (claim 1);
- “decoder/graphics subsystem” (claim 13);
- “decoder/graphics subsystem includes any combination of . . . .” (claim 14);
- “wherein said transport stream interface receives said transport stream from said input section” (claim 15);
- “wherein said transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet streams are stored and played back though [sic] an output side of said transport stream decoder/graphics subsystem” (claim 16)
- “a SDRAM connected to said transport stream decoder/graphics subsystem” (claim 20);
- “wherein said processor is operative to run system software, middleware, and application software” (claim 22);
- “system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components” (claim 23);
- “a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in said media manager” (claim 30); and
- “wherein said second bus element comprises a system bus” (claim 32).



Accordingly, the asserted claims of the '472 patent are not entitled to the priority date of the '071 Application, and the claims are entitled only to the filing date of the application that led to the '472 patent, i.e., August 22, 2001.

**D. Identification of Prior Art Pursuant to P.R. 3-3(a) for the '476 Patent**

**1. Prior Art Patents and Applications**

The following prior art references anticipate and/or render obvious the asserted claims of the '476 patent and describe the state of the art:

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent No. 5,057,932 to Lang	15-Oct-91	Lang_932
U.S. Patent No. 5,126,982 to Yifrach	30-Jun-92	Yifrach_982
U.S. Patent No. 5,132,992 to Yurt et al	21-Jul-92	Yurt_992
U.S. Patent No. 5,164,839 to Lang	17-Nov-92	Lang_839
U.S. Patent No. 5,241,428 to Goldwasser et al	31-Aug-93	Goldwasser_428
U.S. Patent No. 5,329,320 to Yifrach	12-Jul-94	Yifrach_320
U.S. Patent No. 5,371,551 to Logan et al	06-Dec-94	Logan_551
U.S. Patent No. 5,442,390 to Hooper et al	15-Aug-95	Hooper_390
U.S. Patent No. 5,438,423 to Lynch et al	01-Aug-95	Lynch_423
U.S. Patent No. 5,473,744 to Allen et al	05-Dec-95	Allen_744
U.S. Patent No. 5,513,011 to Matsumoto et al.	30-Apr-96	Matsumoto_011
U.S. Patent No. 5,557,724 to Sampat et al.	17-Sep-96	Sampat_724
U.S. Patent No. 5,559,999 to Maturi et al	24-Sep-96	Maturi_999
U.S. Patent No. 5,584,006 to Reber et al	10-Dec-96	Reber_006
U.S. Patent No. 5,614,940 to Cobbley et al	21-Oct-94	Cobbley_940
U.S. Patent No. 5,659,539 to Porter et al	19-Aug-97	Porter_539
U.S. Patent No. 5,696,868 to Kim et al	09-Dec-97	Kim_868
U.S. Patent No. 5,701,383 to Russo et al	23-Dec-97	Russo_383

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent No. 5,719,786 to Nelson et al	17-Feb-98	Nelson_786
U.S. Patent No. 5,721,815 to Ottesen et al	24-Feb-98	Ottesen_815
U.S. Patent No. 5,721,878 to Ottesen et al	24-Feb-98	Ottesen_878
U.S. Patent No. 5,729,280 to Inoue et al	17-Mar-98	Inoue_280
U.S. Patent No. 5,774,186 to Brodsky et al	30-Jun-98	Brodsky_186
U.S. Patent No. 5,815,689 to Shaw et al	4-Oct-98	Shaw_689
U.S. Patent No. 5,822,493 to Uehara et al	13-Oct-98	Uehara_493
U.S. Patent No. 5,898,695 to Fuji et al	27-Apr-99	Fuji_695
U.S. Patent No. 5,930,444 to Camhi et al	27-Jul-99	Camhi_444
U.S. Patent No. 5,949,948 to Krause et al	7-Sep-99	Krause_948
U.S. Patent No. 5,956,716 to Kenner et al	21-Sep-99	Kenner_716
U.S. Patent No. 5,973,679 to Abbott et al	26-Oct-99	Abbot_679
U.S. Patent No. 5,978,855 to Metz et al	2-Nov-99	Metz_855
U.S. Patent No. 5,990,881 to Inoue et al	23-Nov-99	Inoue_881
U.S. Patent No. 5,999,691 to Takagi et al	7-Dec-99	Takagi_691
U.S. Patent No. 6,002,832 to Yoneda	14-Dec-99	Yoneda_832
U.S. Patent No. 6,005,564 to Ahmad et al	21-Dec-99	Ahmad_564
U.S. Patent No. 6,018,612 to Thomason et al	25-Jan-00	Thomason_612
U.S. Patent No. 6,064,792 to Fox et al	16-May-00	Fox_792
U.S. Patent No. 6,081,750 to Hoffberg et al	27-Jun-00	Hoffberg_750
U.S. Patent No. 6,112,226 to Weaver et al	29-Aug-00	Weaver_226
U.S. Patent No. 6,138,221 to Korst et al	24-Oct-00	Korst_221
U.S. Patent No. 6,167,083 to Sporer et al	26-Dec-01	Sporer_083
U.S. Patent No. 6,169,842 to Pijnenburg et al	02-Jan-01	Pijnenburg_842
U.S. Patent No. 6,169,843 to Lenihan et al	02-Jan-01	Lenihan_843
U.S. Patent No. 6,169,844 to Arai	02-Jan-01	Arai_844

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent No. 6,172,712 to Beard et al	09-Jan-01	Beard_712
U.S. Patent No. 6,181,706 to Anderson et al	30-Jan-01	Anderson_706
U.S. Patent No. 6,226,447 to Sasaki et al	01-May-01	Sasaki_447
U.S. Patent No. 6,285,746 to Duran et al	04-Sep-01	Duran_746
U.S. Patent No. 6,209,041 to Shaw et al	27-Mar-01	Shaw_041
U.S. Patent No. 6,304,714 to Krause et al	16-Oct-01	Krause_714
U.S. Patent No. 6,334,022 to Ohba et al	25-Dec-01	Ohba_022
U.S. Patent No. 6,370,323 to Adolph et al	09-Apr-02	Adolph_323
U.S. Patent No. 6,385,386 to Aotake	07-May-02	Aotake_386
U.S. Patent No. 6,445,738 to Zdepski et al	03-Sep-02	Zdepski_738
U.S. Patent No. 6,480,667 to OConnor	12-Nov-02	OConnor_667
U.S. Patent No. 6,490,000 to Schaefer et al	03-Dec-02	Schaefer_000
U.S. Patent No. 6,944,185 to Patki et al	13-Sep-05	Patki_185
U.S. Patent No. 7,272,298 to Lang et al	18-Sep-07	Lang_298
U.S. Patent No. 5,909,559 to So	1-Jun-99	So_559
U.S. Patent No. 6,369,855 to Chauvel et al.	9-Apr-02	Chauvel_855
U.S. Patent No. 5,812,976 to Ryan	22-Sep-98	Ryan_976
U.S. Patent No. 5,889,949 to Charles	30-Mar-99	Charles_949
U.S. Patent No. 6,425,054 to Nguyen	23-Jul-02	Nguyen_054
U.S. Patent No. 5,684,804 to Baronetti et al.	04-Nov-97	Baronetti_804
U.S. Patent No. 6,058,459 to Owen et al.	02-May-2000	Owen_459
U.S. Patent No. 5,801,785 to Crump et al.	01-Sep-98	Crump_785
U.S. Patent No. 5,809,538 to Pollman	15-Sep-98	Pollman_538
U.S. Patent No. 5,598,542 to Leung	28-Jan-97	Leung_542
U.S. Patent No. 6,282,045 to Glover	28-Aug-01	Glover_045
U.S. Patent No. 6,134,638 to Olarig	17-Oct-00	Olarig_638

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent Pub. No. 2002/0057892 to Mano	16-May-02	Mano_892
U.S. Patent No. 5,970,220 to Bolash et al.	19-Oct-99	Bolash_220
U.S. Patent No. 5,990,875 to Bi et al.	23-Nov-99	Bi_875
U.S. Patent No. 5,708,819 to Dunnihoo	13-Jan-98	Dunnihoo_819
U.S. Patent No. 6,385,711 to Colligan	07-May-02	Colligan_711
U.S. Patent No. 6,853,385 to MacInnis et al.	08-Feb-05	MacInnis_385
European Patent No. EP 1376449 to Shin et al.	02-Mar-05	Shin_449
European Patent No. EP 0847001 by Cornaby et al.	06-Oct-98	Cornaby_001
European Patent No. EP 0594241 by Thomason et al	06-May-99	Thomason_241
European Patent Application No. EP 0785675 by Yamada et al	23-Jul-97	Yamada_675
European Patent Application No. EP0762756A2 by Sasaki et al	17-Jun-1998	Sasaki _756

## **2. Prior Art Publications**

The following prior art references anticipate and/or render obvious the asserted claims of the '476 patent and describe the state of the art:<sup>19</sup>

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
Purcell	The Mpact 2 VLIW Media Processor Improves Multimedia Performance in PCs	No later than March 1998	Mpact2
David P. Anderson et al.	A File System for Continuous Media	No later than Nov 1992	Anderson

<sup>19</sup> As detailed in § II Reservation of Rights, TiVo continues to unreasonably delay and withhold production of many prior art references, invalidity charts, and other portions of prior invalidity contentions, and has yet to produce confidential prior art materials and contentions.

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
Kageyama et al.	A Free Time Shift DVD Video Recorder	No later than Aug 1997	Kageyama
Patrick Wai-Ho Chan	A Mobile System for Distributed Multimedia Applications	No later than 1996	Chan
David J. Wetherall	An Interactive Programming System for Media Computation	No later than Sep 1994	Wetherall
Christopher Lindblad	A Programming System for the Dynamic Manipulation of Temporally Sensitive Data	No later than 1994	Lindblad
Cline et al.	DirectShow RTP Support for Adaptivity in Networked Multimedia Applications	No later than Jun 1998	Cline
R. Johnston et al	A Digital Television Sequence Store	No later than May 1978	Johnston
Jonathan Soo	An Architecture for Networked Multimedia	No later than Aug 1995	Soo
Hanna et al.	Demultiplexer IC for MPEG2 Transport Streams	No later than Aug 1995	Hanna
Philipp Ackermann	Developing Object-Oriented Multimedia Software	No later than 1996	Ackermann
Steven Niemczyk	Stream Objects: Dynamically-Segmented Scalable Media Over the Internet	No later than Jun 1996	Niemczyk
Ruihong Wang	Design of a Storage and Retrieval Model for Multimedia Data	No later than 1994	Wang
Thomas Peuker	An Object-Oriented Architecture for the Real-Time Transmission of Multimedia Data Streams	No later than Mar 17, 1997	Peuker
Ramakrishnan et al.	Operating System Support for a Video-On-Demand File Service	No later than Nov 1993	Ramakrishnan
Rangan et al.	Designing File Systems for Digital Video and Audio"	No later than Oct 1991	Rangan

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
K. Almeroth et al.	On the Use of Multicast Delivery to Provide a Scalable and Interactive Video-On-Demand Service by	No later than Aug 1996	Almeroth Multicast
S. Gibbs et al.	Multimedia Programming: Objects, Environments, and Frameworks	No later than 1995	Gibbs_Multimedia
Patel et al.	Synchronized Continuous Playback through the World Wide Web	No later than 1996	Patel
C. Alexandrou	Multimedia Data Exchange Agent: an Object Behavioral Pattern for Multimedia Programming.	Not later than 1997	Alexandrou
Rowe et al.	MPEG Video in Software: Representation, Transmission, and Playback	No later than 1994	Rowe
K. Almeroth et al.	The Interactive Multimedia Jukebox (IMJ): A New Paradigm for the On-Demand Delivery of Audio/Video	No later than Apr 1998	Almeroth IMJ
Holfelder	MBone VCR - Video Conferencing Recording on the MBone	No later than Apr 1997	Holfelder
Kurioka et al.	Television Home Server for Integrated Services - Toward the Realization of ISDB Anytime Services	No later than Jan 1998	Kurioka
David Clark et al.	Aurora at MIT - Final Report on MIT's Participation in the Aurora Gigabit Testbed	No later than 1995	Clark
Bacher et al.	Content-based Indexing of Captioned Video on the ViewStation	No later than Oct 1995	Bacher
J. Adam et al.	Experience with the VuNet - A Network Architecture for a Distributed Multimedia System	No later than 1994	Adam
Anderson et al.	Support for Continuous Media in the Dash System	No later than 1989	Anderson DASH

Primary Author or Publisher	Reference Title	Publication / Use Date	Referenced As
Owen et al.	An Enhanced DSP Architecture for the Seven Multimedia Functions: The Mpact 2 Media Processor	No later than May 1997	Mpact2
Texas Instruments	TMS320AV7110 Integrated Digital Set-top Box Decoder Functional Specification	No later than July 6, 1998	AV7110
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7110 Integrated Digital Set-top Box Decoder Product Preview</a>	<a href="#">No later than Sep 1997</a>	<a href="#">AV7110 Preview<sup>20</sup></a>
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7100 Integrated Digital Set-top Digital Signal Processor</a>	<a href="#">No later than Oct 1997</a>	<a href="#">AV7100 Preview<sup>21</sup></a>
Demura et al.	A Single-Chip MPEG2 Video Decoder LSI	No later than Feb 1994	Demura
Eric H.J. Persoon	SMASH – a concept for advanced use of storage in the home	No later than Mar 1998	Persoon
Eric Persoon	Set Top Unit with (SMASH) Storage	No later than Dec 4, 1996	SMASH System
Kageyama et al.	A Free Time Shift DVD Video Recorder	No later than Aug 1997	Kageyama
Dutta	Architecture and Design of NX-2700	No later than April 2001	TM-2700
Philips	Nexperia NX-2700	No later than 1999	TM-2700
Toshiba	TC81220F MPEG2 Video Audio Decoder, Transport Stream Processor RISC 32-bit MIPS System CPU	No later than 1998	TC81220F

<sup>20</sup> See [TI-0003066-TI-0003165 \(AV7110 Preview\)](#); [TI-0000001-TI-0016157 \(related materials\)](#).

<sup>21</sup> See [TI-0002936-TI-0002997 \(AV7100 Preview\)](#); [TI-0000001-TI-0016157 \(related materials\)](#).

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
Yoshida	Toshiba Chip Handles DVD	No later than Nov 25, 1996	TC81220F
Electronic News	Toshiba Readies One-Chip Decoder	No later than Nov 18, 1996	TC81220F
PR Newswire	Samsung, Sanyo and Toshiba Select Teralogic's TL750 Processor for Enhanced Digital Set-Top Boxes	No later than Nov 02, 1998	Toshiba
PR Newswire	Toshiba Announces First Microprocessor from TX49 Family	No later than Sep 21, 1998	Toshiba
Selliah Ranthnam et al.	An Architectural Overview of the Programmable Multimedia Processor, TM-1	No later than 1996	TM-1
Selliah Ranthnam et al.	Processing the New World of Interactive Media	No later than March 1998	TM-1
STMicro	Two European IT Prizes Awarded to STMicroelectronics	No later than Nov 26, 1998	STi5500
STMicro	STi5500 Set Top Box/DVD Backend Decoder with Integrated Host Processor Datasheet	No later than Oct 1997	STi5500
Philips	TriMedia TM-1100 Programmable Media Processor	No later than 1998	TM-1100
Sato et al.	A Unified Hybrid Recorder: Combining Hard Disk Drives, Betacam SX, and Analog Betacam	Not later than 1996	Sato
C-Cube Microsystems	AViA-DMX MPEG-2 Transport Demultiplexer AViA-GTX Graphics Transport I/O User's Manual	Not later than 1997	Avia DMX-GTX User Manual
ESS Technology, Inc.	ESS3301 A/V Transport Demultiplexer, Descrambler Product Brief	No later than 1998	ESS Products
ESS Technology, Inc.	ESS3308 MPEG2 Audio/Video Decoder Product Brief	No later than 1998	ESS Products



<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
LSI Logic	L64007 MPEG-2, DVB, JSAT Transport Demultiplexer Technical Manual	No later than Jan 16, 1997	LSI Logic Chipset
LSI Logic	L64005 Enhanced MPEG-2 Audio/Video Decoder Technical Manual	No later than May 1998	LSI Logic Chipset
LSI Logic	L64704 Satellite Decoder Technical Manual	No later than May 1997	LSI Logic Chipset
Aaron Hawes	The Design of an IVDS World Wide Web Browser Architecture	No later than Dec 1997	LSI Logic Chipset
Lee et al.	MediaStation 5000: Integrating Video and Audio	No later than 1994	MediaStation5000
Lee et al.	Applying Multimedia to Medical Imaging	No later than Apr 1996	MediaStation5000
Philips	Tri-Media TM-1100 Datasheet	No later than	Philips TM-1 chip
Rathnam et al.	An Architectural Overview of the Programmable Multimedia Processor, TM-1	No later than 1996	Philips TM-1 chip
STMicro	STi5500: Set Top Box Backend Decoder with Integrated Host Processor	No later than Oct 1997	STi5500
Chris Carter	ICs for Next Generation Set-top Boxes	No later than Dec 1997	STi5500
STMicro	SGS-THOMSON Launches STi5500, After Delivering 10 Millionth MPEG Decoder	No later than Apr 21, 1997	STi5500
STMicro	Two European IT Prizes Awarded to STMicroelectronics	No later than Nov 26, 1998	STi5500
STMicro	STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than Oct 1998	STi5510

Primary Author or Publisher	Reference Title	Publication / Use Date	Referenced As
C-Cube	CL9100 Multimode Video Decoder User's Manual	No later than Dec 1994	CL9100
Nguyen et al.	Establish MSP as the Standard for Media Processing	No later than July 25, 1996	Samsung MSP

### 3. Non-Patent/Publication References

Samsung also contends that the asserted claims of the '476 patent are invalid for public use and/or offers for sale of products and services that anticipate the asserted claims of the '476 patent under 35 U.S.C. § 102(b) and/or the purported invention of the asserted claims was made in this country by another inventor who had not abandoned, suppressed, or concealed it under 35 U.S.C. § 102(g). Samsung contends that the following description and events are stated on information and belief, and are supported by the information and documents that will be produced by Samsung, TiVo, and/or third parties.<sup>22</sup> As discovery has only just begun, Samsung continues to investigate these events.

System Name	Use/Knowledge/Offer Date	Primary Publisher/Offeror for Sale
TiVo Series 1	At least as early as March 31, 1999	TiVo
Texas Instruments <a href="#">AV7100 &amp; AV7110</a>	No later than 1996 <i>See, e.g.,</i> <a href="#">AV7110-Specification, AV7110 Preview, AV7100 Preview</a> , Chauvel 855, Gass	Texas Instruments

<sup>22</sup> As detailed in § II Reservation of Rights, TiVo continues to unreasonably delay and withhold production of many prior art references, invalidity charts, and other portions of prior invalidity contentions, and has yet to produce confidential prior art materials and contentions.

<b>System Name</b>	<b>Use/Knowledge/Offer Date</b>	<b>Primary Publisher/Offeror for Sale</b>
Loronix CCTVware Enterprise and Loronix CCTVware Solo	At least by 1996	Loronix Information Systems
Replay TV DVR	At least by November 1997  Public Use: At least by January 1999  <i>See, e.g.,</i> RTV4000 System	ReplayTV
VuSystem	No later than 1994  <i>See, e.g.,</i> VuSystem	MIT / Christopher Lindblad
STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than June 1998  <i>See, e.g.,</i> STi5510	STMicroelectronics
ESS Products ( <i>e.g.,</i> ESS3308 MPEG2 Audio/Video Decoder)	No later than 1998  <i>See, e.g.,</i> ESS Products	ESS Technology, Inc.
LSI Logic Chipset ( <i>e.g.,</i> L64005 Enhanced MPEG-2 Audio/Video Decoder)	No later than May 1998  <i>See, e.g.,</i> LSI Logic Chipset	LSI Logic
MediaStation5000	No later than Dec 1994  <i>See, e.g.,</i> MediaStation 5000	Univ of Washington/Texas Instruments
Toshiba TC81220F MPEG2 Video Audio Decoder, Transport Stream Processor RISC 32-bit MIPS System CPU	No later than Mar 1998  <i>See, e.g.,</i> Toshiba TC81220F	Toshiba
AViA-DMX MPEG-2 Transport Demultiplexer AViA-GTX Graphics Transport I/O	No later than Dec 1996  <i>See, e.g.,</i> Avia DMX-GTX	C-Cube Microsystems

System Name	Use/Knowledge/Offer Date	Primary Publisher/Offeror for Sale
Tri-Media TM-1100	No later than 1996 <i>See, e.g., Philips TM-1 chip</i>	Philips

#### 4. Asserted Priority Date for the '476 Patent

In its P.R. 3-1 disclosure, TiVo asserts that “that the asserted claims of the '476 Patent are entitled to priority dates of at least as early as, and possibly earlier than, Application No. 09/126,071 filed on July 30, 1998,” even though the application for the '476 patent was filed on July 6, 2009 and claims to be a continuation of the application for the '472 patent, filed August 22, 2001. TiVo has not provided any explanation as to why the '476 patent should be entitled to claim priority to the '071 Application. In response to Samsung’s interrogatory seeking TiVo’s basis for alleging that the asserted claims find support in the written description of the applications to which TiVo alleges the claims are entitled to priority, TiVo objected, stating merely, “[e]very element of each asserted claim of the '472 and '476 patents are supported by the disclosure of the '389 patent.” TiVo’s reliance on the '071 Application as allegedly providing support for the asserted claims of the '476 patent and establishing an earlier priority date for the '476 patent is misplaced and is not substantiated.

The asserted claims of the '476 patent are not entitled to the priority date of the '071 Application because the claims recite subject matter not supported by the '071 Application. At least the following exemplary claim elements of the '476 patent’s asserted claims are not supported by the '071 Application:

- “decoder subsystem” (claim 1);

- “host controller” (claim 1);
- “DMA controller” (claim 1);
- “bus arbiter” (claim 1);
- “multimedia data stream processor” (claim 1);
- “decoder/graphics subsystem” (claim 6);
- “decoder/graphics subsystem includes at least one of . . . .” (claim 7);
- “wherein the transport stream interface receives the transport stream from the input section” (claim 8);
- “wherein the transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet streams are stored and played back through an output side of the transport stream decoder/graphics subsystem” (claim 9)
- “a SDRAM connected to the transport stream decoder/graphics subsystem” (claim 10);
- “wherein the processor is operative to run system software, middleware, and application software” (claim 11);
- “a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in the media switch” (claim 13); and
- “system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components” (claim 14).

Accordingly, the asserted claims of the ’476 patent are not entitled to the priority date of the ’071 Application, and the claims are entitled—at best—to the filing date of the application that led to the ’472 patent, i.e., August 22, 2001.

#### **IV. IDENTIFICATION OF PRIOR ART PURSUANT TO P.R. 3-3(B)**

In accordance with P.R. 3-3(b), prior art references anticipating one or more of the asserted claims are listed in the tables below. Each of these prior art patents, publications, and

systems qualifies as prior art under one or more of 35 U.S.C. § 102(a), (b), (e), (f), and/or (g) and anticipates one or more asserted claims as indicated in prior art reference's corresponding P.R. 3-3(c) charts in Appendices A-D, at least based on Plaintiff's apparent claim interpretations and application of the asserted claims to the accused products.

**A. Identification of Anticipatory Prior Art Pursuant to P.R. 3-3(b) for the '389 Patent**

Based on Plaintiff's apparent interpretation of the limitations of the asserted claims of the '389 patent and Plaintiff's application of these claim limitations to the accused products, the following prior art anticipates one or more asserted claims of the '389 patent as indicated in the corresponding P.R. 3-3(c) invalidity charts in Appendix A ("the '389 Anticipatory References"):

<b>Patent</b>	<b>Date of Issue/Publication</b>	<b>Referenced As</b>
U.S. Patent No. 5,557,724 to Sampat et al.	17-Sep-96	Sampat_724
U.S. Patent No. 5,909,559 to So	1-Jun-99	So_559
U.S. Patent No. 6,369,855 to Chauvel et al.	9-Apr-02	Chauvel_855
U.S. Patent No. 5,812,976 to Ryan	22-Sep-98	Ryan_976
U.S. Patent No. 5,913,038 to Griffiths	15-Jun-99	Griffiths_038
U.S. Patent No. 6,169,843 to Lenihan et al	2-Jan-01	Lenihan_843
U.S. Patent No. 5,889,949 to Charles	30-Mar-99	Charles_949
U.S. Patent No. 5,684,804 to Baronetti et al	04-Nov-97	Baronetti_804
U.S. Patent No. 6,425,054 to Nguyen	23-July-02	Nguyen_054
U.S. Patent No. 5,898,695 to Fujii et al	27-Apr-99	Fujii_695
U.S. Patent No. 6,304,714 to Krause et al	16-Oct-01	Krause_714

Primary Author or Publisher	Reference Title	Publication/ Use Date	Referenced As
Jonathan Soo	An Architecture for Networked Multimedia	No later than Aug 1995	Soo
Hanna et al.	Demultiplexer IC for MPEG2 Transport Streams	No later than Aug 1995	Hanna
Texas Instruments	TMS320AV7110 Integrated Digital Set-top Box Decoder Functional Specification	No later than July 6, 1998	AV7110
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7110 Integrated Digital Set-top Box Decoder Product Preview</a>	<a href="#">No later than Sep 1997</a>	<a href="#">AV7110 Preview</a> <sup>23</sup>
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7100 Integrated Digital Set-top Digital Signal Processor</a>	<a href="#">No later than Oct 1997</a>	<a href="#">AV7100 Preview</a> <sup>24</sup>
Bescós et al.	From Multimedia Stream Models to GUI Generation	No later than March 1997	Bescós
Asthana et al.	Kaleido: A System for Dynamic Composition and Processing of Multimedia Flows by	No later than Oct 1995	Kaleido
Wanda Gass	Architecture Trends of MPEG Decoders for Set-Top Box	No later than January 1997	Gass
Steven Niemczyk	Stream Objects: Dynamically-Segmented Scalable Media Over the Internet	No later than Jun 1996	Niemczyk
Coelho et al.	DirectX, RDX, RSX, and MMX Technology	No later than Dec 1997	Coelho
Lars Wolf	Resource Management for Distributed Multimedia Systems	No later than 1996	Wolf

<sup>23</sup> See [TI-0003066-TI-0003165 \(AV7110 Preview\)](#); [TI-0000001-TI-0016157 \(related materials\)](#).

<sup>24</sup> See [TI-0002936-TI-0002997 \(AV7100 Preview\)](#); [TI-0000001-TI-0016157 \(related materials\)](#).

Primary Author or Publisher	Reference Title	Publication/ Use Date	Referenced As
C-Cube Microsystems	AViA-DMX MPEG-2 Transport Demultiplexer AViA-GTX Graphics Transport I/O User's Manual	No later than December 1996	AViA DMX-GTX
STMicro	STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than June 1998	STi5510
Toshiba	TC81220F Datasheet	No later than 1998	Toshiba TC81220F
ESS Technology, Inc.	Ess Chipset	No later than 1998	ESS Products

System Name	Use/Knowledge/Offer Date	Primary Publisher
Texas Instruments <a href="#">AV7100</a> & AV7110	No later than 1996 <i>See, e.g.,</i> AV7110 <a href="#">Specification</a> , <a href="#">AV7110 Preview</a> , <a href="#">AV7100 Preview</a> , Chauvel 855, Gass	Texas Instruments
Microsoft ActiveMovie/DirectShow	No later than 1996 <i>See, e.g.,</i> Coelho, Griffiths, Ennis, Legault, Glass, Chatterjee	Microsoft
STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than June 1998 <i>See, e.g.,</i> STi5510	STMicroelectronics
ESS Products ( <i>e.g.</i> , ESS3308 MPEG2 Audio/Video Decoder)	No later than 1998 <i>See, e.g.,</i> ESS Products	ESS Technology, Inc.
LSI Logic Chipset ( <i>e.g.</i> , L64005 Enhanced MPEG-2 Audio/Video Decoder)	No later than May 1998 <i>See, e.g.,</i> LSI Logic Chipset	LSI Logic
Toshiba TC81220F MPEG2 Video Audio Decoder, Transport Stream Processor	No later than Mar 1998	Toshiba



System Name	Use/Knowledge/Offer Date	Primary Publisher
RISC 32-bit MIPS System CPU	<i>See, e.g.,</i> Toshiba TC81220F	
AViA-DMX MPEG-2 Transport Demultiplexer AViA-GTX Graphics Transport I/O	No later than Dec 1996  <i>See, e.g.,</i> Avia DMX-GTX	C-Cube Microsystems

**B. Identification of Anticipatory Prior Art Pursuant to P.R. 3-3(b) for the '195 Patent**

Based on Plaintiff's apparent interpretation of the limitations of the asserted claims of the '195 patent and Plaintiff's application of these claim limitations to the accused products, the following prior art anticipates one or more asserted claims of the '195 patent as indicated in the corresponding P.R. 3-3(c) invalidity charts in Appendix B ("the '195 Anticipatory References"):

Patent	Date of Issue / Publication	Referenced As
U.S. Patent No. 5,414,455 to Hooper et al	9-May-95	Hooper_455
U.S. Patent No. 5,721,815 to Ottesen et al	24-Feb-98	Ottesen_815
U.S. Patent No. 6,289,172 to Windrem et al	11-Sep-01	Windrem_172
U.S. Patent No. 5,963,202 to Polish	5-Oct-99	Polish_202
U.S. Patent No. 5,774,186 to Brodsky et al	30-Jun-98	Brodsky_186
U.S. Patent No. 6,304,714 to Krause et al	16-Oct-01	Krause_714
U.S. Patent No. 5,438,423 to Lynch et al	1-Aug-95	Lynch_423
U.S. Patent No. 5,371,551 to Logan et al	6-Dec-94	Logan_551
U.S. Patent No. 6,181,706 to Anderson et al	30-Jan-01	Anderson_706
U.S. Patent No. 6,005,599 to Asai et al	21-Dec-99	Asai_599
U.S. Patent No. 6,014,706 to Cannon et al	11-Jan-00	Cannon_706
U.S. Patent No. 5,845,240 to Fielder	1-Dec-98	Fielder_240

<b>Patent</b>	<b>Date of Issue / Publication</b>	<b>Referenced As</b>
U.S. Patent No. 5,898,695 to Fujii et al	27-Apr-99	Fujii_695
U.S. Patent No. 5,241,428 to Goldwasser et al	31-Aug-93	Goldwasser_428
U.S. Patent No. 6,005,600 to Hill	21-Dec-99	Hill_600
U.S. Patent No. 5,442,390 to Hooper et al	15-Aug-95	Hooper_390
U.S. Patent No. 5,729,280 to Inoue et al	17-Mar-98	Inoue_280
U.S. Patent No. 5,706,388 to Isaka	6-Jan-98	Isaka_388
U.S. Patent No. 5,696,868 to Kim et al	9-Dec-97	Kim_868
U.S. Patent No. 5,559,999 to Maturi et al	24-Sep-96	Maturi_999
U.S. Patent No. 5,721,878 to Ottesen et al	24-Feb-98	Ottesen_878
U.S. Patent No. 5,465,120 to Schultheiss	7-Nov-95	Schultheiss_120
U.S. Patent No. 5,999,691 to Takagi et al	7-Dec-99	Takagi_691
European Patent No. EP 0594241 by Thomason et al	06-May-99	Thomason_EP241
U.S. Patent No. 5,822,493 to Uehara et al	13-Oct-98	Uehara_493
U.S. Patent No. 5,329,320 to Yifrach	12-Jul-94	Yifrach_320

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
K. Almeroth et al.	On the Use of Multicast Delivery to Provide a Scalable and Interactive Video-on-Demand Service	No later than Aug 1995	Almeroth
ISO	ISO IEC 11172-1, Information technology - Coding of moving pictures and associated audio for digital storage media at up to about 1.5 Mbits - Part 1	No later than Aug 12, 1993	MPEG-1
ITU-T	ITU-T H.222.0 Generic Coding of Moving Pictures and Associated Audio Information	No later than Nov 1996	MPEG-2
Wu-chi Feng	Buffering Techniques for Delivery of Compressed Video In Video-On-Demand Systems	No later than Sep 30, 1997	Feng

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
Wu-chi Feng	Providing VCR Functionality in a Constant Quality Video-on-Demand Transportation Service	No later than Jun 1996	Feng
Kageyama et al.	A Free Time Shift DVD Video Recorder	No later than August 1997	Kageyama

**C. Identification of Anticipatory Prior Art Pursuant to P.R. 3-3(b) for the '472 Patent**

Based on Plaintiff's apparent interpretation of the limitations of the asserted claims of the '472 patent and Plaintiff's application of these claim limitations to the accused products, the following prior art anticipates one or more asserted claims of the '472 patent as indicated in the corresponding P.R. 3-3(c) invalidity charts in Appendix C ("the '472 Anticipatory References"):

<b>Patent</b>	<b>Date of Issue / Publication</b>	<b>Referenced As</b>
U.S. Patent No. 6,369,855 to Chauvel et al	9-Apr-02	Chauvel_855
U.S. Patent No. 5,909,559 to So	1-Jun-99	So_559
U.S. Patent No. 5,889,949 to Charles	30-Mar-99	Charles_949
U.S. Patent No. 5,684,804 to Baronetti et al	04-Nov-97	Baronetti_804
U.S. Patent No. 6,169,843 to Lenihan et al	2-Jan-01	Lenihan_843
U.S. Patent No. 6,853,385 to MacInnis et al	8-Feb-05	MacInnis_385
U.S. Patent No. 5,898,695 to Fujii et al	27-Apr-99	Fujii_695
U.S. Patent No. 6,425,054 to Nguyen	23-Jul-02	Nguyen_054

<b>Primary Author or Publisher</b>	<b>Reference Title</b>	<b>Publication / Use Date</b>	<b>Referenced As</b>
Texas Instruments	TMS320AV7110 Integrated Digital Set-top Box Decoder Functional Specification	No later than July 6, 1998	AV7110

Primary Author or Publisher	Reference Title	Publication / Use Date	Referenced As
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7110 Integrated Digital Set-top Box Decoder Product Preview</a>	<a href="#">No later than Sep 1997</a>	<a href="#">AV7110 Preview</a> <sup>25</sup>
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7100 Integrated Digital Set-top Digital Signal Processor</a>	<a href="#">No later than Oct 1997</a>	<a href="#">AV7100 Preview</a> <sup>26</sup>
C-Cube Microsystems	AViA-DMX MPEG-2 Transport Demultiplexer AViA-GTX Graphics Transport I/O User's Manual	No later than Dec 1996	AViA DMX-GTX
STMicro	STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than June 1998	STi5510
Toshiba	TC81220F Datasheet	No later than 1998	Toshiba TC81220F
ESS Technology, Inc.	ESS Chipset	No later than 1998	ESS Products
Dutta	Architecture and Design of NX-2700	No later than April 2001	TM-2700
Philips	Nexperia NX-2700	No later than 1999	TM-2700

System Name	Use/Knowledge/Offer Date	Primary Publisher
TiVo Series 1	At least as early as March 31, 1999	TiVo
Texas Instruments <a href="#">AV7100</a> & AV7110	No later than 1996	Texas Instruments

<sup>25</sup> See TI-0003066-TI-0003165 (AV7110 Preview); TI-0000001-TI-0016157 (related materials).

<sup>26</sup> See TI-0002936-TI-0002997 (AV7100 Preview); TI-0000001-TI-0016157 (related materials).

System Name	Use/Knowledge/Offer Date	Primary Publisher
	<i>See, e.g.,</i> AV7110 <del>Specification</del> , <a href="#">AV7110 Preview</a> , <a href="#">AV7100 Preview</a> , Chauvel 855, Gass	
STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than June 1998 <i>See, e.g.,</i> STi5510	STMicroelectronics
ESS Products ( <i>e.g.,</i> ESS3308 MPEG2 Audio/Video Decoder, ESS3301 A/V Transport Demultiplexer, Descrambler)	No later than 1998 <i>See, e.g.,</i> ESS Products	ESS Technology, Inc.
LSI Logic Chipset ( <i>e.g.,</i> L64005 Enhanced MPEG-2 Audio/Video Decoder, L64007 MPEG-2, DVD, JSAT Transport Demultiplexer, L64704 Satellite Decoder Technical Manual)	No later than May 1998 <i>See, e.g.,</i> LSI Logic Chipset	LSI Logic
Toshiba TC81220F MPEG2 Video Audio Decoder, Transport Stream Processor RISC 32-bit MIPS System CPU	No later than Mar 1998 <i>See, e.g.,</i> Toshiba TC81220F	Toshiba
AViA-DMX MPEG-2 Transport Demultiplexer AViA-GTX Graphics Transport I/O	No later than Dec 1996 <i>See, e.g.,</i> Avia DMX-GTX	C-Cube Microsystems

**D. Identification of Anticipatory Prior Art Pursuant to P.R. 3-3(b) for the '476 Patent**

Based on Plaintiff's apparent interpretation of the limitations of the asserted claims of the '476 patent and Plaintiff's application of these claim limitations to the accused products, the

following prior art anticipates one or more asserted claims of the '476 patent as indicated in the corresponding P.R. 3-3(c) invalidity charts in Appendix D ("the '476 Anticipatory References"):

Patent	Date of Issue / Publication	Referenced As
U.S. Patent No. 6,369,855 to Chauvel et al	9-Apr-02	Chauvel_855
U.S. Patent No. 5,909,559 to So	1-Jun-99	So_559
U.S. Patent No. 5,889,949 to Charles	30-Mar-99	Charles_949
U.S. Patent No. 5,684,804 to Baronetti et al	04-Nov-97	Baronetti_804
U.S. Patent No. 6,169,843 to Lenihan et al	2-Jan-01	Lenihan_843
U.S. Patent No. 6,853,385 to MacInnis et al	8-Feb-05	MacInnis_385
U.S. Patent No. 5,898,695 to Fujii et al	27-Apr-99	Fujii_695
U.S. Patent No. 6,425,054 to Nguyen	23-Jul-02	Nguyen_054

Primary Author or Publisher	Reference Title	Publication / Use Date	Referenced As
Texas Instruments	TMS320AV7110 Integrated Digital Set-top Box Decoder Functional Specification	No later than July 6, 1998	AV7110
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7110 Integrated Digital Set-top Box Decoder Product Preview</a>	<a href="#">No later than Sep 1997</a>	<a href="#">AV7110 Preview<sup>27</sup></a>
<a href="#">Texas Instruments</a>	<a href="#">TMS320AV7100 Integrated Digital Set-top Digital Signal Processor</a>	<a href="#">No later than Oct 1997</a>	<a href="#">AV7100 Preview<sup>28</sup></a>
C-Cube Microsystems	AViA-DMX MPEG-2 Transport Demultiplexer AViA-GTX Graphics Transport I/O User's Manual	No later than Dec 1996	AViA DMX-GTX
STMicro	STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than June 1998	STi5510

<sup>27</sup> See [TI-0003066-TI-0003165 \(AV7110 Preview\)](#); [TI-0000001-TI-0016157 \(related materials\)](#).

<sup>28</sup> See [TI-0002936-TI-0002997 \(AV7100 Preview\)](#); [TI-0000001-TI-0016157 \(related materials\)](#).

Primary Author or Publisher	Reference Title	Publication / Use Date	Referenced As
Toshiba	TC81220F Datasheet	No later than 1998	Toshiba TC81220F
ESS Technology, Inc.	ESS Chipset	No later than 1998	ESS Products
Dutta	Architecture and Design of NX-2700	No later than April 2001	TM-2700
Philips	Nexperia NX-2700	No later than 1999	TM-2700

System Name	Use/Knowledge/Offer Date	Primary Publisher
TiVo Series 1	At least as early as March 31, 1999	TiVo
Texas Instruments <a href="#">AV7100</a> & AV7110	No later than 1996 <i>See, e.g.,</i> AV7110 <a href="#">Specification</a> , <a href="#">AV7110 Preview</a> , <a href="#">AV7100 Preview</a> , Chauvel 855, Gass	Texas Instruments
STi5510: Set Top Box Backend Decoder with Integrated Host Processor	No later than June 1998 <i>See, e.g.,</i> STi5510	STMicroelectronics
ESS Products ( <i>e.g.</i> , ESS3308 MPEG2 Audio/Video Decoder, ESS3301 A/V Transport Demultiplexer, Descrambler)	No later than 1998 <i>See, e.g.,</i> ESS Products	ESS Technology, Inc.
LSI Logic Chipset ( <i>e.g.</i> , L64005 Enhanced MPEG-2 Audio/Video Decoder, L64007 MPEG-2, DVD, JSAT Transport Demultiplexer, L64704	No later than May 1998 <i>See, e.g.,</i> LSI Logic Chipset	LSI Logic

System Name	Use/Knowledge/Offer Date	Primary Publisher
Satellite Decoder Technical Manual)		
Toshiba TC81220F MPEG2 Video Audio Decoder, Transport Stream Processor RISC 32-bit MIPS System CPU	No later than Mar 1998 <i>See, e.g.,</i> Toshiba TC81220F	Toshiba
AViA-DMX MPEG-2 Transport Demultiplexer AViA-GTX Graphics Transport I/O	No later than Dec 1996 <i>See, e.g.,</i> Avia DMX-GTX	C-Cube Microsystems

**V. DISCLOSURE OF INVALIDITY DUE TO OBVIOUSNESS PURSUANT TO P.R. 3-3(B) AND (C)**

Subject to the reservation of rights above and based upon TiVo's Complaint, Infringement Contentions, and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered, the references charted and/or identified in these Invalidity Contentions, including the prior art identified pursuant to P.R. 3-3(a) above, at least render obvious the asserted claims in view of the teachings of these references and/or the knowledge of a person of ordinary skill in the art.

To the extent a finder of fact finds that a limitation of a given claim was not disclosed by one of the references charted in these Invalidity Contentions, such claim(s) are nevertheless unpatentable as obvious because the asserted claims contain nothing more than simple and obvious substitution of one known element for another or the mere obvious application of a known technique to a piece of prior art ready for the improvement. To the extent not anticipated,



no asserted claim goes beyond combining known elements to achieve predictable results or does more than choose between clear alternatives known to those of skill in the art.

Moreover, to the extent the foregoing references are found not to anticipate the asserted claims, the foregoing references render the asserted claims obvious either alone, in combination with one or more of the other references identified above, pursuant to P.R. 3-3(a) and (b), or in combination with the knowledge of one of ordinary skill in the art. Samsung is currently unaware of the extent, if any, to which TiVo will contend that limitations of the asserted claims are not disclosed in the art identified by Samsung. Nevertheless, Samsung provides below the following exemplary combinations that render the asserted claims obvious. Further reasons to combine the references disclosed in these contentions include the nature of the problem being solved, the express, implied, and inherent teachings of the prior art, the knowledge of persons of ordinary skill in the art, the fact that the prior art is generally directed toward the same fields of endeavor (*e.g.*, media processing, set-top boxes, multimedia computers, etc.), that such combinations would have yielded predictable results, and that such combinations would have represented known alternatives to a person of ordinary skill in the art. For each TiVo patent-in-suit, Samsung provides below a discussion of exemplary obviousness combinations, categorized by each claim element that TiVo may contend is not disclosed in any individual reference.

**A. '389 Patent**

1. **“a physical data source, wherein said physical data source accepts broadcast data from an input device, parses video and audio data from said broadcast data, and temporarily stores said video and audio data” (claims 31, 61)**

Claims 31 and 61 require “a physical data source, wherein said physical data source accepts broadcast data from an input device, parses video and audio data from said broadcast data, and temporarily stores said video and audio data.” To the extent TiVo contends that a '389

Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Ryan 976
- Gass
- Blatter 478
- Chauvel 855
- AV7110, [AV7110 Preview](#), [AV7100 Preview](#)
- Wolf
- Coelho
- Griffiths 038
- VuSystem
- Soo
- So 559
- Niemczyk
- Sampat 724
- Thomason 612
- Inoue 280
- Lang 839
- Ohba 022
- Kim 868
- Krause 714
- Ottesen 878

- Weaver 226
- Hanna

In addition, to the extent TiVo contends that any of the prior art references for which claim charts have been provided in Appendix A (“Appendix A References”) fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the ’389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing exemplary Secondary References, techniques for parsing MPEG streams from different inputs were well-known in the art by the time of the ’389 patent’s claimed invention. Combining a ’389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the ’389 Anticipatory References, Appendix A References, and exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing), *see, e.g.*, Ryan 976 at 1:6-10 (“The present invention relates generally to data reception, processing and transmission according to the MPEG-2 standards and, more particularly, the present invention relates to the operation and interfacing of a transport decoder which handles an MPEG-2 format datastream.”); Gass at 169 (“The TMS320AV7100 was developed by team of about 50 people in Digital Compression Products at Texas Instruments. The hard work of this group over the last year has made this chip possible.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems

and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards); AV7110 at 7, § 1 (“The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box.”); Wolf at Foreword (“Experts will make use of the book in order to understand the issues in detail. It allows a look into the resource management with an explanation of all it’s why’s, wherefores, and hows. Students and any people interested in multimedia technology will get an inside view into what a multimedia system is and where interesting questions arise. This book may even serve as a basis for an advanced course on multimedia systems.”), 133-42 (citing related prior art by Coulson, IBM, Jeffay, Liu, Tennenhouse, for example); Coelho at XXIII (“Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . . .”); Griffiths 038 at 1:13-16 (“The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams.”); Soo at 4 (“This paper presents an architecture for Networked Multimedia distribution . . . .”); So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”), 2:46-67 (incorporating by reference prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”); Niemczyk at 11 (“The StreamObjects system provides a method of distributing dynamically-segmented, scalable multimedia over the Internet using the convention client/server technologies of the World Wide Web (WWW).”), 12 (citing Soo); Sampat 724 at 1:10-12 (“The present invention relates to computer data processing, and, in particular, to user interfaces and methods for processing multiple data streams on a computer.”); Ottesen 878 at 1:26-29 (“The present invention relates generally to communication systems, and, more particularly, to a system and method for locally controlling multimedia programming received from a remote media-on-demand communication system server.”), and given the design needs,

*e.g.*, the reception of multiple MPEG programs, combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “a physical data source, wherein said physical data source accepts broadcast data from an input device, parses video and audio data from said broadcast data, and temporarily stores said video and audio data” to a '389 Anticipatory Reference or an Appendix A Reference. One of ordinary skill in the art would have been motivated to accept broadcast data and parse audio and video for further processing, and such a combination would have been within that person's skill. As demonstrated in the exemplary Secondary References listed above, “a physical data source, wherein said physical data source accepts broadcast data from an input device, parses video and audio data from said broadcast data, and temporarily stores said video and audio data” was well-known in the art by the time of the '389 patent's claimed invention and thus, adding it to a '389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**2. “a source object, wherein said source object extracts video and audio data from said physical data source” (claims 31, 61)**

Claims 31 and 61 require “a source object, wherein said source object extracts video and audio data from said physical data source.” To the extent TiVo contends that a '389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Coelho

- Griffiths 038 (and related charted references describing the same or similar Microsoft technology including Ennis, Legault, Glass 665, Chatterjee)
- Soo
- Bescós
- Sampat
- Wolf
- Kaleido
- Chauvel 855 (and related charted references describing the same or similar Texas Instruments technology AV7110, [AV7110 Preview](#), [AV7100 Preview](#), Gass, So 559)
- Ackermann
- Lindblad
- Patki 185

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, the source-transform-sink paradigm of multimedia processing was well-known in the art by the time of the '389 patent's claimed invention. In addition, combining a '389 Anticipatory Reference or an Appendix A References with any one of the above Secondary References would have amounted to applying a known technique, *e.g.*,

object-oriented-programming, to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing), *see, e.g.*, Coelho at XXIII (“Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . . .”); Griffiths 038 at 1:13-16 (“The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams.”); Soo at 4 (“This paper presents an architecture for Networked Multimedia distribution . . . .”); Bescós at 136 (“This paper is centered on the description of a model that generalizes multimedia data flows handling including complete behavior and interaction mechanisms, hence allowing full integration of GUIs generation.”); Sampat 724 at 1:10-12 (“The present invention relates to computer data processing, and, in particular, to user interfaces and methods for processing multiple data streams on a computer.”); Wolf at Foreword (“Experts will make use of the book in order to understand the issues in detail. It allows a look into the resource management with an explanation of all it’s why’s, wherefores, and hows. Students and any people interested in multimedia technology will get an inside view into what a multimedia system is and where interesting questions arise. This book may even serve as a basis for an advanced course on multimedia systems.”), 133-42 (citing related prior art by Coulson, IBM, Jeffay, Liu, Tennenhouse, for example); Kaleido at 25 (“Kaleido is an experimental approach to designing . . . an integrated multimedia system. It is an on-going project and in this paper we present the current snap shot of our architecture and implementation.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards); Patki 185 at 1:10-21 (“This invention relates to the field of sending and receiving data packets on a computer network. . . . Computers are often used to process, play back, and display video data, audio data and other data.”), and seek to solve a

similar problem (*e.g.*, efficiently processing multimedia streams) and given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “a source object, wherein said source object extracts video and audio data from said physical data source” to a '389 Anticipatory Reference or an Appendix A Reference. One of ordinary skill in the art would have been motivated to employ this object-oriented-programming concept to improve the function and utility of the same, and such a combination would have been within that person's skill. As demonstrated in the Secondary References listed above, “a source object, wherein said source object extracts video and audio data from said physical data source” was well-known in the art by the time of the '389 patent's claimed invention—including within the context of an object-oriented pipeline for processing multimedia data as disclosed in the Secondary References—and thus, adding it to a '389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**3. “a transform object, wherein said transform object stores and retrieves data streams onto a storage device” (claims 31, 61)**

Claims 31 and 61 require “a transform object, wherein said transform object stores and retrieves data streams onto a storage device.” To the extent TiVo contends that a '389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:



- Coelho
- Griffiths 038 (and related references describing the same or similar Microsoft technology including Ennis, Legault, Glass 665, Chatterjee)
- Soo
- Bescós
- Sampat 724
- Wolf
- Kaleido
- Chauvel 855 (and related references describing the same or similar Texas Instruments technology including AV7110, [AV7110 Preview](#), [AV7100 Preview](#), Gass, So 559)
- Ackermann
- Lindblad
- Patki 185
- Hanna
- Peuker
- Matsumoto 011
- Sato (discussed below)
- Glover 045 (discussed below)
- Colligan 711 (discussed below)
- Mano 892 (discussed below)

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement

Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, (a) the source-transform-sink paradigm of multimedia processing was well-known in the art by the time of the '389 patent's claimed invention as was (b) storing and retrieving such multimedia on a storage device. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing), *see, e.g.*, Coelho at XXIII ("Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . ."); Griffiths 038 at 1:13-16 ("The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams."); Soo at 4 ("This paper presents an architecture for Networked Multimedia distribution . . ."); Bescós at 136 ("This paper is centered on the description of a model that generalizes multimedia data flows handling including complete behavior and interaction mechanisms, hence allowing full integration of GUIs generation."); Sampat 724 at 1:10-12 ("The present invention relates to computer data processing, and, in particular, to user interfaces and methods for processing multiple data streams on a computer."); Wolf at Foreword ("Experts will make use of the book in order to understand the issues in detail. It allows a look into the resource management with an explanation of all it's why's, wherefores, and hows. Students and any people interested in multimedia technology will

get an inside view into what a multimedia system is and where interesting questions arise. This book may even serve as a basis for an advanced course on multimedia systems.”), 133-42 (citing related prior art by Coulson, IBM, Jeffay, Liu, Tennenhouse, for example); Kaleido at 25 (“Kaleido is an experimental approach to designing . . . an integrated multimedia system. It is an on-going project and in this paper we present the current snap shot of our architecture and implementation.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards); Patki 185 at 1:10-21 (“This invention relates to the field of sending and receiving data packets on a computer network. . . . Computers are often used to process, play back, and display video data, audio data and other data.”); Matsumoto 011 at 1:8-12 (“The present invention relates to a method and an apparatus for recording video data with compressed bandwidth, such as video signals and sound signals, on storage media and for reproducing and transmitting the video data in response to subscribers' request.”); Sato at 6 (“The DNW-A100 Hybrid Recorder is equipped with two built-in HDDs which provide 90 minutes of record playback time. This record time can be expanded incrementally up to 6.4 hours by connecting additional HDD storage units to the SCSI-2 port. The internal storage combined with an external RAID 3 level HDD storage array, gives a higher protection of the A/V data which is a significant benefit for on-air application. With this added array, it is also possible to replay fully edited programs while simultaneously recording source material. Simultaneous recording mode and playback is also done with the internal HDD with assembled scenes that have no audio/video split.”), 6 (disclosure under “Simple Edit and Full Edit Modes”), 11 (disclosure under “Live Events with Simultaneous Recording and Editing”); Glover at 5:38-47 (“Server hard disk drive integrated circuit 12 includes a disk control circuitry 24 and a digital signal processor (DSP) 26 that may be implemented using any of a variety of interface circuitry and/or software to allow server hard disk drive 10 to couple to essentially any available network or computer. For example, disk control circuitry 24 and DSP 26 may be implemented to interface hard disk drive integrated

circuit 12 with client 20 through a Universal Serial Bus (USB), a 1394 data transport bus, or any other bus or interface.”), 5:47-6:25; Mano at [0008] (“Video programs are preferably recorded on a mass storage device. Preferably, the mass storage device is a hard disk drive coupled to the television through an IEEE 1394 serial bus network.”), [0009], [0011], [0014] (“The user also has the ability to fast forward and rewind through the already recorded portion of the program while the remainder of the program is recorded. The user can also record one video broadcast while concurrently watching another previously recorded video broadcast. The concurrency of these operations is aided by the IEEE 1394 serial bus network. This bus protocol operates sufficiently fast that both the record and playback operations can occur concurrently . . . .”), [0017], figs. 2-4; Colligan at 3:38-43 (“Types of interfaces for hard disks include SCSI, EIDE and 1394. Data is organized on a hard disk into cylinders, heads and sectors. Modern hard disks have sector sizes that can be changed and no longer have anything to do with the physical geometry of the hard drive.”), and seek to solve a similar problem (*e.g.*, efficiently recording and playing back multimedia streams) and given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “a transform object, wherein said transform object stores and retrieves data streams onto a storage device” to a ’389 Anticipatory Reference or an Appendix A Reference. One of ordinary skill in the art would have been motivated to employ an object-oriented design like the well-known source-transform-sink paradigm (*See, e.g.*, Secondary References) to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “a transform object, wherein said transform object stores and retrieves data streams onto a storage device” was well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389 Anticipatory

Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**4. “said source object obtains a buffer from said transform object, said source object converts video data into data streams and fills said buffer with said streams” (claims 31, 61)**

Claims 31 and 61 require “said source object obtains a buffer from said transform object, said source object converts video data into data streams and fills said buffer with said streams.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Bescós
- Coulson
- Wolf
- Kaleido
- Coelho
- Griffiths 038 (and related references describing the same or similar Microsoft technology including Ennis, Legault, Glass 665, Chatterjee)
- Soo
- Sampat
- Chauvel 855 (and related references describing the same or similar Texas Instruments technology including AV7110, [AV7110 Preview](#), [AV7100 Preview](#), Gass, So 559)
- Jeffay
- Miller
- Gibbs

- Krause 714

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, the transfer of buffers between objects in a source-transform-sink multimedia processing architecture was well-known in the art by the time of the '389 patent's claimed invention. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique, *e.g.*, object-oriented-design, to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing) and address multimedia stream processing techniques including memory handling and management. *See, e.g.*, Bescós at 136 ("This paper is centered on the description of a model that generalizes multimedia data flows handling including complete behavior and interaction mechanisms, hence allowing full integration of GUIs generation."); Sampat 724 at 1:10-12 ("The present invention relates to computer data processing, and, in particular, to user interfaces and methods for processing multiple data streams on a computer."); Wolf at Foreword ("Experts will make use of the book in order to understand the issues in detail. It allows a look into the resource management with an explanation of all it's

why's, wherefores, and hows. Students and any people interested in multimedia technology will get an inside view into what a multimedia system is and where interesting questions arise. This book may even serve as a basis for an advanced course on multimedia systems.”), 133-42 (citing related prior art by Coulson, IBM, Jeffay, Liu, Tennenhouse, for example); Coelho at XXIII (“Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . . .”); Griffiths 038 at 1:13-16 (“The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams.”); Soo at 4 (“This paper presents an architecture for Networked Multimedia distribution . . . .”); Kaleido at 25 (“Kaleido is an experimental approach to designing . . . an integrated multimedia system. It is an on-going project and in this paper we present the current snap shot of our architecture and implementation.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards).

Alternatively, each '389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art for a source object to obtain and fill buffers with portions of a stream in the normal course of processing a multimedia stream. As demonstrated in the Secondary References listed above, “[a] source object [that] obtains a buffer from said transform object [and] converts video data into data streams and fills said buffer with said streams” was well-known in the art by the time of the '389 patent's claimed invention and thus, adding it to a '389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

5. **“source/sink object is automatically flow controlled by said transform object”; “source object obtains a buffer from said transform object”;**

**“sink object obtains data stream buffers from said transform object”**  
**(claims 31, 61)**

Claims 31 and 61 require that the “source object” and “sink object” obtain buffers from and are “automatically flow controlled” by the “transform object.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Parsons (discussed below)
- Rothermel (discussed below)
- Watlington (discussed below)
- Wiser 675
- Ryan 976
- Coelho
- Griffiths 038 (and related references describing the same or similar Microsoft technology including Ennis, Legault, Glass 665, Chatterjee)
- AV7110, [AV7110 Preview](#), [AV7100 Preview](#)
- Chauvel 855
- Gass
- So 559
- Sampat
- Wolf
- Kaleido
- Krause 714
- Miller



- Coulson
- Niemczyk
- Wang
- Peuker

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, "automatic[] flow control[] by said transform object," at least as Plaintiff appears to interpret this and apply it to the accused products, was a well-known technique for processing multimedia with limited resources by the time of the '389 patent's claimed invention. *See, e.g.*, Parsons at 22 ("Pairs of stream handlers implement the transport of data from a source to a target while the synchronization and streaming manager (SSM) provides coordination and central management of data buffers and synchronization data. . . . Figure 3 illustrates the architecture and general operation of the synchronization and streaming manager."); Rothermel at 325 ("The controller communicates with the agents, which are software entities controlling individual streams [including] a sink agent and a source agent, which commonly realize the functionality for starting and stopping the stream, as well as modifying the stream's play-out rate."), 324 (discussing a "buffer-level control mechanism" for preventing "buffer overflow"); Watlington at 221 ("Memory resources are allocated and

automatically deallocated by the resource manager.”). Indeed, Wiser discloses a system where “the data flow is controlled by queue space availability,” and the objects processing the multimedia data “will block until more queue space becomes available.” Wiser at 7:48-63.

In addition, combining a ’389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique, *e.g.*, basic buffer management like what Parsons, Rothermel, Wiser, and the other Secondary References disclose, to a known device ready for improvement to yield predictable results. Furthermore, the ’389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing). *See, e.g.*, Wiser 675 at 1:17-48 (“This invention relates generally to tile secure transfer of digital data, and more particularly, to the transfer of digital data to a local recordable storage medium while securing the transfer against unauthorized copying of the data. . . . For example, rather than purchasing music albums from a local retail outlet, consumers could download the digital data across the Internet and then write this data to their local CD-R, thus creating their own compact disks. Similarly, rather than renting a video tape from a local video retailer, consumers could download the digital version and then play it locally on their computer screens or televisions.”); Coelho at XXIII (“Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . . .”); Griffiths 038 at 1:13-16 (“The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams.”); AV7110 at 7, § 1 (“The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box.”); Niemczyk at 11 (“The StreamObjects system provides a method of distributing dynamically-segmented, scalable multimedia over the Internet using the convention client/server technologies of the World Wide Web (WWW).”), 12 (citing Soo); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more

particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards); Gass at 169 (“The TMS320AV7100 was developed by team of about 50 people in Digital Compression Products at Texas Instruments. The hard work of this group over the last year has made this chip possible.”); So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”), 2:46-67 (incorporating by reference prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”); Sampat 724 at 1:10-12 (“The present invention relates to computer data processing, and, in particular, to user interfaces and methods for processing multiple data streams on a computer.”); Kaleido at 25 (“Kaleido is an experimental approach to designing . . . an integrated multimedia system. It is an on-going project and in this paper we present the current snap shot of our architecture and implementation.”); Wolf at Foreword (“Experts will make use of the book in order to understand the issues in detail. It allows a look into the resource management with an explanation of all it’s why’s, wherefores, and hows. Students and any people interested in multimedia technology will get an inside view into what a multimedia system is and where interesting questions arise. This book may even serve as a basis for an advanced course on multimedia systems.”), 133-42 (citing related prior art by Coulson, IBM, Jeffay, Liu, Tennenhouse, for example); Ryan 976 at 1:6-10 (“The present invention relates generally to data reception, processing and transmission according to the MPEG-2 standards and, more particularly, the present invention relates to the operation and interfacing of a transport decoder which handles an MPEG-2 format datastream.”); Coulson at 1323 (“This paper describes a design for distributed multimedia support in a micro kernel operating system environment which provides the necessary soft real-time support while simultaneously running conventional applications.”). Given the design needs and market pressures, combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to have “automatic flow control” of and provide buffers to the “source object” and “sink object” by the “transform object.” One of ordinary skill in the art would have been motivated to add buffer and flow control by the transform object to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, and to the extent that Samsung can understand Plaintiff’s interpretation and application of these claim limitations, “automatic flow control” was well-known in the art by the time of the '389 patent’s claimed invention and thus, adding it to a '389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**6. “a sink object, wherein said sink object obtains data stream buffers from said transform object and outputs said streams to a video and audio decoder” (claims 31, 61)**

Claims 31 and 61 require “a sink object, wherein said sink object obtains data stream buffers from said transform object and outputs said streams to a video and audio decoder.” To the extent TiVo contends that a '389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Coelho
- Griffiths 038 (and related references describing the same or similar Microsoft technology including Ennis, Legault, Glass 665, Chatterjee)
- Davis (discussed below)
- Coulson

- Soo
- Bescós
- Sampat 724
- Wolf
- Kaleido
- Chauvel 855 (and related references describing the same or similar Texas Instruments technology including AV7110, [AV7110 Preview](#), [AV7100 Preview](#), Gass, So 559)
- Krause 714
- Ackermann
- Lindblad
- Patki 185
- Hanna
- ESS Chipset (discussed below)

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this limitation and application of this limitation to Samsung's products, (a) the transfer of buffers

between objects in a source-transform-sink multimedia processing architecture was well-known in the art by the time of the '389 patent's claimed invention and (b) the transfer of multimedia data ultimately to "a video and audio decoder" was also a known design choice in the art by the time of the '389 patent's claimed invention. *See, e.g.*, ESS Chipset at ESS3301 Brief at fig. 1, ESS3308 Brief at 1 ("The ES3308 can decode MPEG2 video and layer 1 or layer 2 audio simultaneously. For embedded applications, the ES3308's internal RISC processor can be used in place of a microcontroller to provide all system controls and user features."); Davis at 1 ("The VES6000 represents a next-generation MPEG-2 decoder architecture. Previously, MPEG-2 decoder products have integrated separate legacy MPEG audio and MPEG video blocks within the chip, not optimizing the commonality between the two blocks. VLSI determined that some of the more complex audio decoding functions could be overlaid onto the video decoding functions. This unique approach allowed the VES6000 design to 're-use' key complex processing blocks – producing very efficient design.").

In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique, *e.g.*, object-oriented-design, to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing) and address multimedia stream processing techniques. *See, e.g.*, Coelho at XXIII ("Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . ."); Griffiths 038 at 1:13-16 ("The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams."); Soo at 4 ("This paper presents an architecture for Networked Multimedia distribution . . ."); Bescós at 136 ("This paper is centered on the description of a model that generalizes multimedia data flows handling including complete behavior and interaction mechanisms, hence allowing full integration of

GUIs generation.”); Wolf at Foreword (“Experts will make use of the book in order to understand the issues in detail. It allows a look into the resource management with an explanation of all it’s why’s, wherefores, and hows. Students and any people interested in multimedia technology will get an inside view into what a multimedia system is and where interesting questions arise. This book may even serve as a basis for an advanced course on multimedia systems.”), 133-42 (citing related prior art by Coulson, IBM, Jeffay, Liu, Tennenhouse, for example); Kaleido at 25 (“Kaleido is an experimental approach to designing . . . an integrated multimedia system. It is an on-going project and in this paper we present the current snap shot of our architecture and implementation.”); Sampat 724 at 1:10-12 (“The present invention relates to computer data processing, and, in particular, to user interfaces and methods for processing multiple data streams on a computer.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards); Patki 185 at 1:10-21 (“This invention relates to the field of sending and receiving data packets on a computer network. . . . Computers are often used to process, play back, and display video data, audio data and other data.”).

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art for a sink object to obtain buffers and continue moving multimedia data down the pipeline to a decoder including “a video and audio decoder.” One of ordinary skill in the art would have been motivated to add the use of a sink object to obtain buffers and continue moving multimedia data down the pipeline to a decoder including “a video and audio decoder” to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, and to the extent that Samsung can understand TiVo’s interpretation and application of this claim limitation, using a sink object to obtain buffers and continue moving multimedia data down the pipeline to a decoder including “a

video and audio decoder” was well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**7. “converts said streams into display signals and sends said signals to a display” (claims 31, 61)**

Claims 31 and 61 require “convert[ing] said streams into display signals and sends said signals to a display.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- AV7110, [AV7110 Preview](#), [AV7100 Preview](#)
- Chauvel 855
- Gass
- So 559
- Coelho
- Griffiths 038
- Soo
- Sampat 724
- Krause 714

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement



Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this limitation and application of this limitation to Samsung's products, this limitation was well-known in the art by the time of the '389 patent's claimed invention. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, AV7110 at 7, § 1 ("The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box."); Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."), 2:15-30 (referencing MPEG standards); Gass at 169 ("The TMS320AV7100 was developed by team of about 50 people in Digital Compression Products at Texas Instruments. The hard work of this group over the last year has made this chip possible."); Soo at 4 ("This paper presents an architecture for Networked Multimedia distribution . . ."); Coelho at XXIII ("Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . ."); Sampat 724 at 1:10-12 ("The present invention relates to computer data processing, and, in particular, to user interfaces and methods for processing multiple data streams on a computer."); So 559 at 2:15-17 ("This invention generally relates to improved integrated circuits, computer

systems, software products, and processes of operating integrated circuits and computers.”), 2:46-67 (incorporating by reference prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”); Griffiths 038 at 1:13-16 (“The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “[a] decoder [that] converts said streams into display signals and sends said signals to a display” to a ’389 Anticipatory Reference or an Appendix A Reference. One of ordinary skill in the art would have been motivated to add “[a] decoder [that] converts said streams into display signals and sends said signals to a display” to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, and to the extent that Samsung can understand Plaintiff’s interpretation of this claim limitation and application of this claim limitation to the accused products, using a “[a] decoder [that] converts said streams into display signals and sends said signals to a display” was well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**8. “a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system” (claims 31, 61)**

Claims 31 and 61 require a control object that receives commands from a user that control the flow of the broadcast data through the system. To the extent TiVo contends that a

'389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Coelho
- Griffiths 038 (and related references describing the same or similar Microsoft technology including Ennis, Legault, Glass 665, Chatterjee)
- Chauvel 855
- AV7110, [AV7110 Preview](#), [AV7100 Preview](#)
- Bescós
- Sampat 724

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, a control object for receiving commands that control the flow of the broadcast data was well-known in the art by the time of the '389 patent's claimed invention. In addition, combining a '389

Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing), *see, e.g.*, Coelho at XXIII (“Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . . .”); Sampat 724 at 1:10-12 (“The present invention relates to computer data processing, and, in particular, to user interfaces and methods for processing multiple data streams on a computer.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards); Bescós at 136 (“This paper is centered on the description of a model that generalizes multimedia data flows handling including complete behavior and interaction mechanisms, hence allowing full integration of GUIs generation.”); Griffiths 038 at 1:13-16 (“The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams.”); AV7110 at 7, § 1 (“The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box.”), and seek to solve a similar problem (*e.g.*, enabling playback manipulation according to Plaintiff’s apparent interpretation of this limitation). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “a control object, wherein said control object receives commands from a user, said commands

control the flow of the broadcast data through the system” to a ’389 Anticipatory Reference or an Appendix A Reference. One of ordinary skill in the art would have been motivated to add “a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system” to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system” was well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**9. “said control object sends flow command events to said source, transform, and sink objects” (claim 31, 61)**

Claims 31 and 61 require “said control object sends flow command events to said source, transform, and sink objects.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Coelho
- Griffiths 038 (and related references describing the same or similar Microsoft technology including Ennis, Legault, Glass 665, Chatterjee)
- Bescós
- Soo

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures

from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to enable the control object to send command events to each source, transform, and sink object, and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, it was well-known in the art by the time of the '389 patent's claimed invention to use programming mechanisms such as those disclosed in the Secondary References for communication amongst software objects. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing). *See, e.g.*, Coelho at XXIII ("Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . ."); Bescós at 136 ("This paper is centered on the description of a model that generalizes multimedia data flows handling including complete behavior and interaction mechanisms, hence allowing full integration of GUIs generation."); Griffiths 038 at 1:13-16 ("The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams."). Given the design needs and market pressures, combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “[a] control object [that] sends flow command events to said source, transform, and sink objects” to a '389 Anticipatory Reference or an Appendix A Reference. One of ordinary skill in the art would have been motivated to add “[a] control object [that] sends flow command events to said source, transform, and sink objects” to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “[a] control object [that] sends flow command events to said source, transform, and sink objects” was well-known in the art by the time of the '389 patent’s claimed invention and thus, adding it to a '389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**10. “simultaneous storage and play back of multimedia data” (claims 1, 31, 32, 61)**

To the extent that the preamble is limiting, claims 1, 31, 32, and 61 require “simultaneous storage and play back of multimedia data.” To the extent TiVo contends that a '389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- So 559
- Camhi 444
- Lenihan 843
- AV 7110 Specification (and related disclosures in Chauvel 855)
- Nguyen 054

- Logan 551
- Krause 714
- Lang 298
- Sasaki 756
- Ottesen 878
- Goldwasser 428
- Inoue 881
- Camhi 444
- Schaefer 000
- Thomason 612
- Kageyama
- Sato (discussed below)
- Glover 045 (discussed below)
- Colligan 711 (discussed below)
- Mano 892 (discussed below)

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products,



simultaneous storage and playback of multimedia data was well-known in the art by the time of the '389 patent's claimed invention. *See, e.g.*, Kageyama at § 3, 470 ("To better meet the needs of users, the proposed DVD video recorder is designed to enable quick viewing access of desired programs at any time. That is, what we call 'free timeshift viewing'. It frees viewers from restrictions on their viewing times by allowing a program to be played while the recorder continues to record other programs. It allows users to: (a) View reverse playback then fast forward, or to freeze selected frames of a live TV program; (b) Record a TV program on one channel while viewing a second program on another channel.; (c) Record a TV program while viewing a previously recorded program. It also makes it much easier for users to manage, record, view, and locate programs."), 470-72-72; Sato at 6 ("The DNW-A100 Hybrid Recorder is equipped with two built-in HDDs which provide 90 minutes of record playback time. This record time can be expanded incrementally up to 6.4 hours by connecting additional HDD storage units to the SCSI-2 port. The internal storage combined with an external RAID 3 level HDD storage array, gives a higher protection of the A/V data which is a significant benefit for on-air application. With this added array, it is also possible to replay fully edited programs while simultaneously recording source material. Simultaneous recording mode and playback is also done with the internal HDD with assembled scenes that have no audio/video split."), 6 (disclosure under "Simple Edit and Full Edit Modes"), 11 (disclosure under "Live Events with Simultaneous Recording and Editing"); Glover at 5:38-47 ("Server hard disk drive integrated circuit 12 includes a disk control circuitry 24 and a digital signal processor (DSP) 26 that may be implemented using any of a variety of interface circuitry and/or software to allow server hard disk drive 10 to couple to essentially any available network or computer. For example, disk control circuitry 24 and DSP 26 may be implemented to interface hard disk drive integrated circuit 12 with client 20 through a Universal Serial Bus (USB), a 1394 data transport bus, or any other bus or interface."), 5:47-6:25; Mano at [0008] ("Video programs are preferably recorded on a mass storage device. Preferably, the mass storage device is a hard disk drive coupled to the television through an IEEE 1394 serial bus network."), [0009], [0011], [0014] ("The user also

has the ability to fast forward and rewind through the already recorded portion of the program while the remainder of the program is recorded. The user can also record one video broadcast while concurrently watching another previously recorded video broadcast. The concurrency of these operations is aided by the IEEE 1394 serial bus network. This bus protocol operates sufficiently fast that both the record and playback operations can occur concurrently . . . .”), [0017], figs. 2-4; Colligan at 3:38-43 (“Types of interfaces for hard disks include SCSI, EIDE and 1394. Data is organized on a hard disk into cylinders, heads and sectors. Modern hard disks have sector sizes that can be changed and no longer have anything to do with the physical geometry of the hard drive.”).

In addition, combining a ’389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the ’389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”), 2:46-67 (incorporating by reference prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”); AV7110 at 7, § 1 (“The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box.”); Ottesen 878 at 1:26-29 (“The present invention relates generally to communication systems, and, more particularly, to a system and method for locally controlling multimedia programming received from a remote media-on-demand communication system server.”). Given the design needs and market pressures, and combined with a finite

number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add essentially simultaneous storage and playback to a '389 Anticipatory Reference or an Appendix A Reference. One of ordinary skill in the art would have been motivated to add this to improve the function and utility of the same, *e.g.*, storing while viewing, as one non-limiting example based on Plaintiff's apparent interpretation of this limitation, and such a combination would have been within that person's skill. As demonstrated in the Secondary References listed above, "simultaneous storage and play back of multimedia data" was well-known in the art by the time of the '389 patent's claimed invention at least based on Plaintiff's apparent interpretation of this limitation, and, thus, adding it to a '389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**11. "accepting television (TV) broadcast signals, wherein said TV signals are based on a multitude of standards, including, but not limited to, National Television Standards Committee (NTSC) broadcast, PAL broadcast, satellite transmission, DSS, DBS, or ATSC" (claims 1, 32)**

Claims 1 and 32 require "accepting television (TV) broadcast signals . . . ." To the extent TiVo contends that a '389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Blatter 478

- Chauvel 855
- Crump 785
- Baronetti 804
- STi5500
- STi5510
- LSI Integra Chipset
- Fujii 695
- Charles 949
- Thomason 612
- So 559
- Beard 712
- Lang 298
- Lenihan 843
- Lang 932
- Hoffberg 750
- MediaStation 5000
- Ryan '976

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such

a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, the step of accepting TV broadcast signals in a multitude of formats was well-known in the art by the time of the '389 patent's claimed invention. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing, *see, e.g.*, Blatter 478 at 1:10-14 ("This invention is related to the field of digital signal processing, and more particularly to the formation of Program Specific Information used to recover program content and the insertion of the information in digital video data for storage, for example."); So 559 at 2:15-17 ("This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers."), 2:46-67 (incorporating by reference prior art related to software including "Microsoft Corporation: publications" and the Microsoft Windows "Software Development Kit"); Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."), 2:15-30 (referencing MPEG standards); Beard 712 at 1:9-13 ("The present invention relates generally to the field of digitization and storage of an analog video signal and, more particularly, to a television equipped with a mass storage device wherein digitized video input may be stored for later viewing."), and seek to solve a similar problem (*e.g.*, compatibility with multiple TV standards). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add

“accepting television (TV) broadcast signals . . .” to a ’389 Anticipatory Reference or an Appendix A Reference. One of ordinary skill in the art would have been motivated to add the step of accepting TV broadcast signals in a multitude of formats to improve the function and utility of the same, *e.g.*, increasing the number of media standards with which a device is compatible, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “accepting television (TV) broadcast signals . . .” was well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**12. “tuning said TV signals to a specific program” (claims 1, 32)**

Claims 1 and 32 require “tuning said TV signals to a specific program.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Blatter 478
- Chauvel 855
- Thomason 612
- So 559
- Beard 712
- Lang 298
- Lenihan 843
- Lang 932

- Hoffberg 750
- Lenihan 843
- Crump 785
- STi5500
- STi5510
- LSI Integra Chipset
- Fujii 695
- Charles 949 (and corresponding disclosures in AViA DMX-GTX)

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, tuning TV signals to a specific program was well-known in the art by the time of the '389 patent's claimed invention. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing), *see, e.g.*, Blatter 478 at 1:10-14 ("This invention is related to the field of digital signal processing, and more particularly to the formation of Program Specific Information used to recover program content and the insertion of the

information in digital video data for storage, for example.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards); So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”), 2:46-67 (incorporating by reference prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”); Beard 712 at 1:9-13 (“The present invention relates generally to the field of digitization and storage of an analog video signal and, more particularly, to a television equipped with a mass storage device wherein digitized video input may be stored for later viewing.”), and seek to solve a similar problem (*e.g.*, selecting a TV program for viewing). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “tuning said TV signals to a specific program” to a ’389 Anticipatory Reference or an Appendix A Reference. One of ordinary skill in the art would have been motivated to add the step of “tuning said TV signals to a specific program” to improve the function and utility of the same, *e.g.*, permitting a user to select a specific TV program, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “tuning said TV signals to a specific program” was well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.



**13. “at least one Input Section, wherein said Input Section converts said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation” (claims 1, 32)**

Claims 1 and 32 require “at least one Input Section, wherein said Input Section converts said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- So 559
- Blatter 478
- Krause 714
- Lang 298
- STi5510
- STi5500
- Lenihan 843
- Baronetti 804
- Charles 949 (and corresponding disclosures in AViA DMX-GTX)
- Chauvel 855 (and the corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- Ryan 976
- ESS Chipset
- LSI Integra Chipset
- Thomason 612
- Lenihan 843

- Ottesen 878
- Patki 185
- Weaver 226
- Porter 539
- Lynch 423

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, converting a TV program to an MPEG stream was well-known in the art by the time of the '389 patent's claimed invention. Indeed, the MPEG standard had been developed and successfully implemented well before the '389 patent. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing), *see, e.g.*, So 559 at 2:15-17 ("This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers."), 2:46-67 (incorporating by reference prior art related to software including "Microsoft Corporation: publications" and the Microsoft Windows "Software Development Kit"); Blatter 478 at 1:10-14 ("This invention is

related to the field of digital signal processing, and more particularly to the formation of Program Specific Information used to recover program content and the insertion of the information in digital video data for storage, for example.”); Patki 185 at 1:10-21 (“This invention relates to the field of sending and receiving data packets on a computer network. . . . Computers are often used to process, play back, and display video data, audio data and other data.”); Weaver 226 at 1:29-33 (“The present invention relates to a method and apparatus for processing audio-visual information, and more specifically, to a method and apparatus for providing non-sequential access to audio-visual information represented in a live content stream.”); Ottesen 878 at 1:26-29 (“The present invention relates generally to communication systems, and, more particularly, to a system and method for locally controlling multimedia programming received from a remote media-on-demand communication system server.”), and seek to solve a similar problem (*e.g.*, storing and playing back media using limited resources). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to “convert[] said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation” in a ’389 Anticipatory Reference or Appendix A Reference. One of ordinary skill in the art would have been motivated to add the step of “converting said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation” to improve the function and utility of the same, *e.g.*, formatting data according to a well-known standard for internal transfer and manipulation, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “converting said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation” was well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389

Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**14. “a Media Switch, wherein said Media Switch parses said MPEG stream, said MPEG stream is separated into its video and audio components” (claims 1, 32)**

Claims 1 and 32 require a Media Switch that “parses said MPEG stream, said MPEG stream is separated into its video and audio components.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Wilson (discussed below)
- Neuman (discussed below)
- Naimpally 337
- Blatter 478
- Thomason 612
- Inoue 280
- Sampat 724
- Kim 868
- O’Callaghan 263
- Obha 022
- Lang 298
- Lenihan 843
- Ottesen 878
- Patki 185
- Weaver 226

- Porter 539
- Lynch 423
- Niemczyk
- Hanna
- Wang
- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- Lenihan 843
- LSI Integra Chipset
- MacInnis 385
- STi5510
- STi5500
- So 559
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Baronetti 804
- Lenihan 843
- Toshiba TC81220F
- Ryan 976
- Nguyen 054

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. In particular, and to the extent Samsung understands TiVo's apparent interpretation of this limitation and application of this limitation to the accused products, (a) parsing an MPEG stream was well-known in the art by the time of the '389 patent's claimed invention and (b) separating the MPEG stream into its video and audio components was a well-known design choice for processing multimedia data by the time of the '389 patent's claimed invention. *See, e.g.,* Wilson at 7 ("The stream must be error-corrected, depacketized and demultiplexed into its constituent data streams. Then these streams must be sent to their proper receptors, whether they be system commands, MPEG-2 video data or compressed audio data."); Neuman at 84 ("During the parsing process, video and audio streams are separated into header and payload streams and written to independent buffers in DRAM.").

In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor, *e.g.,* media processing. *See, e.g.,* Naimpally 337 at 1:7-11 ("The present invention concerns a system for recording programs that have been encoded according to the MPEG standard defined by the moving-pictures expert group and in particular to a system for recording selected MPEG-2 programs from a multi-program transport stream."); Blatter 478 at 1:10-14 ("This invention is related to the field of digital signal processing, and more particularly to the formation of Program Specific Information used to recover program content and the insertion of the information in digital video data for storage, for example."); Sampat 724 at 1:10-12 ("The present invention relates to computer data processing, and, in particular, to user interfaces and methods for processing multiple data streams on a computer."); Ottesen 878 at 1:26-29 ("The present invention relates generally to

communication systems, and, more particularly, to a system and method for locally controlling multimedia programming received from a remote media-on-demand communication system server.”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”); Weaver 226 at 1:29-33 (“The present invention relates to a method and apparatus for processing audio-visual information, and more specifically, to a method and apparatus for providing non-sequential access to audio-visual information represented in a live content stream.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, (a) parsing an MPEG stream was already well-known and (b) it would have been obvious in view of the finite choices for processing an MPEG stream to elect to separate the MPEG stream “into its video and audio components.” This would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. As demonstrated in the Secondary References listed above, parsing an MPEG stream was well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**15. “storing said video and audio components on a storage device”;  
“extracts said video and audio components from said storage device”  
(claims 1, 32)**

Claims 1 and 32 require storing and extracting “video and audio components” on/from a storage device. To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose

these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Maturi 999
- Brodsky 186
- Matsumoto 011
- Thomason 612
- Lang 839
- Inoue 280
- Sampat 724
- Blatter 478
- Naimpally 337
- Kim 868
- Obha 022
- Lang 298
- Lenihan 843
- Ottesen 878
- Patki 185
- Weaver 226
- Porter 539
- Lynch 423
- So 559
- Lenihan 843
- AV 7110 Specification (and related disclosures in Chauvel 855)
- Nguyen 054



- Logan 551
- Kageyama
- Sato (discussed below)
- Glover 045 (discussed below)
- Colligan 711 (discussed below)
- Mano 892 (discussed below)

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, separating the MPEG stream into its video and audio components and then using a storage device to store and extract these components was a well-known design choice for processing and recording multimedia data by the time of the '389 patent's claimed invention. *See, e.g.*, Sato at 6 ("The DNW-A100 Hybrid Recorder is equipped with two built-in HDDs which provide 90 minutes of record playback time. This record time can be expanded incrementally up to 6.4 hours by connecting additional HDD storage units to the SCSI-2 port. The internal storage combined with an external RAID 3 level HDD storage array, gives a higher protection of the A/V data which is a significant benefit for on-air application. With this added array, it is also possible to replay fully edited programs while simultaneously recording source material. Simultaneous recording mode and playback is also done with the internal HDD with assembled scenes that have no audio/video split."), 6 (disclosure under

“Simple Edit and Full Edit Modes”), 11 (disclosure under “Live Events with Simultaneous Recording and Editing”); Glover at 5:38-47 (“Server hard disk drive integrated circuit 12 includes a disk control circuitry 24 and a digital signal processor (DSP) 26 that may be implemented using any of a variety of interface circuitry and/or software to allow server hard disk drive 10 to couple to essentially any available network or computer. For example, disk control circuitry 24 and DSP 26 may be implemented to interface hard disk drive integrated circuit 12 with client 20 through a Universal Serial Bus (USB), a 1394 data transport bus, or any other bus or interface.”), 5:47-6:25; Mano at [0008] (“Video programs are preferably recorded on a mass storage device. Preferably, the mass storage device is a hard disk drive coupled to the television through an IEEE 1394 serial bus network.”), [0009], [0011], [0014] (“The user also has the ability to fast forward and rewind through the already recorded portion of the program while the remainder of the program is recorded. The user can also record one video broadcast while concurrently watching another previously recorded video broadcast. The concurrency of these operations is aided by the IEEE 1394 serial bus network. This bus protocol operates sufficiently fast that both the record and playback operations can occur concurrently . . . .”), [0017], figs. 2-4; Colligan at 3:38-43 (“Types of interfaces for hard disks include SCSI, EIDE and 1394. Data is organized on a hard disk into cylinders, heads and sectors. Modern hard disks have sector sizes that can be changed and no longer have anything to do with the physical geometry of the hard drive.”). In addition, combining a ’389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the ’389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Maturi 999 at 1:9-12 (“The present invention generally relates to the art of audio/video data compression and transmission, and more specifically to a synchronization system for a Motion Picture Experts Group (MPEG) audio/video decoder.”); Brodsky 186 at 1:8-11 (“The present invention is directed to the field of video, monitoring, storage and playback. It

is more particularly directed to concurrent storage of a video signal being received and display of a previously stored signal.”); Matsumoto 011 at 1:8-12 (“The present invention relates to a method and an apparatus for recording video data with compressed bandwidth, such as video signals and sound signals, on storage media and for reproducing and transmitting the video data in response to subscribers' request.”); Sampat 724 at 1:10-12 (“The present invention relates to computer data processing, and, in particular, to user interfaces and methods for processing multiple data streams on a computer.”); Blatter 478 at 1:10-14 (“This invention is related to the field of digital signal processing, and more particularly to the formation of Program Specific Information used to recover program content and the insertion of the information in digital video data for storage, for example.”); Naimpally 337 at 1:7-11 (“The present invention concerns a system for recording programs that have been encoded according to the MPEG standard defined by the moving-pictures expert group and in particular to a system for recording selected MPEG-2 programs from a multi-program transport stream.”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”); Lynch 423 at 1:8-11 (“The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in view of the finite, known techniques for processing an MPEG stream to elect to separate the MPEG stream “into its video and audio components” and use a storage device to store and extract these components. One of ordinary skill in the art would have been motivated to add the step of separating the MPEG stream “into its video and

audio components” and using a storage device to store and extract these components to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, separating the MPEG stream “into its video and audio components” and using a storage device to store and extract these components was well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

16. **“said Output Section assembles said video and audio components into an MPEG stream”; “said Output Section sends said MPEG stream to a decoder”; “said decoder converts said MPEG stream into TV output signals”; “said decoder delivers said TV output signals to a TV receiver” (claims 1, 32)**

Claims 1 and 32 require assembling “said video and audio components into an MPEG stream” and sending “said MPEG stream to a decoder.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Thomason 612
- Maturi 999
- Krause 714
- Lang 839
- Inoue 280
- Sampat 724
- Brodsky 186
- Matsumoto 011

- Kim 868
- Obha 022
- Lang 298
- Lenihan 843
- Ottesen 878
- Patki 185
- Weaver 226
- Porter 539
- Lynch 423
- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#),  
[AV7100 Preview](#))
- STi5510
- ESS Chipset
- LSI Integra Chipset
- Owen 459
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Lenihan 843

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the

above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, separating the MPEG stream into its video and audio components for storage and then re-assembling them for sending to a decoder for TV output was a well-known design choice for processing and playback of multimedia by the time of the '389 patent's claimed invention. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Brodsky 186 at 1:8-11 ("The present invention is directed to the field of video, monitoring, storage and playback. It is more particularly directed to concurrent storage of a video signal being received and display of a previously stored signal."); Maturi 999 at 1:9-12 ("The present invention generally relates to the art of audio/video data compression and transmission, and more specifically to a synchronization system for a Motion Picture Experts Group (MPEG) audio/video decoder."); Matsumoto 011 at 1:8-12 ("The present invention relates to a method and an apparatus for recording video data with compressed bandwidth, such as video signals and sound signals, on storage media and for reproducing and transmitting the video data in response to subscribers' request."); Sampat 724 at 1:10-12 ("The present invention relates to computer data processing, and, in particular, to user interfaces and methods for processing multiple data streams on a computer."); Lenihan 843 at 1:8-13 ("The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs."); Lynch 423 at 1:8-11 ("The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals."). Given the design needs and market pressures, and

combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious as an ordinary design choice to elect to separate the MPEG stream “into its video and audio components” and then re-assemble them for sending to a decoder. One of ordinary skill in the art would have been motivated to add the step of separating the MPEG stream into its video and audio components for storage and then re-assembling them for sending to a decoder for TV output to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, separating the MPEG stream into its video and audio components for storage and then re-assembling them for sending to a decoder for TV output was well-known in the art by the time of the '389 patent’s claimed invention and, thus, adding it to a '389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**17. “accepting control commands from a user, wherein said control commands are sent through the system and affect the flow of said MPEG stream” (claims 1, 32)**

Claims 1 and 32 require “accepting control commands from a user, wherein said control commands are sent through the system and affect the flow of said MPEG stream.” To the extent TiVo contends that a '389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Bescós (discussed below)

- Coelho (discussed below)
- Griffiths 038 (discussed below)
- Thomason 612
- Thomason 241
- Maturi 999
- Krause 714
- Inoue 280
- Sampat 724
- Blatter 478
- Adolph 323
- Brodsky 186
- Matsumoto 011
- O'Callaghan 263
- Obha 022
- Lang 298
- Ottesen 878
- Weaver 226
- Lynch 423

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the



above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, it was well-known in the art by the time of the '389 patent's claimed invention to accept control commands from a user in order to affect the flow of an MPEG stream. *See, e.g.*, Bescós at 144 ("Fig. 6 shows a video viewer, one of the applications developed using the presented stream model. It shows several GUI streams [that] are used to call the flow control functions of a video streams. The single multimedia stream (the application itself) is composed of: . . . Nine multi-state button streams (also derived from an animation stream). Six (the centered ones) display multi-image push buttons to control the video sequence playback. They have default behavior (their own Play function is called when the user clicks on them), and an active status, triggered by the mouse click, whose action targets the video stream and specifies the graphically described operation. The three remaining (the left ones marked with +,0,-) control parameters of the video sequence (audio and video distance)."); Coelho at 111 ("At the high level, ActiveX, you only need to embed the ActiveX control in your application, and ActiveX control will handle the rest. It opens the media file, builds the filter graph, and even provides the user interface for controlling the filter graph (Run, Stop, Pause, and so forth)."), fig. 9-6 ("ActiveX control default user interface components"); Griffiths 038 at 10:24-30 ("The filter graph manager 202 can control the media stream by allowing the application program 37A or OLE control 206 to specify certain activities, such as starting, pausing, or stopping the media stream, playing for a particular duration or seeking to a particular point in the data stream. The filter graph manager 202 then calls appropriate methods on the filters to invoke them."), 8:30-33 ("A user may enter commands and information into the personal computer 20 through a keyboard 40 and an input or pointing device, such as a mouse 42."). In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the

same field of endeavor, *e.g.*, media processing. *See, e.g.*, Bescós at 136 (“This paper is centered on the description of a model that generalizes multimedia data flows handling including complete behavior and interaction mechanisms, hence allowing full integration of GUIs generation.”); Griffiths 038 at 1:13-16 (“The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams.”); Coelho at XXIII (“Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . . .”); Blatter 478 at 1:10-14 (“This invention is related to the field of digital signal processing, and more particularly to the formation of Program Specific Information used to recover program content and the insertion of the information in digital video data for storage, for example.”); Maturi 999 at 1:9-12 (“The present invention generally relates to the art of audio/video data compression and transmission, and more specifically to a synchronization system for a Motion Picture Experts Group (MPEG) audio/video decoder.”); Lynch 423 at 1:8-11 (“The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to accept “control commands” so as to allow a user to affect the flow of an MPEG stream. One of ordinary skill in the art would have been motivated to implement “control commands” and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, this was well-known in the art by the time of the ’389 patent’s claimed invention and, thus, adding it to a ’389 Anticipatory Reference or an Appendix A Reference

would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**18. “said Input Section directs said MPEG stream to the destination indicated by said control commands” (claims 2, 33); “said Output Section extracts said video and audio components from the storage device indicated by said control commands” (claims 3, 34)**

Claims 2/33 require “said Input Section directs said MPEG stream to the destination indicated by said control commands” and claims 3/34 require “said Output Section extracts said video and audio components from the storage device indicated by said control commands.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Thomason 612
- Thomason 241
- So 559
- Blatter 478
- Krause 714
- Krause 948
- Lang 298
- Lenihan 843
- Ottesen 878
- Weaver 226
- Porter 539
- Lynch 423
- Maturi 999

- STi5500
- Lenihan 843
- Baronetti 804
- Charles 949 (and corresponding disclosures in AViA DMX-GTX)
- Chauvel 855 (and the corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- Ryan 976
- ESS Chipset
- LSI Integra Chipset
- MediaStation 5000
- Fujii 695

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, it was well-known in the art by the time of the '389 patent's claimed invention at least to design systems that are responsive to control commands. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary

References are in the same field of endeavor (*e.g.*, media processing). *See, e.g.*, So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”), 2:46-67 (incorporating by reference prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”); Blatter 478 at 1:10-14 (“This invention is related to the field of digital signal processing, and more particularly to the formation of Program Specific Information used to recover program content and the insertion of the information in digital video data for storage, for example.”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”); Ottesen 878 at 1:26-29 (“The present invention relates generally to communication systems, and, more particularly, to a system and method for locally controlling multimedia programming received from a remote media-on-demand communication system server.”); Lynch 423 at 1:8-11 (“The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references. Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art, as demonstrated in the Secondary References, for example.

**19. “storing and extracting of said video and audio components from said storage device are performed simultaneously” (claims 5, 36)**

Claims 5 and 36 require “storing and extracting of said video and audio components from said storage device are performed simultaneously.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with

the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- So 559
- Lenihan 843
- AV 7110 Specification (and related disclosures in Chauvel 855)
- Nguyen ’054
- Logan 551
- Krause 714
- Lang 298
- European Patent No. 0762756 to Sasaki et al.
- Ottesen 878
- Goldwasser 428
- Inoue 881
- Camhi 444
- Schaefer 000
- Thomason 612
- Sato (discussed below)
- Glover 045 (discussed below)
- Colligan 711 (discussed below)
- Mano 892 (discussed below)

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement

Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitations and application of this claim limitations to the accused products, simultaneous storage and extraction of video and audio components were well-known in the art by the time of the '389 patent's claimed invention. *See, e.g.*, Kageyama at § 3, 470 ("To better meet the needs of users, the proposed DVD video recorder is designed to enable quick viewing access of desired programs at any time. That is, what we call 'free timeshift viewing'. It frees viewers from restrictions on their viewing times by allowing a program to be played while the recorder continues to record other programs It allows users to: (a) View reverse playback then fast forward, or to freeze selected frames of a live TV program; (b) Record a TV program on one channel while viewing a second program on another channel.; (c) Record a TV program while viewing a previously recorded program. It also makes it much easier for users to manage, record, view, and locate programs."), 470-72-72; Sato at 6 ("The DNW-A100 Hybrid Recorder is equipped with two built-in HDDs which provide 90 minutes of record playback time. This record time can be expanded incrementally up to 6.4 hours by connecting additional HDD storage units to the SCSI-2 port. The internal storage combined with an external RAID 3 level HDD storage array, gives a higher protection of the A/V data which is a significant benefit for on-air application. With this added array, it is also possible to replay fully edited programs while simultaneously recording source material. Simultaneous recording mode and playback is also done with the internal HDD with assembled scenes that have no audio/video split."), 6 (disclosure under "Simple Edit and Full Edit Modes"), 11 (disclosure under "Live Events with Simultaneous Recording and Editing"); Glover at 5:38-47 ("Server hard disk drive integrated

circuit 12 includes a disk control circuitry 24 and a digital signal processor (DSP) 26 that may be implemented using any of a variety of interface circuitry and/or software to allow server hard disk drive 10 to couple to essentially any available network or computer. For example, disk control circuitry 24 and DSP 26 may be implemented to interface hard disk drive integrated circuit 12 with client 20 through a Universal Serial Bus (USB), a 1394 data transport bus, or any other bus or interface.”), 5:47-6:25; Mano at [0008] (“Video programs are preferably recorded on a mass storage device. Preferably, the mass storage device is a hard disk drive coupled to the television through an IEEE 1394 serial bus network.”), [0009], [0011], [0014] (“The user also has the ability to fast forward and rewind through the already recorded portion of the program while the remainder of the program is recorded. The user can also record one video broadcast while concurrently watching another previously recorded video broadcast. The concurrency of these operations is aided by the IEEE 1394 serial bus network. This bus protocol operates sufficiently fast that both the record and playback operations can occur concurrently . . . .”), [0017], figs. 2-4; Colligan at 3:38-43 (“Types of interfaces for hard disks include SCSI, EIDE and 1394. Data is organized on a hard disk into cylinders, heads and sectors. Modern hard disks have sector sizes that can be changed and no longer have anything to do with the physical geometry of the hard drive.”).

In addition, combining a ’389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the ’389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”), 2:46-67 (incorporating by reference prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically



organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”); AV7110 at 7, § 1 (“The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box.”); Ottesen 878 at 1:26-29 (“The present invention relates generally to communication systems, and, more particularly, to a system and method for locally controlling multimedia programming received from a remote media-on-demand communication system server.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of this claim limitation and application of this limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add simultaneous storage and extraction of video and audio components to a ’389 Anticipatory Reference or an Appendix A Reference. One of ordinary skill in the art would have been motivated to add simultaneous storage and extraction of video and audio components to improve the function and utility of the same, *e.g.*, storing while viewing, as one non-limiting example based on Plaintiff’s apparent interpretation of these limitations, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, these concepts were well-known in the art by the time of the ’389 patent’s claimed invention at least based on Plaintiff’s apparent interpretation of this limitation, and, thus, adding it to a ’389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**20. “said Media Switch calculates and logically associates a time stamp to said video and audio components” (claims 6, 37); “said Media Switch extracts time stamp values from a digital TV stream and logically associates said time stamp values to said video and audio components” (claims 7, 38)**

Claims 6/37 require “said Media Switch calculates and logically associates a time stamp to said video and audio components” and claims 7/38 require “said Media Switch extracts time stamp values from a digital TV stream and logically associates said time stamp values to said video and audio components.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Krause 714
- Lang 298
- Sasaki 756
- Ottesen 878
- Goldwasser 428
- Logan 551
- Inoue 881
- Camhi 444
- Schaefer 000
- Lenihan 843
- Lynch 423
- Brodsky 186
- Thomason 612

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, at least extracting and/or associating timestamps with multimedia streams was well-known in the art by the time of the '389 patent's claimed invention. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Ottesen 878 at 1:26-29 ("The present invention relates generally to communication systems, and, more particularly, to a system and method for locally controlling multimedia programming received from a remote media-on-demand communication system server."); Lenihan 843 at 1:8-13 ("The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs."); Lang 298 1:7-9 ("This invention is related to the field of broadcast television in all it's forms. This includes but is not limited to over-the-air broadcast, cable TV, and satellite TV."); Camhi 444 at 1:12-16 ("The present invention relates to information and entertainment systems, and more particularly, to a keyboard and memory

equipped interface apparatus for the storage and processing of signals associated with such information and entertainment systems.”); Sasaki 756 at [001] (“The present invention relates to a video signal recording and reproducing apparatus which can simultaneously record and reproduce a video by using a disk apparatus.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders these elements obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art at least to add extracting and/or associating timestamps with multimedia streams to a ’389 Anticipatory Reference or an Appendix A Reference, as demonstrated in the Secondary References, for example.

**21. “increasing the decoder system clock rate for fast playback or fast reverse playback” (claims 12, 43); “decreasing the decoder system clock rate for slow playback or slow reverse playback” (claims 13, 44)**

Claims 12/43 and 13/44 require increasing or decreasing the decoder system clock rate for affecting playback. To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Krause 714
- Lang 298
- Sasaki 756
- Adolph 323
- Ottesen 878

- Goldwasser 428
- Logan 551
- Inoue 881
- Camhi 444
- Inoue 280
- Sampat 724
- Lynch 423
- Brodsky 186
- Thomason 612

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, it was well-known in the art by the time of the '389 patent's claimed invention that playback can be affected by increasing or decreasing the decoder system clock rate. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Inoue 280 at 1:7-8 ("This invention relates to a video signal receiver for a near video-on-

demand broadcast system.”); Ottesen 878 at 1:26-29 (“The present invention relates generally to communication systems, and, more particularly, to a system and method for locally controlling multimedia programming received from a remote media-on-demand communication system server.”); Camhi 444 at 1:12-16 (“The present invention relates to information and entertainment systems, and more particularly, to a keyboard and memory equipped interface apparatus for the storage and processing of signals associated with such information and entertainment systems.”); Lynch 423 at 1:8-11 (“The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals.”); Sasaki 756 at [001] (“The present invention relates to a video signal recording and reproducing apparatus which can simultaneously record and reproduce a video by using a disk apparatus.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in view of known techniques in the art to affect playback by increasing or decreasing the decoder system clock rate. One of ordinary skill in the art would have been motivated to add “increasing the decoder system clock rate for fast playback or fast reverse playback” or “decreasing the decoder system clock rate for slow playback or slow reverse playback” as one option for improving the function and utility of the same, *e.g.*, effecting fast or slow playback, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, these limitations were well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

22. **“said Media Switch has a data bus connecting it to a CPU and DRAM” (claims 18, 49); “said Media Switch shares an address bus with a CPU and DRAM” (claims 19, 50); “said storage device is**

**connected to said Media Switch” (claims 21, 52); “said Media Switch is implemented in hardware” (claim 23)**

Claims 18/49 and 49/50 require a shared data bus and address bus between certain components, claims 21/52 similarly require a connection between certain components, and claim 23 requires one of these components to be hardware. To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- AV7110, [AV7110 Preview](#), [AV7100 Preview](#) (and corresponding disclosures in Chauvel [855](#))
- Lang 298
- Krause 714
- So 559
- Chauvel 855
- Sasaki 756
- Ottesen 878
- Goldwasser 428
- Logan 551
- Inoue 881
- Camhi 444
- Schaefer 000
- Thomason 612
- Baronetti 804
- LSI Integra Chipset
- Lenihan 843

- Nguyen 054
- Owen 459
- Toshiba TC81220F

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, it was well-known in the art by the time of the '389 patent's claimed invention that components could be connected together, *e.g.*, by using a data bus and/or address bus. In addition, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing), *see, e.g.*, AV7110 at 7, § 1 ("The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box."); Lang 298 1:7-9 ("This invention is related to the field of broadcast television in all it's forms. This includes but is not limited to over-the-air broadcast, cable TV, and satellite TV."); So 559 at 2:15-17 ("This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers."), 2:46-67 (incorporating by reference



prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards); Ottesen 878 at 1:26-29 (“The present invention relates generally to communication systems, and, more particularly, to a system and method for locally controlling multimedia programming received from a remote media-on-demand communication system server.”); Camhi 444 at 1:12-16 (“The present invention relates to information and entertainment systems, and more particularly, to a keyboard and memory equipped interface apparatus for the storage and processing of signals associated with such information and entertainment systems.”), and seek to solve a similar problem (*e.g.*, communications between hardware components) and given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in view of known techniques in the art to use a data bus and/or address bus to connect these components. One of ordinary skill in the art would have been motivated to connect these components via a data bus and/or address bus as one option for improving the function and utility of the same, *e.g.*, facilitating communications between hardware components, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, to use a data bus and/or address bus to connect these components was well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389 Anticipatory Reference or an Appendix A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results

**23. “said Media Switch operates asynchronously [sic]and autonomously with a CPU” (claims 20, 51)**

Claims 20 and 51 require “said Media Switch operates asynchronously [sic]and autonomously with a CPU.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- LSI Integra Chipset
- Fujii 695
- STi5510
- So 559
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Baronetti 804
- Lenihan 843
- Toshiba TC81220F
- Nguyen 054
- Krause 714
- Lang 298
- Sasaki 756
- Ottesen 878
- Goldwasser 428
- STi5510
- Lenihan 843

- LSI Integra Chipset
- Ryan 976

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this limitation to the accused products, a media switch operating asynchronously and autonomously with a CPU was well-known in the art by the time of the '389 patent's claimed invention. Thus, combining a '389 Anticipatory Reference or an Appendix A Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."), 2:15-30 (referencing MPEG standards); LSI Integra Chipset at LSI60047 Manual at 1-1 ("LSI Logic's L64007 MPEG-2 DVB and JSAT compliant 32 PID transport demultiplexer integrates all audio, video, and data service MPEG-2 transport layer demultiplexing functions on a single chip."); MacInnis 385 at 1:37-39 ("The present invention relates generally to integrated circuits and systems, and more particularly to a

system for processing and displaying video and graphics.”); Fujii 695 at 1:5-9 (“The present invention relates to decoding video and audio data which are multiplexed after compression coding, and more particularly to a receiver/decoder for receiving video and audio data compression encoded by high efficiency coding means and decoding the received encoded data.”); Charles 949 at 1:7-13 (“The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications.”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of this claim limitation and application of this limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add a media switch operating asynchronously and autonomously with a CPU to a ’389 Anticipatory Reference or an Appendix A Reference to improve the function and utility of the same, *e.g.*, at least in part, offloading the system’s media processing needs from the processor, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, a media switch operating asynchronously and autonomously with a CPU was well-known in the art by the time of the ’389 patent’s claimed invention and thus, adding it to a ’389 Anticipatory Reference or an Appendix

A Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**24. “said Media Switch allows the CPU to queue up Direct Memory Access (DMA) transfers” (claims 22, 53)**

Claims 22 and 53 require “said Media Switch allows the CPU to queue up Direct Memory Access (DMA) transfers.” To the extent TiVo contends that a ’389 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Chauvel 855
- STi5500
- Toshiba TC81220F
- Ryan 976
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- So 559
- Nguyen 054
- MacInnis 385
- Thomason 612
- So 559
- O’Callaghan 263

In addition, to the extent TiVo contends that any of the Appendix A References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement

Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '389 Anticipatory References or the Appendix A References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, DMA transfer queueing was well-known design choice in the art by the time of the '389 patent's claimed invention. Furthermore, the '389 Anticipatory References, the Appendix A References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, AV7110 at 7, § 1 ("The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box."); Nguyen 054 at 3:31-43 ("[M]ultimedia computing such as audio and video data compression and decompression requires many repetitive calculations on pixel arrays and strings of audio data. To perform real-time multimedia operations, a general purpose processor which manipulates scalar data . . . must operate at a high clock frequency. . . . Therefore, the vector processor can perform real-time multimedia operations at a fraction of the clock frequency required for a general purpose processor to perform the same function."); Charles 949 at 1:7-13 ("The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications."); Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."), 2:15-30 (referencing MPEG standards). Moreover, the '389 Anticipatory References, the Appendix A References, and the exemplary

Secondary references seek to solve a similar problem (*e.g.*, efficient and direct access to memory) and given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '389 Anticipatory Reference and Appendix A Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add DMA transfer queueing to a '389 Anticipatory Reference or an Appendix A Reference. One of ordinary skill in the art would have been motivated to add "a DMA controller" to improve the function and utility of the same, *e.g.*, facilitating efficient and direct access to memory, and such a combination would have been within that person's skill.

## **B. '195 Patent**

### **1. "a linear cache for storing information from said data stream" (claims 58, 78); "a plurality of linear caches for storing information from said data streams as digital blocks" (claim 119)**

Claims 58/78 require "a linear cache for storing information from said data stream" and claim 119 requires "a plurality of linear caches for storing information from said data streams as digital blocks." To the extent TiVo contends that a '195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Logan 551
- Lynch 423
- Feng

- Brodsky 186
- Hooper 455
- Ottesen 815
- Polish 202
- Windrem 172
- Porter 539
- Nelson 786
- Yurt 992
- Yamagishi 008
- Abbott 679
- Rowe
- Katayama
- Shaw 689
- Fujinami 274
- Weimer 082
- Pak 602
- Engle 801
- Cooper 209
- Camhi 444
- Masahiko
- Iwasaki 536

In addition, to the extent TiVo contends that any of the prior art references for which claim charts have been provided in Appendix B (“Appendix B References”) fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions



and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this limitation, a "linear cache" was well-known in the art as one of several different memory techniques by the time of the '195 patent's claimed invention. In addition, combining a '195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '195 Anticipatory References, the Appendix B References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing). *See, e.g.*, Brodsky 186 at 1:8-11 ("The present invention is directed to the field of video, monitoring, storage and playback. It is more particularly directed to concurrent storage of a video signal being received and display of a previously stored signal."); Lynch 423 at 1:8-11 ("The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals."); Hooper 455 at 1:6-8 ("This invention applies to the general area of information distribution, and more particularly to information distributed as video signals."); Ottesen 815 at 1:24-29 ("The present invention relates generally to communication systems, and, more particularly, to a method and apparatus for providing a media-on-demand communication system including a multimedia server and independent set-top control units for receiving and controlling multimedia programming preferably on a pay-per-view basis."); Polish 202 at 1:16-19 ("This invention relates generally to digital video, and more particularly to a system and method for distributing and managing digital video information in a video distribution network."); Windrem 172 at 1:5-8 ("This invention relates generally to digital

video recorders and, more particularly, to cache management and disk utilization for digital video recorders having multiple inputs and outputs.”); Porter 539 at 1:6-10 (“The present invention relates to a method and apparatus for processing audio-visual information, and more specifically, to a method and apparatus for providing non-sequential access to audio-visual information stored in a digital format.”); Nelson 786 at 1:6-10 (“This invention relates to the management of digitized media stream data, *e.g.*, digitized video, and particularly relates to the capture, storage, distribution, access and presentation of digital video within a network computing environment.”). Given the design needs, combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in view of known memory storage techniques to add “a linear cache for storing information from said data stream” or a plurality thereof to a ’195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to add one or more “linear caches” to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “a linear cache for storing information from said data stream” or plurality thereof, at least according to Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, was well-known in the art by the time of the ’195 patent’s claimed invention and thus, adding it to a ’195 Anticipatory Reference or an Appendix B Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

2. **“cache access means for selecting a portion of the linear cache for streaming access to information stored therein” (claims 58, 78);**

**“cache access means for selecting a portion of said linear caches for streaming access” (claim 119)**

Claims 58/78 require “cache access means for selecting a portion of the linear cache for streaming access to information stored therein” and claim 119 requires “cache access means for selecting a portion of said linear caches for streaming access.” To the extent TiVo contends that a ’195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Logan 551
- Lynch 423
- Brodsky 186
- Feng
- Hooper 455
- Ottesen 815
- Polish 202
- Windrem 172
- Porter 539
- Nelson 786
- Yurt 992
- Yamagishi 008
- Abbott 679
- Rowe
- Katayama
- Shaw 689
- Fujinami 274

- Weimer 082
- Pak 602
- Engle 801
- Cooper 209
- Camhi 444
- Masahiko
- Iwasaki 536

In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, it was well-known in the art by the time of the '195 patent's claimed invention to provide an access method for streaming access to information stored in one or more linear caches. In addition, combining a '195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '195 Anticipatory References, the Appendix B References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Hooper 455 at 1:6-8 ("This invention applies to the general area of information distribution, and more particularly to information distributed as video signals."); Polish 202 at 1:16-19 ("This invention relates generally to digital video, and more particularly to

a system and method for distributing and managing digital video information in a video distribution network.”); Windrem 172 at 1:5-8 (“This invention relates generally to digital video recorders and, more particularly, to cache management and disk utilization for digital video recorders having multiple inputs and outputs.”); Lynch 423 at 1:8-11 (“The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals.”); Ottesen 815 at 1:24-29 (“The present invention relates generally to communication systems, and, more particularly, to a method and apparatus for providing a media-on-demand communication system including a multimedia server and independent set-top control units for receiving and controlling multimedia programming preferably on a pay-per-view basis.”); Yurt 992 at 1:6-10 (“The present invention relates generally to an audio and video transmission and receiving system, and more specifically to such a system in which the user controls the access and the playback operations of selected material.”); Yamagishi 008 at 1:7-11 (“The present invention relates to a method for reproducing pictures which reproduces video data of a moving picture coded with high efficiency by a MPEG (Moving Pictures Expert Group) method or the like in a jump reproducing mode.”); Abbott 679 at 1:10-15 (“The present invention relates generally to media delivery systems. More particularly, the present invention relates to a system and method for implementing interactive media delivery. Still more particularly, the present invention relates to a system and method for media stream indexing and synchronization.”); Logan 551 at 1:7-13 (“This invention relates generally to video and audio broadcast recording and playback systems and more particularly, although in its broader aspects not exclusively, to an arrangement for monitoring programming as it is broadcast and for enabling the listener or viewer to pause, replay and fast-forward the broadcast programming.”); Shaw 689 at 1:11-22 (“The field of the present invention is methods and computer program products relating to timing issues in multimedia applications, such as stream synchronization and rate matching between a generating clock and a rendering clock. The present invention also relates to standardized timing mechanisms in software drivers. More specifically, the present invention is directed to methods

and computer program products for providing timing and clock mechanisms used by multiple entities, such as interconnected software drivers, in a standardized fashion so that multiple streams of processed data may be synchronized and rates between different hardware clocks may be matched.”); Fujinami 274 at 1:16-23 (“This invention relates to an apparatus and method for processing a variable-rate coded signal prior to recording so that high-speed searching can be carried out on a recording medium on which the processed signal is recorded. The invention also relates to an apparatus and method for performing a high-speed search on a medium on which a processed variable-rate coded signal is recorded. Finally, the invention relates to a recording of the processed variable-rate coded signal.”); Weimer 082 at 3:1-3 (“FIG. 1 shows audio/video entertainment apparatuses forming a local bus communication system constructed in accordance with the invention.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in view of known memory storage techniques to add providing an access method for streaming access to information stored in one or more linear caches to a ’195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to provide this functionality to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, providing an access method for streaming access to information stored in a linear cache at least according to Plaintiff’s apparent interpretation of this claim limitation, was well-known in the art by the time of the ’195 patent’s claimed invention and, thus, adding it to a ’195 Anticipatory References or an Appendix B Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

3. **“cache control means for controlling a rate of said streaming access to said linear cache” (claims 58, 78); “said cache control means controls a rate and direction of said streaming access” (claim 58, 119); “cache control means for controlling a rate of streaming access from said linear caches” (claim 119)**

Claims 58 and 78 require a “cache control means” that controls a rate and direction of streaming access to the linear cache, and claim 119 requires a “cache control means” that controls a rate and direction of streaming access from said linear caches. To the extent TiVo contends that a ’195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Logan 551
- Lynch 423
- Brodsky 186
- Hooper 455
- Ottesen 815
- Polish 202
- Windrem 172
- Porter 539
- Feng
- Nelson 786
- Yurt 992
- Yamagishi 008
- Abbott 679
- Rowe
- Katayama

- Shaw 689
- Fujinami 274
- Weimer 082
- Pak 602
- Engle 801
- Cooper 209
- Camhi 444
- Masahiko
- Iwasaki 536

In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, it was well-known in the art by the time of the '195 patent's claimed invention to control both the rate and direction of streaming access to a linear cache (or from a linear cache, to the extent Plaintiff interprets "streaming access to a linear cache" as the same as "streaming access from a linear cache" as recited in claim 119). In addition, combining a '195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '195 Anticipatory References, Appendix B References, and the Secondary References are in



the same field of endeavor (*e.g.*, media processing). *See, e.g.*, Logan 551 at 1:7-13 (“This invention relates generally to video and audio broadcast recording and playback systems and more particularly, although in its broader aspects not exclusively, to an arrangement for monitoring programming as it is broadcast and for enabling the listener or viewer to pause, replay and fast-forward the broadcast programming.”); Lynch 423 at 1:8-11 (“The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals.”); Ottesen 815 at 1:24-29 (“The present invention relates generally to communication systems, and, more particularly, to a method and apparatus for providing a media-on-demand communication system including a multimedia server and independent set-top control units for receiving and controlling multimedia programming preferably on a pay-per-view basis.”); Windrem 172 at 1:5-8 (“This invention relates generally to digital video recorders and, more particularly, to cache management and disk utilization for digital video recorders having multiple inputs and outputs.”); Nelson 786 at 1:6-10 (“This invention relates to the management of digitized media stream data, *e.g.*, digitized video, and particularly relates to the capture, storage, distribution, access and presentation of digital video within a network computing environment.”); Yamagishi 008 at 1:7-11 (“The present invention relates to a method for reproducing pictures which reproduces video data of a moving picture coded with high efficiency by a MPEG (Moving Pictures Expert Group) method or the like in a jump reproducing mode.”); Shaw 689 at 1:11-22 (“The field of the present invention is methods and computer program products relating to timing issues in multimedia applications, such as stream synchronization and rate matching between a generating clock and a rendering clock. The present invention also relates to standardized timing mechanisms in software drivers. More specifically, the present invention is directed to methods and computer program products for providing timing and clock mechanisms used by multiple entities, such as interconnected software drivers, in a standardized fashion so that multiple streams of processed data may be synchronized and rates between different hardware clocks may be matched.”); Weimer 082 at 3:1-3 (“FIG. 1 shows audio/video entertainment apparatuses

forming a local bus communication system constructed in accordance with the invention.”); Engle 801 at 1:4-7 (“This invention relates to the field of image recordation and playback, and in particular concerns user programming of control commands and data referring to recorded image tracks.”); Cooper 209 at 1:13-16 (“This invention relates to the field of delivery of programming, for example entertainment and educational programming such as that currently delivered by television and film technology.”); Camhi 444 at 1:12-16 (“The present invention relates to information and entertainment systems, and more particularly, to a keyboard and memory equipped interface apparatus for the storage and processing of signals associated with such information and entertainment systems.”)

Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art, as demonstrated in the Secondary References listed above. That is, it would have been obvious in view of known memory storage techniques to add controlling both the rate and direction of streaming access to a linear cache (or from a linear cache, to the extent Plaintiff interprets “streaming access to a linear cache” as the same as “streaming access from a linear cache” as recited in claim 119) to a ’195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to provide controlling both the rate and direction of streaming access to a linear cache to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, controlling both the rate and direction of streaming access to a linear cache, at least according to Plaintiff’s apparent interpretation of this claim limitation, was well-known in the art by the time of the ’195 patent’s claimed invention and, thus, adding it to a ’195 Anticipatory Reference or an Appendix B Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

4. **“synchronization means for synchronizing streamed information from said linear cache for delivery to said cache access means” (claims 58, 78)**

Claims 58 and 78 require “synchronization means for synchronizing streamed information from said linear cache for delivery to said cache access means.” To the extent TiVo contends that a ’195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Rothermel (discussed below)
- Herman (discussed below)
- Parsons (discussed below)
- Sung (discussed below)
- Ottesen 815
- Porter 539
- Nelson 786
- Yurt 992
- Yamagishi 008
- Abbott 679
- Rowe
- Shaw 689
- Fujinami 274
- Weimer 082
- Pak 602
- Engle 801
- Cooper 209

- Camhi 444
- Masahiko
- Iwasaki 536
- O'Callaghan 263 (discussed below)

In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, it was well-known in the art by the time of the '195 patent's claimed invention that "stream synchronization can be further subdivided into intra-stream synchronization and inter-stream synchronization," wherein "the former refers to preserving temporal relationships of data within a stream, the latter deals with the temporal dependencies across streams." Rothermel at 324, 325-27 (§ 2 disclosing "basic principles and concepts" of inter-stream synchronization), 327-28 (§§ 3.1, 3.4 discussing a "master/slave synchronization protocol"); Herman at 90 (disclosing "time-related synchronization schemes" and "event-based synchronization"); Sung at 230 (§ 8 disclosing exemplary techniques for "how to resynchronize the audio and video"); O'Callaghan 263 at 9:48-10:13 ("MPEG-2 packets carry time stamps which relate to an overall time frame associated with the start of the program. The time stamps are utilized to coordinate the arrival of MPEG-2 packets. For example, if MPEG-2 audio packets arrive early at the audio decoder, that is, before the related video packets arrive, they will be held until the corresponding video packets arrive and then both audio and

corresponding video packet information will be released simultaneously at exactly the right time to be part of a smooth flowing program presentation. The time stamp controls the release.”). In addition, combining a ’195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the ’195 Anticipatory References, the Appendix B References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing). *See, e.g.*, Ottesen 815 at 1:24-29 (“The present invention relates generally to communication systems, and, more particularly, to a method and apparatus for providing a media-on-demand communication system including a multimedia server and independent set-top control units for receiving and controlling multimedia programming preferably on a pay-per-view basis.”); Porter 539 at 1:6-10 (“The present invention relates to a method and apparatus for processing audio-visual information, and more specifically, to a method and apparatus for providing non-sequential access to audio-visual information stored in a digital format.”); Nelson 786 at 1:6-10 (“This invention relates to the management of digitized media stream data, *e.g.*, digitized video, and particularly relates to the capture, storage, distribution, access and presentation of digital video within a network computing environment.”); Yurt 992 at 1:6-10 (“The present invention relates generally to an audio and video transmission and receiving system, and more specifically to such a system in which the user controls the access and the playback operations of selected material.”); Yamagishi 008 at 1:7-11 (“The present invention relates to a method for reproducing pictures which reproduces video data of a moving picture coded with high efficiency by a MPEG (Moving Pictures Expert Group) method or the like in a jump reproducing mode.”); Abbott 679 at 1:10-15 (“The present invention relates generally to media delivery systems. More particularly, the present invention relates to a system and method for implementing interactive media delivery. Still more particularly, the present invention relates to a system and method for media stream indexing and synchronization.”); Shaw 689 at 1:11-22 (“The field of the present invention is methods and computer program products relating to timing issues in multimedia applications,

such as stream synchronization and rate matching between a generating clock and a rendering clock. The present invention also relates to standardized timing mechanisms in software drivers. More specifically, the present invention is directed to methods and computer program products for providing timing and clock mechanisms used by multiple entities, such as interconnected software drivers, in a standardized fashion so that multiple streams of processed data may be synchronized and rates between different hardware clocks may be matched.”); Fujinami 274 at 1:16-23 (“This invention relates to an apparatus and method for processing a variable-rate coded signal prior to recording so that high-speed searching can be carried out on a recording medium on which the processed signal is recorded. The invention also relates to an apparatus and method for performing a high-speed search on a medium on which a processed variable-rate coded signal is recorded. Finally, the invention relates to a recording of the processed variable-rate coded signal.”); Weimer 082 at 3:1-3 (“FIG. 1 shows audio/video entertainment apparatuses forming a local bus communication system constructed in accordance with the invention.”); Pak 602 at 1:20-24 (“This invention relates to a repeat reproduction method for magnetic tape and, more particularly, to a method for repeatedly reproducing data from a section of a magnetic tape desired by the user in which audio and/or video signals are recorded.”); Engle 801 at 1:4-7 (“This invention relates to the field of image recordation and playback, and in particular concerns user programming of control commands and data referring to recorded image tracks.”); Cooper 209 at 1:13-16 (“This invention relates to the field of delivery of programming, for example entertainment and educational programming such as that currently delivered by television and film technology.”); Camhi 444 at 1:12-16 (“The present invention relates to information and entertainment systems, and more particularly, to a keyboard and memory equipped interface apparatus for the storage and processing of signals associated with such information and entertainment systems.”); O’Callaghan 263 at 1:10-15 (“The invention relates to the transmission and distribution of video programming and more particularly to a method and apparatus for rapid channel selection and for providing fast forward, reverse and channel pause functions when receiving digital video programming.”). Further, the references seek to solve a

similar problem, *See, e.g.*, Parsons at 27 (disclosing “several problems including the difficulty in starting two streams at the same time, and also because the audio stream is independent and can encounter its own time fluctuations”), and given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references, *See, e.g., id.* (“To solve this problem, the streaming subsystem allows a media driver to indicate master/slave timing relationships between multiple streams.”).

Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “synchronization means for synchronizing streamed information from said linear cache for delivery to said cache access means” to a ’195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to add “synchronization means for synchronizing streamed information from said linear cache for delivery to said cache access means” to improve the function and utility of the same, *e.g.*, synchronizing streams, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “synchronization means for synchronizing streamed information from said linear cache for delivery to said cache access means” was well-known in the art by the time of the ’195 patent’s claimed invention and thus, adding it to a ’195 Anticipatory Reference or an Appendix B Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

5. **“said cache control means sends clock events to said cache access means to control a rate and direction of said streaming access” (claims 59, 78)**

Claims 59 and 78 require “said cache control means sends clock events to said cache access means to control a rate and direction of said streaming access.” To the extent TiVo contends that a ’195 Anticipatory Reference fails to disclose these elements, such reference(s)

can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Krause 714
- Windrem 172
- Hooper 455
- Polish 202
- Cannon 706
- Ottesen 815

In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the ’195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff’s apparent interpretation of this claim limitation, it was known in the art by the time of the ’195 patent’s claimed invention that clock events could be used at least to control a rate of streaming access. In addition, combining a ’195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the ’195 Anticipatory References, the Appendix B References, and the exemplary Secondary References



are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Hooper 455 at 1:6-8 (“This invention applies to the general area of information distribution, and more particularly to information distributed as video signals.”); Polish 202 at 1:16-19 (“This invention relates generally to digital video, and more particularly to a system and method for distributing and managing digital video information in a video distribution network.”); Windrem 172 at 1:5-8 (“This invention relates generally to digital video recorders and, more particularly, to cache management and disk utilization for digital video recorders having multiple inputs and outputs.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add clock events that could be used at least to control a rate of streaming access to a ’195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to add clock events that could be used at least to control a rate of streaming access to improve the function and utility of the same, *e.g.*, to vary the rate of streaming access to a cache, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, clock events that could be used at least to control a rate of streaming access were well-known in the art by the time of the ’195 patent’s claimed invention and thus, adding it to a ’195 Anticipatory Reference or an Appendix B Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

6. **“said linear cache maintains a window that represents a time span into a past history of said data stream that includes a most recently stored portion of said data stream” (claims 58, 78); “said linear cache maintains a window that represents a time span into a past history of**

**said data stream that includes a most recently stored portion of said data streams” (claim 119)**

Claims 58 and 78 require “said linear cache maintains a window that represents a time span into a past history of said data stream that includes a most recently stored portion of said data stream” and claim 119 requires “said linear cache maintains a window that represents a time span into a past history of said data stream that includes a most recently stored portion of said data streams.” To the extent TiVo contends that a ’195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Logan 551
- Lynch 423
- Brodsky 186
- Hooper 455
- Ottesen 815
- Polish 202
- Windrem 172
- Katayama
- Cooper 209
- Camhi 444
- Masahiko
- Iwasaki 536

In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious

this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, it was well-known in the art by the time of the '195 patent's claimed invention at least to use a cache window containing the most recent portions of a media stream. In addition, combining a '195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '195 Anticipatory References, the Appendix B References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing), *see, e.g.*, Brodsky 186 at 1:8-11 ("The present invention is directed to the field of video, monitoring, storage and playback. It is more particularly directed to concurrent storage of a video signal being received and display of a previously stored signal."); Lynch 423 at 1:8-11 ("The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals."); Hooper 455 at 1:6-8 ("This invention applies to the general area of information distribution, and more particularly to information distributed as video signals."); Ottesen 815 at 1:24-29 ("The present invention relates generally to communication systems, and, more particularly, to a method and apparatus for providing a media-on-demand communication system including a multimedia server and independent set-top control units for receiving and controlling multimedia programming preferably on a pay-per-view basis."); Polish 202 at 1:16-19 ("This invention relates generally to digital video, and more particularly to a system and method for distributing and managing digital video information in a video distribution network."); Logan 551 at 1:7-13

(“This invention relates generally to video and audio broadcast recording and playback systems and more particularly, although in its broader aspects not exclusively, to an arrangement for monitoring programming as it is broadcast and for enabling the listener or viewer to pause, replay and fast-forward the broadcast programming.”); Windrem 172 at 1:5-8 (“This invention relates generally to digital video recorders and, more particularly, to cache management and disk utilization for digital video recorders having multiple inputs and outputs.”); Cooper 209 at 1:13-16 (“This invention relates to the field of delivery of programming, for example entertainment and educational programming such as that currently delivered by television and film technology.”); Camhi 444 at 1:12-16 (“The present invention relates to information and entertainment systems, and more particularly, to a keyboard and memory equipped interface apparatus for the storage and processing of signals associated with such information and entertainment systems.”), and seek to solve a similar problem (*e.g.*, processing media streams with limited resources). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “[a] linear cache [that] maintains a window that represents a time span into a past history of said data stream that includes a most recently stored portion of said data stream” or data streams to a ’195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to use a cache window containing the most recent portions of a media stream to improve the function and utility of the same, *e.g.*, enabling media stream processing with limited system resources, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “[a] linear cache [that] maintains a window that represents a time span into a past history of said data stream that includes a most recently stored portion of said data stream” was a well-known design choice by the time of the

'195 patent's claimed invention and thus, adding it to a '195 Anticipatory Reference or an Appendix B Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**7. "said linear cache discards any information that falls outside of said window" (claims 58, 78, 119)**

Claims 58, 78, and 119 require "said linear cache discards any information that falls outside of said window." To the extent TiVo contends that a '195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Logan 551
- Lynch 423
- Brodsky 186
- Hooper 455
- Ottesen 815
- Polish 202
- Windrem 172
- Katayama
- Cooper 209

In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and at least under Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it was well-known in the art by the time of the '195 patent's claimed invention to discard information falling outside of the window. In addition, combining a '195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '195 Anticipatory References, the Appendix B References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing) and seek to solve a similar problem (*e.g.*, data storage constraints). *See, e.g.*, Logan 551 at 1:7-13 ("This invention relates generally to video and audio broadcast recording and playback systems and more particularly, although in its broader aspects not exclusively, to an arrangement for monitoring programming as it is broadcast and for enabling the listener or viewer to pause, replay and fast-forward the broadcast programming."); Brodsky 186 at 1:8-11 ("The present invention is directed to the field of video, monitoring, storage and playback. It is more particularly directed to concurrent storage of a video signal being received and display of a previously stored signal."); Lynch 423 at 1:8-11 ("The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals."); Hooper 455 at 1:6-8 ("This invention applies to the general area of information distribution, and more particularly to information distributed as video signals."); Ottesen 815 at 1:24-29 ("The present invention relates generally to communication systems, and, more particularly, to a method and apparatus for providing a media-on-demand communication system including a multimedia server and independent set-top control units for receiving and controlling multimedia programming preferably on a pay-per-

view basis.”); Polish 202 at 1:16-19 (“This invention relates generally to digital video, and more particularly to a system and method for distributing and managing digital video information in a video distribution network.”); Windrem 172 at 1:5-8 (“This invention relates generally to digital video recorders and, more particularly, to cache management and disk utilization for digital video recorders having multiple inputs and outputs.”); Cooper 209 at 1:13-16 (“This invention relates to the field of delivery of programming, for example entertainment and educational programming such as that currently delivered by television and film technology.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products it would have been obvious in the view of one of ordinary skill in the art to add “[a] linear cache [that] discards any information that falls outside of said window” to a ’195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to add “[a] linear cache [that] discards any information that falls outside of said window” to improve the function and utility of the same, *e.g.*, to enable maintaining a window that includes the most recently stored portion of the stream, and such a combination would have been within that person’s skill. Based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, “[a] linear cache [that] discards any information that falls outside of said window” was well-known in the art by the time of the ’195 patent’s claimed invention as demonstrated in the Secondary References listed above. Thus, adding it to a ’195 Anticipatory Reference or an Appendix B Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

8. **“stream capture means for capturing information for a particular data stream type and encoding said information before storing said information in said linear cache” (claims 60, 79); “stream capture means for capturing the information for a particular data stream type” (claim 121); “encoding said information before storing said information in a linear cache” (claim 122)**

Claims 60, 79, 121, and 122 require stream capture means for capturing information for a particular data stream type and encoding said information before storing said information in said linear cache. To the extent TiVo contends that a '195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Logan 551
- Lynch 423
- Ottesen 815
- Porter 539
- Nelson 786
- Yurt 992
- Yamagishi 008
- Abbott 679
- Rowe
- Fujinami 274
- Engle 801
- Cooper 209
- Camhi 444
- Masahiko
- Iwasaki 536



In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, it was well-known in the art by the time of the '195 patent's claimed invention to capture and encode media streams for storage in a linear cache. In addition, combining a '195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '195 Anticipatory References, the Appendix B References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing). *See, e.g.*, Logan 551 at 1:7-13 ("This invention relates generally to video and audio broadcast recording and playback systems and more particularly, although in its broader aspects not exclusively, to an arrangement for monitoring programming as it is broadcast and for enabling the listener or viewer to pause, replay and fast-forward the broadcast programming."); Lynch 423 at 1:8-11 ("The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals."); Ottesen 815 at 1:24-29 ("The present invention relates generally to communication systems, and, more particularly, to a method and apparatus for providing a media-on-demand communication system including a multimedia server and independent set-top control units for receiving and controlling multimedia programming preferably on a pay-per-view basis."); Porter 539 at 1:6-10

(“The present invention relates to a method and apparatus for processing audio-visual information, and more specifically, to a method and apparatus for providing non-sequential access to audio-visual information stored in a digital format.”); Nelson 786 at 1:6-10 (“This invention relates to the management of digitized media stream data, *e.g.*, digitized video, and particularly relates to the capture, storage, distribution, access and presentation of digital video within a network computing environment.”); Yurt 992 at 1:6-10 (“The present invention relates generally to an audio and video transmission and receiving system, and more specifically to such a system in which the user controls the access and the playback operations of selected material.”); Yamagishi 008 at 1:7-11 (“The present invention relates to a method for reproducing pictures which reproduces video data of a moving picture coded with high efficiency by a MPEG (Moving Pictures Expert Group) method or the like in a jump reproducing mode.”); Abbott 679 at 1:10-15 (“The present invention relates generally to media delivery systems. More particularly, the present invention relates to a system and method for implementing interactive media delivery. Still more particularly, the present invention relates to a system and method for media stream indexing and synchronization.”); Fujinami 274 at 1:16-23 (“This invention relates to an apparatus and method for processing a variable-rate coded signal prior to recording so that high-speed searching can be carried out on a recording medium on which the processed signal is recorded. The invention also relates to an apparatus and method for performing a high-speed search on a medium on which a processed variable-rate coded signal is recorded. Finally, the invention relates to a recording of the processed variable-rate coded signal.”); Engle 801 at 1:4-7 (“This invention relates to the field of image recordation and playback, and in particular concerns user programming of control commands and data referring to recorded image tracks.”); Cooper 209 at 1:13-16 (“This invention relates to the field of delivery of programming, for example entertainment and educational programming such as that currently delivered by television and film technology.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add capturing and encoding media streams for storage in a linear cache to a '195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to add “stream capture means for capturing information for a particular data stream type and encoding said information before storing said information in said linear cache” to improve the function and utility of the same, *e.g.*, the ability to capture different stream types for caching, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “stream capture means for capturing information for a particular data stream type and encoding said information before storing said information in said linear cache” was well-known in the art by the time of the '195 patent’s claimed invention and thus, adding it to a '195 Anticipatory Reference or an Appendix B Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**9. “presentation means for presenting the streaming access from said cache access means to a storage device” (claims 64, 83)**

Claims 64 and 83 require “presentation means for presenting the streaming access from said cache access means to a storage device.” To the extent TiVo contends that a '195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Brodsky 186
- Porter 539
- Nelson 786

- Yurt 992
- Yamagishi 008
- Abbott 679
- Rowe
- Shaw 689
- Weimer 082
- Pak 602
- Engle 801
- Cooper 209
- Camhi 444
- Masahiko
- Iwasaki 536

In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, it was well-known in the art by the time of the '195 patent's claimed invention to present multimedia data to a storage device. In addition, combining a '195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '195

Anticipatory References, the Appendix B References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing). *See, e.g.*, Brodsky 186 at 1:8-11 (“The present invention is directed to the field of video, monitoring, storage and playback. It is more particularly directed to concurrent storage of a video signal being received and display of a previously stored signal.”); Porter 539 at 1:6-10 (“The present invention relates to a method and apparatus for processing audio-visual information, and more specifically, to a method and apparatus for providing non-sequential access to audio-visual information stored in a digital format.”); Nelson 786 at 1:6-10 (“This invention relates to the management of digitized media stream data, *e.g.*, digitized video, and particularly relates to the capture, storage, distribution, access and presentation of digital video within a network computing environment.”); Yurt 992 at 1:6-10 (“The present invention relates generally to an audio and video transmission and receiving system, and more specifically to such a system in which the user controls the access and the playback operations of selected material.”); Yamagishi 008 at 1:7-11 (“The present invention relates to a method for reproducing pictures which reproduces video data of a moving picture coded with high efficiency by a MPEG (Moving Pictures Expert Group) method or the like in a jump reproducing mode.”); Abbott 679 at 1:10-15 (“The present invention relates generally to media delivery systems. More particularly, the present invention relates to a system and method for implementing interactive media delivery. Still more particularly, the present invention relates to a system and method for media stream indexing and synchronization.”); Shaw 689 at 1:11-22 (“The field of the present invention is methods and computer program products relating to timing issues in multimedia applications, such as stream synchronization and rate matching between a generating clock and a rendering clock. The present invention also relates to standardized timing mechanisms in software drivers. More specifically, the present invention is directed to methods and computer program products for providing timing and clock mechanisms used by multiple entities, such as interconnected software drivers, in a standardized fashion so that multiple streams of processed data may be synchronized and rates between different hardware clocks may be matched.”); Weimer 082 at 3:1-3 (“FIG. 1 shows audio/video

entertainment apparatuses forming a local bus communication system constructed in accordance with the invention.”); Pak 602 at 1:20-24 (“This invention relates to a repeat reproduction method for magnetic tape and, more particularly, to a method for repeatedly reproducing data from a section of a magnetic tape desired by the user in which audio and/or video signals are recorded.”); Engle 801 at 1:4-7 (“This invention relates to the field of image recordation and playback, and in particular concerns user programming of control commands and data referring to recorded image tracks.”); Cooper 209 at 1:13-16 (“This invention relates to the field of delivery of programming, for example entertainment and educational programming such as that currently delivered by television and film technology.”); Camhi 444 at 1:12-16 (“The present invention relates to information and entertainment systems, and more particularly, to a keyboard and memory equipped interface apparatus for the storage and processing of signals associated with such information and entertainment systems.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references. Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add “presentation means for presenting the streaming access from said cache access means to a storage device” to a ’195 Anticipatory Reference or an Appendix B Reference.

**10. “said cache access means implements a reverse function by moving a current block indicator backwards through said cache” (claims 73, 92)**

Claims 73 and 92 require “said cache access means implements a reverse function by moving a current block indicator backwards through said cache.” To the extent TiVo contends that a ’195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art

references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Logan 551
- Lynch 423
- Brodsky 186
- Hooper 455
- Ottesen 815
- Polish 202
- Porter 539
- Nelson 786
- Yurt 992
- Yamagishi 008
- Abbott 679
- Rowe
- Katayama
- Fujinami 274
- Weimer 082
- Pak 602
- Cooper 209
- Camhi 444
- Masahiko

In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement

Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, moving a current block indicator backwards through a cache was a well-known technique for implementing a reverse function in the art by the time of the '195 patent's claimed invention. In addition, combining a '195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '195 Anticipatory References, the Appendix B References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing) and seek to solve a similar problem (*e.g.*, manipulation of streaming media playback). *See, e.g.*, Logan 551 at 1:7-13 ("This invention relates generally to video and audio broadcast recording and playback systems and more particularly, although in its broader aspects not exclusively, to an arrangement for monitoring programming as it is broadcast and for enabling the listener or viewer to pause, replay and fast-forward the broadcast programming."); Lynch 423 at 1:8-11 ("The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals."); Brodsky 186 at 1:8-11 ("The present invention is directed to the field of video, monitoring, storage and playback. It is more particularly directed to concurrent storage of a video signal being received and display of a previously stored signal."); Hooper 455 at 1:6-8 ("This invention applies to the general area of information distribution, and more particularly to information distributed as video signals."); Ottesen 815 at 1:24-29 ("The present invention relates generally to communication systems, and, more particularly, to a method and apparatus for providing a media-on-demand communication



system including a multimedia server and independent set-top control units for receiving and controlling multimedia programming preferably on a pay-per-view basis.”); Polish 202 at 1:16-19 (“This invention relates generally to digital video, and more particularly to a system and method for distributing and managing digital video information in a video distribution network.”); Porter 539 at 1:6-10 (“The present invention relates to a method and apparatus for processing audio-visual information, and more specifically, to a method and apparatus for providing non-sequential access to audio-visual information stored in a digital format.”); Nelson 786 at 1:6-10 (“This invention relates to the management of digitized media stream data, *e.g.*, digitized video, and particularly relates to the capture, storage, distribution, access and presentation of digital video within a network computing environment.”); Yurt 992 at 1:6-10 (“The present invention relates generally to an audio and video transmission and receiving system, and more specifically to such a system in which the user controls the access and the playback operations of selected material.”); Yamagishi 008 at 1:7-11 (“The present invention relates to a method for reproducing pictures which reproduces video data of a moving picture coded with high efficiency by a MPEG (Moving Pictures Expert Group) method or the like in a jump reproducing mode.”); Abbott 679 at 1:10-15 (“The present invention relates generally to media delivery systems. More particularly, the present invention relates to a system and method for implementing interactive media delivery. Still more particularly, the present invention relates to a system and method for media stream indexing and synchronization.”); Fujinami 274 at 1:16-23 (“This invention relates to an apparatus and method for processing a variable-rate coded signal prior to recording so that high-speed searching can be carried out on a recording medium on which the processed signal is recorded. The invention also relates to an apparatus and method for performing a high-speed search on a medium on which a processed variable-rate coded signal is recorded. Finally, the invention relates to a recording of the processed variable-rate coded signal.”); Weimer 082 at 3:1-3 (“FIG. 1 shows audio/video entertainment apparatuses forming a local bus communication system constructed in accordance with the invention.”); Pak 602 at 1:20-24 (“This invention relates to a repeat reproduction method for magnetic tape and, more

particularly, to a method for repeatedly reproducing data from a section of a magnetic tape desired by the user in which audio and/or video signals are recorded.”); Cooper 209 at 1:13-16 (“This invention relates to the field of delivery of programming, for example entertainment and educational programming such as that currently delivered by television and film technology.”); Camhi 444 at 1:12-16 (“The present invention relates to information and entertainment systems, and more particularly, to a keyboard and memory equipped interface apparatus for the storage and processing of signals associated with such information and entertainment systems.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “[a] cache access means [that] implements a reverse function by moving a current block indicator backwards through said cache” to a ’195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to add “[a] cache access means [that] implements a reverse function by moving a current block indicator backwards through said cache” to improve the function and utility of the same, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “[a] cache access means [that] implements a reverse function by moving a current block indicator backwards through said cache” was well-known in the art by the time of the ’195 patent’s claimed invention and thus, adding it to a ’195 Anticipatory Reference or an Appendix B Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

11. **“said cache access means reverts to moving said current block indicator forward through said cache if said current block indicator**

**cannot be moved past the oldest block in said linear cache” (claims 75, 94)**

Claims 75 and 94 require “said cache access means reverts to moving said current block indicator forward through said cache if said current block indicator cannot be moved past the oldest block in said linear cache.” To the extent TiVo contends that a ’195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Logan 551
- Lynch 423
- Hooper 455
- Ottesen 815
- Katayama
- Weimer 082
- Pak 602
- Engle 801
- Suzuki 435

In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the ’195 Anticipatory References or the Appendix B References with any one or more of the

above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, resuming playback when the current block indicator reaches the oldest block in a cache was well-known in the art by the time of the '195 patent's claimed invention. In addition, combining a '195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '195 Anticipatory References, the Appendix B References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing) and seek to solve a similar problem (*e.g.*, manipulating playback within a limited window). *See, e.g.*, Suzuki 435 at 1:7-13 ("The present invention relates to a video signal frame search apparatus for enabling a specific frame (or field) of a video signal recorded on a magnetic tape of a VTR (Video Tape Recorder) to be specified by a user, and for the specified frame to be searched for and subsequently outputted to a video printer apparatus to be printed."); Logan 551 at 1:7-13 ("This invention relates generally to video and audio broadcast recording and playback systems and more particularly, although in its broader aspects not exclusively, to an arrangement for monitoring programming as it is broadcast and for enabling the listener or viewer to pause, replay and fast-forward the broadcast programming."); Lynch 423 at 1:8-11 ("The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals."); Hooper 455 at 1:6-8 ("This invention applies to the general area of information distribution, and more particularly to information distributed as video signals."); Ottesen 815 at 1:24-29 ("The present invention relates generally to communication systems, and, more particularly, to a method and apparatus for providing a media-on-demand communication system including a multimedia server and independent set-top control units for receiving and controlling multimedia programming preferably on a pay-per-view basis."); Weimer 082 at 3:1-3 ("FIG. 1 shows audio/video entertainment apparatuses forming a local bus communication system constructed in

accordance with the invention.”); Pak 602 at 1:20-24 (“This invention relates to a repeat reproduction method for magnetic tape and, more particularly, to a method for repeatedly reproducing data from a section of a magnetic tape desired by the user in which audio and/or video signals are recorded.”); Engle 801 at 1:4-7 (“This invention relates to the field of image recordation and playback, and in particular concerns user programming of control commands and data referring to recorded image tracks.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “[a] cache access means [that] reverts to moving said current block indicator forward through said cache if said current block indicator cannot be moved past the oldest block in said linear cache” to a ’195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to add “[a] cache access means [that] reverts to moving said current block indicator forward through said cache if said current block indicator cannot be moved past the oldest block in said linear cache” to improve the function and utility of the same, *e.g.*, maintaining playback within a limited window, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “revert[ing] to moving said current block indicator forward through said cache if said current block indicator cannot be moved past the oldest block in said linear cache” was well-known in the art by the time of the ’195 patent’s claimed invention and thus, adding it to a ’195 Anticipatory Reference or an Appendix B Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**12. “said cache access means implements a pause function by locking a current block indicator to one block in said linear cache” (claims 76, 95)**

Claims 76 and 95 require “said cache access means implements a pause function by locking a current block indicator to one block in said linear cache.” To the extent TiVo contends that a ’195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Logan 551
- Lynch 423
- Brodsky 186
- Hooper 455
- Ottesen 815
- Polish 202
- Porter 539
- Nelson 786
- Yurt 992
- Yamagishi 008
- Abbott 679
- Rowe
- Katayama
- Fujinami 274
- Weimer 082
- Pak 602
- Cooper 209

- Camhi 444
- Masahiko

In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, locking a current block indicator backwards was a known design choice for implementing a pause function in the art by the time of the '195 patent's claimed invention. In addition, combining a '195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '195 Anticipatory References, the Appendix B References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing) and seek to solve a similar problem (*e.g.*, manipulation of streaming media playback). *See, e.g.*, Logan 551 at 1:7-13 ("This invention relates generally to video and audio broadcast recording and playback systems and more particularly, although in its broader aspects not exclusively, to an arrangement for monitoring programming as it is broadcast and for enabling the listener or viewer to pause, replay and fast-forward the broadcast programming."); Lynch 423 at 1:8-11 ("The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals."); Brodsky 186 at 1:8-11 ("The present invention is directed to the

field of video, monitoring, storage and playback. It is more particularly directed to concurrent storage of a video signal being received and display of a previously stored signal.”); Hooper 455 at 1:6-8 (“This invention applies to the general area of information distribution, and more particularly to information distributed as video signals.”); Ottesen 815 at 1:24-29 (“The present invention relates generally to communication systems, and, more particularly, to a method and apparatus for providing a media-on-demand communication system including a multimedia server and independent set-top control units for receiving and controlling multimedia programming preferably on a pay-per-view basis.”); Polish 202 at 1:16-19 (“This invention relates generally to digital video, and more particularly to a system and method for distributing and managing digital video information in a video distribution network.”); Porter 539 at 1:6-10 (“The present invention relates to a method and apparatus for processing audio-visual information, and more specifically, to a method and apparatus for providing non-sequential access to audio-visual information stored in a digital format.”); Nelson 786 at 1:6-10 (“This invention relates to the management of digitized media stream data, *e.g.*, digitized video, and particularly relates to the capture, storage, distribution, access and presentation of digital video within a network computing environment.”); Yurt 992 at 1:6-10 (“The present invention relates generally to an audio and video transmission and receiving system, and more specifically to such a system in which the user controls the access and the playback operations of selected material.”); Yamagishi 008 at 1:7-11 (“The present invention relates to a method for reproducing pictures which reproduces video data of a moving picture coded with high efficiency by a MPEG (Moving Pictures Expert Group) method or the like in a jump reproducing mode.”); Abbott 679 at 1:10-15 (“The present invention relates generally to media delivery systems. More particularly, the present invention relates to a system and method for implementing interactive media delivery. Still more particularly, the present invention relates to a system and method for media stream indexing and synchronization.”); Fujinami 274 at 1:16-23 (“This invention relates to an apparatus and method for processing a variable-rate coded signal prior to recording so that high-speed searching can be carried out on a recording medium on which the processed signal is



recorded. The invention also relates to an apparatus and method for performing a high-speed search on a medium on which a processed variable-rate coded signal is recorded. Finally, the invention relates to a recording of the processed variable-rate coded signal.”); Weimer 082 at 3:1-3 (“FIG. 1 shows audio/video entertainment apparatuses forming a local bus communication system constructed in accordance with the invention.”); Pak 602 at 1:20-24 (“This invention relates to a repeat reproduction method for magnetic tape and, more particularly, to a method for repeatedly reproducing data from a section of a magnetic tape desired by the user in which audio and/or video signals are recorded.”); Cooper 209 at 1:13-16 (“This invention relates to the field of delivery of programming, for example entertainment and educational programming such as that currently delivered by television and film technology.”); Camhi 444 at 1:12-16 (“The present invention relates to information and entertainment systems, and more particularly, to a keyboard and memory equipped interface apparatus for the storage and processing of signals associated with such information and entertainment systems.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “[a] cache access means [that] implements a pause function by locking a current block indicator to one block in said linear cache” to a ’195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to add “[a] cache access means [that] implements a pause function by locking a current block indicator to one block in said linear cache” to improve the function and utility of the same, *e.g.*, enabling manipulation of playback, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “implement[ing] a pause function by locking a current block indicator to one block in said linear cache” was well-known in the art by the time of the ’195

patent's claimed invention and thus, adding it to a '195 Anticipatory Reference or an Appendix B Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**13. “said cache access means reverts to moving said current block indicator forward through said cache if said current block indicator is moved past the earliest block in said linear cache” (claims 77, 96)**

Claims 77 and 96 require “said cache access means reverts to moving said current block indicator forward through said cache if said current block indicator is moved past the earliest block in said linear cache.” To the extent TiVo contends that a '195 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Logan 551
- Lynch 423
- Hooper 455
- Ottesen 815
- Katayama
- Weimer 082
- Pak 602
- Engle 801
- Suzuki 435

In addition, to the extent TiVo contends that any of the Appendix B References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement

Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '195 Anticipatory References or the Appendix B References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, resuming playback when the current block indicator is moved past the earliest block in a cache was well-known in the art by the time of the '195 patent's claimed invention. In addition, combining a '195 Anticipatory Reference or an Appendix B Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '195 Anticipatory References, the Appendix B References, and the exemplary Secondary References are in the same field of endeavor (*e.g.*, media processing) and seek to solve a similar problem (*e.g.*, manipulating playback within a limited window). *See, e.g.*, Suzuki 435 at 1:7-13 ("The present invention relates to a video signal frame search apparatus for enabling a specific frame (or field) of a video signal recorded on a magnetic tape of a VTR (Video Tape Recorder) to be specified by a user, and for the specified frame to be searched for and subsequently outputted to a video printer apparatus to be printed."); Logan 551 at 1:7-13 ("This invention relates generally to video and audio broadcast recording and playback systems and more particularly, although in its broader aspects not exclusively, to an arrangement for monitoring programming as it is broadcast and for enabling the listener or viewer to pause, replay and fast-forward the broadcast programming."); Lynch 423 at 1:8-11 ("The present invention relates to processing of realtime video signals, and more particularly to time warping for video viewing by managing delay, review and continuation of realtime video signals."); Hooper 455 at 1:6-8 ("This invention applies to the general area of information distribution, and more particularly to information distributed as video signals."); Ottesen 815 at 1:24-29 ("The present invention relates generally to communication systems, and, more particularly, to a

method and apparatus for providing a media-on-demand communication system including a multimedia server and independent set-top control units for receiving and controlling multimedia programming preferably on a pay-per-view basis.”); Weimer 082 at 3:1-3 (“FIG. 1 shows audio/video entertainment apparatuses forming a local bus communication system constructed in accordance with the invention.”); Pak 602 at 1:20-24 (“This invention relates to a repeat reproduction method for magnetic tape and, more particularly, to a method for repeatedly reproducing data from a section of a magnetic tape desired by the user in which audio and/or video signals are recorded.”); Engle 801 at 1:4-7 (“This invention relates to the field of image recordation and playback, and in particular concerns user programming of control commands and data referring to recorded image tracks.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’195 Anticipatory Reference and Appendix B Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “[a] cache access means [that] reverts to moving said current block indicator forward through said cache if said current block indicator is moved past the earliest block in said linear cache” to a ’195 Anticipatory Reference or an Appendix B Reference. One of ordinary skill in the art would have been motivated to add “[a] cache access means [that] reverts to moving said current block indicator forward through said cache if said current block indicator is moved past the earliest block in said linear cache” to improve the function and utility of the same, *e.g.*, maintaining playback within a limited window, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, “revert[ing] to moving said current block indicator forward through said cache if said current block indicator is moved past the earliest block in said linear cache” was well-known in the art by the time of the ’195 patent’s claimed invention and thus, adding it to a ’195 Anticipatory Reference or an Appendix B

Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**C. '472 Patent**

**1. “simultaneous storage and playback of multimedia data”;  
“multimedia data are stored on said storage subsystem and retrieved  
from said storage subsystem essentially simultaneously” (claim 1)**

Claim 1 requires “multimedia data are stored on said storage subsystem and retrieved from said storage subsystem essentially simultaneously,” and to the extent the preamble is limiting, claim 1 also requires “simultaneous storage and playback of multimedia data.” To the extent TiVo contends that a '472 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- So 559
- Lenihan 843
- AV 7110 Specification (and related disclosures in Chauvel 855)
- Nguyen 054
- Logan 551
- Kageyama
- Sato (discussed below)
- Glover 045 (discussed below)
- Colligan 711 (discussed below)
- Mano 892 (discussed below)
- Krause 714
- Sampat 724

- Lang 298
- Sasaki 756
- Ottesen 878
- Goldwasser 428
- Inoue 881
- Camhi 444
- Schaefer 000
- Thomason 612

In addition, to the extent TiVo contends that any of the prior art references for which claim charts have been provided in Appendix C (“Appendix C References”) fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the ’472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff’s apparent interpretation of these elements and application of these elements to the accused products, the above elements were well-known in the art by the time of the ’472 patent’s claimed invention. *See, e.g.*, Kageyama at § 3, 470 (“To better meet the needs of users, the proposed DVD video recorder is designed to enable quick viewing access of desired programs at any time. That is, what we call ‘free timeshift viewing’. It frees viewers from restrictions on their viewing times by allowing a program to be played while the recorder continues to record other programs It allows users to: (a) View reverse playback then fast forward, or to freeze selected frames of a live TV program; (b)

Record a TV program on one channel while viewing a second program on another channel.; (c) Record a TV program while viewing a previously recorded program. It also makes it much easier for users to manage, record, view, and locate programs.”), 470-72; Sato at 6 (“The DNW-A100 Hybrid Recorder is equipped with two built-in HDDs which provide 90 minutes of record playback time. This record time can be expanded incrementally up to 6.4 hours by connecting additional HDD storage units to the SCSI-2 port. The internal storage combined with an external RAID 3 level HDD storage array, gives a higher protection of the A/V data which is a significant benefit for on-air application. With this added array, it is also possible to replay fully edited programs while simultaneously recording source material. Simultaneous recording mode and playback is also done with the internal HDD with assembled scenes that have no audio/video split.”), 6 (disclosure under “Simple Edit and Full Edit Modes”), 11 (disclosure under “Live Events with Simultaneous Recording and Editing”); Glover at 5:38-47 (“Server hard disk drive integrated circuit 12 includes a disk control circuitry 24 and a digital signal processor (DSP) 26 that may be implemented using any of a variety of interface circuitry and/or software to allow server hard disk drive 10 to couple to essentially any available network or computer. For example, disk control circuitry 24 and DSP 26 may be implemented to interface hard disk drive integrated circuit 12 with client 20 through a Universal Serial Bus (USB), a 1394 data transport bus, or any other bus or interface.”), 5:47-6:25; Mano at [0008] (“Video programs are preferably recorded on a mass storage device. Preferably, the mass storage device is a hard disk drive coupled to the television through an IEEE 1394 serial bus network.”), [0009], [0011], [0014] (“The user also has the ability to fast forward and rewind through the already recorded portion of the program while the remainder of the program is recorded. The user can also record one video broadcast while concurrently watching another previously recorded video broadcast. The concurrency of these operations is aided by the IEEE 1394 serial bus network. This bus protocol operates sufficiently fast that both the record and playback operations can occur concurrently . . . .”), [0017], figs. 2-4; Colligan 071 at 3:38-43 (“Types of interfaces for hard disks include SCSI, EIDE and 1394. Data is organized on a hard disk into cylinders, heads and sectors. Modern hard

disks have sector sizes that can be changed and no longer have anything to do with the physical geometry of the hard drive.”).

In addition, combining a ’472 Anticipatory Reference or an Appendix C Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the ’472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”), 2:46-67 (incorporating by reference prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”); AV7110 at 7, § 1 (“The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box.”); Ottesen 878 at 1:26-29 (“The present invention relates generally to communication systems, and, more particularly, to a system and method for locally controlling multimedia programming received from a remote media-on-demand communication system server.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’472 Anticipatory Reference and Appendix C Reference alone renders these elements obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of these elements and application of these elements to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add these elements to a ’472 Anticipatory Reference or an Appendix C



Reference. One of ordinary skill in the art would have been motivated to add essentially simultaneous storage and retrieval, and simultaneous storage and playback, to improve the function and utility of the same, *e.g.*, storing while viewing, as one non-limiting example based on Plaintiff's apparent interpretation of these limitations, and such a combination would have been within that person's skill. As demonstrated in the Secondary References listed above, these concepts were well-known in the art by the time of the '472 patent's claimed invention at least based on Plaintiff's apparent interpretation of these limitations, and thus, adding it to a '472 Anticipatory Reference or an Appendix C Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

## **2. "an input section for acquiring an input signal" (claim 1)**

Claim 1 requires "an input section for acquiring an input signal." To the extent TiVo contends that a '472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- So 559
- Lenihan 843
- Crump 785
- Baronetti 804
- STi5500
- STi5510
- LSI Integra Chipset
- Fujii 695

- Charles 949 (and corresponding disclosures in AViA DMX-GTX)
- MediaStation 5000
- Ryan 976
- Thomason 612
- Beard 712
- Lang 298
- Hoffberg 750
- Ottesen 878
- Patki 185
- Weaver 226
- Porter 539
- Lynch 423

MacInnisIn addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this limitation to the accused products, acquiring an input signal at an input section was well-known in the art by the time of the '472 patent's claimed

invention. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”); Baronetti 804 at 1:6-11 (“The present invention relates to processing systems for digitized audio and video signals, and in particular, to a device for receiving, transmitting and decoding compressed audio-visual streams, arranged in accordance with international standard ISO/IEC 11172, also known as ISO/MPEG-1). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add “an input section for acquiring an input signal” to a '472 Anticipatory Reference or an Appendix C Reference, amounting to applying a known technique to a known device ready for improvement to yield predictable results.

**3. “said input signal is passed to said output section as a transport stream” (claim 1)**

Claim 1 requires that the “acquired input signal” is “passed to [the] output section as a transport stream.” To the extent TiVo contends that a '472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- STi5510

- STi5500
- So 559
- Lenihan 843
- Baronetti 804
- Charles 949 (and corresponding disclosures in AViA DMX-GTX)
- Chauvel 855 (and the corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- Ryan 976
- ESS Chipset
- LSI Integra Chipset
- MediaStation 5000
- Fujii 695
- Thomason 612
- Lang 298
- Ottesen 878
- Patki 185
- Weaver 226
- Porter 539
- Lynch 423

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the

above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, passing an acquired input signal to the output section as transport stream, was a well-known design choice in the art by the time of the '472 patent's claimed invention. Indeed, the MPEG standard had been developed and successfully implemented well before the '472 patent's claimed invention. In addition, the '472 Anticipatory References, the Appendix C References and the foregoing, exemplary Secondary References seek to solve a similar problem (*e.g.*, storing, transmitting, and retrieving media using limited resources) and thus, combining them would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Charles 949 at 1:7-14 ("The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications."); Ryan 976 at 1:6-10 ("The present invention relates generally to data reception, processing and transmission according to the MPEG-2 standards and, more particularly, the present invention relates to the operation and interfacing of a transport decoder which handles an MPEG-2 format datastream."). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the

art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add this element to a '472 Anticipatory Reference or an Appendix C Reference.

#### **4. "a processor" (claim 1)**

Claim 1 requires "a processor." To the extent TiVo contends that a '472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Baronetti 804
- Ryan 976
- Charles 949 (and corresponding disclosures in AViA DMX-GTX)
- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- Owen 459
- STi5510
- STi5500
- ESS Chipset
- So 559
- Nguyen 054
- Fujii 695
- Samsung MSP
- MacInnis

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same, and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this limitation to the accused products, utilizing a processor in a media processing system was well-known by the time of the '472 patent's claimed invention. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."); Nguyen at 3:31-43 ("[M]ultimedia computing such as audio and video data compression and decompression requires many repetitive calculations on pixel arrays and strings of audio data. To perform real-time multimedia operations, a general purpose processor which manipulates scalar data . . . must operate at a high clock frequency. . . . Therefore, the vector processor can perform real-time multimedia operations at a fraction of the clock frequency required for a general purpose processor to perform the same function."). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, utilizing a processor in a media processing system would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

5. **“a decoder subsystem that decodes said transport stream” (claim 1); “said decoder further comprising a transport stream decoder/graphics subsystem” (claim 13); “said transport stream decoder/graphics subsystem comprises at least one transport stream interface . . . said transport stream interface receives said transport stream from said input section” (claim 15)**

Claim 1 requires “a decoder subsystem that decodes said transport stream, said decoder subsystem connected to said processor by a first data bus.” Relatedly, claim 13 requires “said decoder further comprising a transport stream decoder/graphics subsystem,” and claim 14, which depends from claim 13, further requires “said transport stream decoder/graphics subsystem comprises at least one transport stream interface . . . said transport stream interface receives said transport stream from said input section.” To the extent TiVo contends that a '472 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious these claim limitations under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- MacInnis 385
- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- ESS Chipset



- LSI Integra Chipset
- Owen 459
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Lenihan 843
- Fujii 695
- Lenihan 843
- Samsung MSP
- Nguyen 054
- So 559
- Toshiba TC81220F
- Crump 785

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same, and such a combination would have been within that person's skill. In particular, and to the extent Samsung understands TiVo's apparent interpretation of these limitations and application of these limitations to the accused products, a decoder subsystem receiving a transport stream, *e.g.*, via a transport interface, and outputting the decoded data, *e.g.*, to a television, was a well-known

design choice in the art by the time of the '472 patent's claimed invention. Thus, combining a '472 Anticipatory Reference or an Appendix C Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Crump 785 at 1:46-56 ("This invention relates to consumer use of what is here called the 'television space'. That is, the use of video/audio signal streams such as in the past have been distributed by broadcast over radio frequency bands or by cable distribution, or made available from video recorder/player devices such as cassette recorders or video disc player, or made available from direct, live sources such as cameras, game systems or computers. Such video/audio signal streams, whether carrying analog or digitally encoded information, have come to represent a significant resource to most consumers for information and entertainment."); Charles 949 at 1:7-14 ("The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications."). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders these elements obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of these claim limitations and application of these claim limitations to the accused products, it would have been obvious as an ordinary design choice for a decoder subsystem to receive a transport stream via a transport stream interface, and output the decoded data, *e.g.*, to a television. Thus, adding "a decoded subsystem that decodes [a] transport stream" to a '472 Anticipatory Reference or an Appendix C Reference

would have been within the skillset of one of ordinary skill and would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**6. “a media switch . . . operative to interface a plurality of system components and operates asynchronously from said processor”; “a storage subsystem connected to said media switch” (claim 1)**

Claim 1 requires “a media switch . . . operative to interface a plurality of system components and operates asynchronously from said processor.” Relatedly, claim 1 further requires “a storage subsystem connected to said media switch.” To the extent TiVo contends that a ’472 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious these claim limitations under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- Lenihan 843
- LSI Integra Chipset
- MacInnis 385
- So 559
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Baronetti 804
- Toshiba TC81220F
- Ryan 976
- Nguyen 054
- TM-2700

- Samsung MSP
- Thomason 612
- Inoue 280
- Sampat 724
- Kim 868
- O'Callaghan 263
- Obha 022
- Lang 298
- Ottesen 878
- Patki 185
- Weaver 226
- Porter 539
- Lynch 423
- Niemczyk
- Hanna
- Wang
- Krause 714
- Sasaki 756
- Goldwasser 428

In addition, to the extent TiVo contends that any of the Appendix C References fail to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the

above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of these claim limitations and application of this limitation to the accused products, a media switch mediating between different system components and operating asynchronously of the processor was a well-known design choice in the art by the time of the '472 patent's claimed invention. Thus, combining a '472 Anticipatory Reference or an Appendix C Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 ("This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers."); Lenihan 843 at 1:8-13 ("The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs."); Charles 949 at 1:7-13 ("The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications."); Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."), 2:15-30 (referencing MPEG standards). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of these claim limitations and application of these limitations to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add "a media switch . . . operative to interface a plurality of system components and operates asynchronously from [a] processor" and "a storage subsystem connected to said media switch" to a '472 Anticipatory Reference or an Appendix C Reference. One of ordinary skill in the art would have been motivated to add "a media switch . . . operative to interface a plurality of system components and operates asynchronously from [a] processor" and "a storage subsystem connected to said media switch" to improve the function and utility of the same, *e.g.*, at least in part, offloading the system's media processing needs from the processor, and such a combination would have been within that person's skill. Thus, adding these elements to a '472 Anticipatory Reference or an Appendix C Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**7. "said decoder subsystem connected to said processor by a first data bus"; "a media switch connected to said decoder subsystem by a second data bus" (claim 1)**

Claim 1 requires "said decoder subsystem connected to a processor by a first bus" and "a media switch connected to said decoder subsystem by a second data bus." To the extent TiVo contends that a '472 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious these claim limitations under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- MacInnis 385

- Philips TM-2700
- So 559
- Baronetti 804
- LSI Integra Chipset
- Lenihan 843
- Nguyen 054
- Owen 459
- Samsung MSP

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of these claim limitations and application of these limitations to the accused products, using buses to facilitate communication between components was well known in the art. In addition, as shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of these claim limitations and application of these limitations to the accused products, using two buses to connect components, *e.g.*, connecting the decoder subsystem to a media switch and to a processor (as one non-limiting example), was a well-known design choice in the art by the time of the '472 patent's claimed invention. Moreover, the '472 Anticipatory References, the Appendix C References and the foregoing, exemplary

Secondary References seek to solve a similar problem (*e.g.*, interconnection of components with different operating needs) and thus, combining a '472 Anticipatory Reference or an Appendix C Reference with any one of the above, exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Owen 459 at 1:18-24 (“The present invention relates to the field of electronic systems having a video and/or audio decompression and/or compression device, and is more specifically directed to sharing a memory interface between a video and/or audio decompression and/or compression device and another device contained in the electronic system.”); MacInnis 385 at 1:37-40 (“The present invention relates generally to integrated circuits and systems, and more particularly to a system for processing and displaying video and graphics.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of these claim limitations to the accused products, adding “[a] decoder subsystem connected to a processor by a first bus” and “a media switch connected to [the] decoder subsystem by a second data bus” to a '472 Anticipatory Reference or an Appendix C Reference would have been obvious to one of ordinary skill in the art. A person of ordinary skill would have been motivated to add these elements to a '472 Anticipatory Reference or an Appendix C Reference to improve the function and utility of the same, *e.g.*, facilitating interconnection of components with different operating needs, and such a combination would have been within that person's skill. Thus, adding these elements to a '472 Anticipatory Reference or an Appendix C Reference



would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**8. “a host controller” (claim 1)**

Claim 1 requires “a host controller.” To the extent TiVo contends that a ’472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Crump 785
- So 559
- Chauvel 855 (and associated disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- Baronetti 804
- Lenihan 843
- Owen 459
- Fujii 695
- Glover 045 (discussed below)
- Colligan 711 (discussed below)
- Mano 892 (discussed below)

In addition, to the extent TiVo contends that any of the Appendix C References fail to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement

Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, utilizing a host controller in a system was well-known in the art by the time of the '472 patent's claimed invention. *See, e.g.*, Glover at 5:38-47 ("Server hard disk drive integrated circuit 12 includes a disk control circuitry 24 and a digital signal processor (DSP) 26 that may be implemented using any of a variety of interface circuitry and/or software to allow server hard disk drive 10 to couple to essentially any available network or computer. For example, disk control circuitry 24 and DSP 26 may be implemented to interface hard disk drive integrated circuit 12 with client 20 through a Universal Serial Bus (USB), a 1394 data transport bus, or any other bus or interface."), 5:47-6:25; Mano at [0008] ("Video programs are preferably recorded on a mass storage device. Preferably, the mass storage device is a hard disk drive coupled to the television through an IEEE 1394 serial bus network."), [0009], [0011], [0014] ("The user also has the ability to fast forward and rewind through the already recorded portion of the program while the remainder of the program is recorded. The user can also record one video broadcast while concurrently watching another previously recorded video broadcast. The concurrency of these operations is aided by the IEEE 1394 serial bus network. This bus protocol operates sufficiently fast that both the record and playback operations can occur concurrently . . . ."), [0017], figs. 2-4; Colligan at

3:38-43 (“Types of interfaces for hard disks include SCSI, EIDE and 1394. Data is organized on a hard disk into cylinders, heads and sectors. Modern hard disks have sector sizes that can be changed and no longer have anything to do with the physical geometry of the hard drive.”). In addition, combining a ’472 Anticipatory Reference or an Appendix C Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique, *e.g.*, enabling communication between a host system and a device, ready for improvement to yield predictable results. Furthermore, the ’472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references. Alternatively, each ’472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, adding “a host

controller” to a ’472 Anticipatory Reference or an Appendix C Reference would have amounted to applying a known technique, *e.g.*, enabling communication between a host system and a device (as one non-limiting example), to a known device ready for improvement to yield predictable results.

**9. “a DMA controller” (claim 1)**

Claim 1 requires “a DMA controller.” To the extent TiVo contends that a ’472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- STi5500
- TM2700
- Toshiba TC81220F
- Ryan 976
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Fujii 695
- So 559
- Nguyen 054
- MacInnis 385
- Samsung MSP

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures

from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, "a DMA controller" was a well-known design choice in the art by the time of the '472 patent's claimed invention. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, AV7110 at 7, § 1 ("The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box."); Nguyen 054 at 3:31-43 ("[M]ultimedia computing such as audio and video data compression and decompression requires many repetitive calculations on pixel arrays and strings of audio data. To perform real-time multimedia operations, a general purpose processor which manipulates scalar data . . . must operate at a high clock frequency. . . . Therefore, the vector processor can perform real-time multimedia operations at a fraction of the clock frequency required for a general purpose processor to perform the same function."). Moreover, the '472 Anticipatory References, Appendix C References, and exemplary Secondary references seek to solve a similar problem (*e.g.*, efficient and/or direct access to memory) and given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the

art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add "a DMA controller" to a '472 Anticipatory Reference or an Appendix C Reference. One of ordinary skill in the art would have been motivated to add "a DMA controller" to improve the function and utility of the same, *e.g.*, facilitating efficient and/or direct access to memory, and such a combination would have been within that person's skill.

#### **10. "a bus arbiter" (claim 1)**

Claim 1 requires "a bus arbiter." To the extent TiVo contends that a '472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
  - Charles 949 (and corresponding disclosures in AViA DMX-GTX)
  - Baronetti 804
  - MacInnis 385
  - Fujii 695
  - So 559
  - STi5510
  - TM/NX-2700
  - LSI Integra chipset
  - Crump 785
  - "A Single-Chip MPEG2 Video Decoder LSI" by Demura et al. (Feb. 1994)
- (discussed below)

- U.S. Pat. No. 5,809,538 to Pollman (discussed below)
- U.S. Pat. No. 5,598,542 to Leung (discussed below)

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, "a bus arbiter" was a well-known design choice in the art by the time of the '472 patent's claimed invention. *See, e.g.*, Demura at 1 ("The second improvement is on the DRAM interface. . . . A memory bandwidth problem occurs, however, in the sharing of 64b memory bus between reading from and writing to these buffers. To solve this problem, the BU (bus arbitration unit), several FIFOs, and memories are used to avoid data conflict on the memory bus. Figure 3 shows a state diagram of the algorithm in the BU. The basic idea of this algorithm is a combination of priority assignment and polling. Five requests for the memory bus are classified into the three priority groups as shown in Figure 3 and a grant to use the memory bus is given corresponding to the priority group."); Pollman at 2:45-3:11 ("The arbiter is tuned to efficiently time-multiplex access to a DRAM among a number of client processes which are required in an Motion Pictures Experts Group (MPEG) or similar digital television delivery system. These processes include, for example, an on-screen display (OSD) graphics processor, host microprocessor interface, graphics

accelerator functions, a compressed digital audio processor, and a digital data processor. The arbiter also receives packetized data from an MPEG transport layer in the received signal for subsequent distribution to the DRAM. When access to the DRAM bus is granted by the arbiter, the selected client process will be granted a predetermined amount of time to read data from or write data to the DRAM. Those processes which are bidirectional (i.e., can either read from or write to the DRAM) will only be able to read or write in a given access period or time slot. . . . However, in accordance with the present invention, an arbiter optimizes the bandwidth allocation of a DRAM bus. . . . The arbiter is particularly applicable to MPEG digital television delivery systems.”); Leung at 2:21-25 (“A particularly complicated system is a system having a PCI bus and an MCA bus. Both the PCI bus and the MCA bus allow bus masters to assume control of that particular bus. Therefore, both of these buses have arbiters for arbitrating control of their respective buses.”).

Furthermore, the ‘472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Baronetti 804 at 1:6-11 (“The present invention relates to processing systems for digitized audio and video signals, and in particular, to a device for receiving, transmitting and decoding compressed audio-visual streams, arranged in accordance with international standard ISO/IEC 11172, also known as ISO/MPEG-1); AV7110 at 7, § 1 (“The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box.”). Moreover, the ‘472 Anticipatory References, the Appendix C References and the foregoing exemplary Secondary References seek to solve a similar problem (*e.g.*, using a bus to connect components) and thus, combining any one or more of them would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. In addition, given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.



Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add "a bus arbiter" to a '472 Anticipatory Reference or an Appendix C Reference. One of ordinary skill in the art would have been motivated to add "a bus arbiter" to improve the function and utility of the same, *e.g.*, efficient use of a bus, and such a combination would have been within that person's skill. As demonstrated in the Secondary References listed above, "a bus arbiter" was well-known in the art by the time of the '472 patent's claimed invention and thus, adding it to a '472 Anticipatory Reference or an Appendix C Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**11. "a multimedia data stream processor" (claim 1)**

Claim 1 requires "a multimedia data stream processor." To the extent TiVo contends that a '472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- Charles 949 (and corresponding disclosures in AViA DMX-GTX)
- MediaStation 5000
- Baronetti 804
- Charles 949
- Lenihan 843

- STi5510
- Toshiba TC81220F
- Ryan 976
- MacInnis 385
- So 559
- Samsung MSP
- Nguyen 054
- Neuman
- Kim 868
- O'Callaghan 263
- Obha 022
- Lang 298
- Lenihan 843
- Ottesen 878
- Patki 185
- Weaver 226
- Porter 539
- Lynch 423
- Niemczyk
- Hanna

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this limitation to the accused products, a multimedia data stream processor was a well-known design choice in the art by the time of the '472 patent's claimed invention. *See, e.g.*, Neuman at 84 ("During the parsing process, video and audio streams are separated into header and payload streams and written to independent buffers in DRAM."). In addition, combining a '472 Anticipatory Reference or an Appendix C Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique, *e.g.*, processing of media streams (as one non-limiting example based on Plaintiff's apparent interpretation of this claim limitation and application of this limitation to the accused products), to a known device ready for improvement to yield predictable results. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Lenihan 843 at 1:8-13 ("The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs."); TC81220F Datasheet ("TC81220F integrates MPEG1/2 Main Profile/Main Level video, MPEG1/2 audio decoder with a Transport Stream (TS) processor and high performance MIPS RISC microcontroller. The MPEG decoder features audio and video decoding with automatic Audio/Video synchronization logic, utilizing STC, PTS and DTS time stamps, requiring no intervention from the CPU."). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add "a multimedia data stream processor" to a '472 Anticipatory Reference or an Appendix C Reference. One of ordinary skill in the art would have been motivated to add this element to improve the function and utility of the same, *e.g.*, facilitating processing of media streams (as one non-limiting example based on Plaintiff's apparent interpretation of this claim limitation and application of this limitation to the accused products), and such a combination would have been within that person's skill. Thus, adding this element to a '472 Anticipatory References or an Appendix C Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**12. "said output section further comprising a transport interface, wherein said transport interface receives said transport stream from said input section" (claim 12)**

Claim 12 requires "said output section further comprising a transport interface, wherein said transport interface receives said transport stream from said input section." To the extent TiVo contends that a '472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- STi5510
- So 559
- Lenihan 843
- Baronetti 804
- TM-2700

- Charles 949 (and corresponding disclosures in AViA DMX-GTX)
- Chauvel 855 (and the corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- Ryan 976
- MacInnis 385
- ESS Chipset
- Fujii 695

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, receiving a transport stream via a transport interface was a well-known design choice in the art by the time of the '472 patent's claimed invention. In addition, combining a '472 Anticipatory Reference or an Appendix C Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 ("This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated

circuits and computers.”); Baronetti 804 at 1:6-11 (“The present invention relates to processing systems for digitized audio and video signals, and in particular, to a device for receiving, transmitting and decoding compressed audio-visual streams, arranged in accordance with international standard ISO/IEC 11172, also known as ISO/MPEG-1); Ryan 976 at 1:6-10 (“The present invention relates generally to data reception, processing and transmission according to the MPEG-2 standards and, more particularly, the present invention relates to the operation and interfacing of a transport decoder which handles an MPEG-2 format datastream.”); Charles 949 at 1:7-13 (“The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious as an ordinary design choice to utilize a transport stream interface to receive a transport stream. Thus, as demonstrated in the Secondary References listed above, adding “[an] output section [] compris[es] a transport interface [that] receives [the] transport stream from [an] input section” to a ’472 Anticipatory Reference or an Appendix C Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

13. **“said transport stream decoder/graphics subsystem includes any combination of: a host bridge; a memory controller; an MPEG-2 transport demultiplexer; an MPEG-2 decoder; an audio/video**

**decoder; a graphics processor; a bus bridge; or a bus controller”**  
**(claim 14)**

Claim 14, which depends from claim 13, requires that a “transport decoder/graphics subsystem includes any combination of: a host bridge; a memory controller; an MPEG-2 transport demultiplexer; an MPEG-2 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller.” To the extent TiVo contends that a ’472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- MacInnis 385
- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#),  
[AV7100 Preview](#))
- STi5510
- ESS Chipset
- LSI Integra Chipset
- Owen 459
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Lenihan 843
- Fujii 695
- Lenihan 843
- Samsung MSP
- Nguyen 054
- So 559

- Toshiba TC81220F
- Crump 785

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, components such as a host bridge, a memory controller, an MPEG-2 transport demultiplexer, an MPEG-2 decoder, an audio/video decoder, a graphics processor, a bus bridge, or a bus controller were well-known in the art by the time of the '472 patent's claimed invention. Thus, combining a '472 Anticipatory Reference or an Appendix C Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, MacInnis 385 at 1:37-40 ("The present invention relates generally to integrated circuits and systems, and more particularly to a system for processing and displaying video and graphics."); STi5510 at 7, § 1 ("The STi5510 is one of the OMEGA family of integrated multimedia decoder engines for DVB set top box systems."); Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated



circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards); Charles 949 at 1:7-13 (“The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications.”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious to add “any combination of: a host bridge; a memory controller; an MPEG-2 transport demultiplexer; an MPEG-2 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller” to a ’472 Anticipatory Reference or an Appendix C Reference because doing so would result in implementing a well-known design choice based on well-known components. Thus, adding this element to a ’472 Anticipatory Reference or an Appendix C Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

14. **“said transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet streams are stored and**

**played back though an output side of said transport stream decoder/graphics subsystem” (claim 16)**

Claim 16 requires “said transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet streams are stored and played back though an output side of said transport stream decoder/graphics subsystem.” To the extent TiVo contends that a ’472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- ESS Chipset
- Ryan 976
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Baronetti 804
- Fujii 695
- Toshiba TC81220F
- Lenihan 843
- MacInnis 385
- ESS Chipset
- LSI Integra Chipset
- Owen 459

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious

this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, by the time of the '472 patent's claimed invention, it was well-known design choice: (1) to demultiplex a transport stream into audio and video packet streams, (2) to store the demultiplexed audio and video packet streams, and (3) to play back the audio and video packet streams through an output side of the transport stream decoder/graphics subsystem. One of ordinary skill in the art would have been motivated to add this claim element to a '472 Anticipatory Reference or an Appendix C Reference to improve the function and utility of the same, *e.g.*, facilitating storage and playback of media data, and such a combination would have been within that person's skill. Thus, combining a '472 Anticipatory Reference or an Appendix C Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Baronetti 804 at 1:6-11 ("The present invention relates to processing systems for digitized audio and video signals, and in particular, to a device for receiving, transmitting and decoding compressed audio-visual streams, arranged in accordance with international standard ISO/IEC 11172, also known as ISO/MPEG-1); AV7110 at 7, § 1 ("The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box."); Lenihan 843 at 1:8-13 ("The present invention relates to recording and playback of hierarchically

organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”); Charles 949 at 1:7-13 (“The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications.”); Ryan 976 at 1:6-10 (“The present invention relates generally to data reception, processing and transmission according to the MPEG-2 standards and, more particularly, the present invention relates to the operation and interfacing of a transport decoder which handles an MPEG-2 format datastream.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references. Alternatively, each ’472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, and based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious to add this element to a ’472 Anticipatory Reference or an Appendix C Reference to improve the function and utility of the same, *e.g.*, facilitating storage and play back of media data.

**15. “a SDRAM connected to said transport stream decoder/graphics subsystem” (claim 20)**

Claim 20 requires “a SDRAM connected to said transport stream decoder/graphics subsystem.” To the extent TiVo contends that a ’472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one

or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- LSI Integra Chipset
- Lenihan 843
- Nguyen 054
- Samsung MSP
- So 559
- Chauvel 855 (and corresponding disclosures in the AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- TM/NX-2700
- Toshiba TC81220F
- STi5500
- U.S. Pat. No. 6,134,638 to Olarig & Pettey (Oct. 2000) (discussed below)

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the ’472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff’s apparent interpretation of

this claim limitation and application of this claim limitation to the accused products, connecting memory, *e.g.*, SDRAM (a well-known type of DRAM memory<sup>29</sup>), to at least a decoder subsystem was a well-known design choice in the art by the time of the '472 patent's claimed invention. In addition, the '472 Anticipatory References, Appendix C References, and exemplary Secondary References seek to solve a similar problem (*e.g.*, providing memory to facilitate the decoding process) and thus, combining a '472 Anticipatory References or an Appendix C Reference with any one of the exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, TC81220F Datasheet ("TC81220F integrates MPEG1/2 Main Profile/Main Level video, MPEG1/2 audio decoder with a Transport Stream (TS) processor and high performance MIPS RISC microcontroller. The MPEG decoder features audio and video decoding with automatic Audio/Video synchronization logic, utilizing STC, PTS and DTS time stamps, requiring no intervention from the CPU."); So 559 at 2:15-17 ("This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers."); Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."), 2:15-30 (referencing MPEG standards). Moreover, given the design needs and market pressures,

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<sup>29</sup> *See, e.g.*, Olarig at 1:66-2:12 ("Recently, memory device manufacturers have introduced synchronous DRAM ("DRAM") to alleviate the memory bottleneck that occurs using conventional DRAM devices. Synchronous DRAM devices require a clock signal as a control input signal. SDRAM devices, like DRAM chips, are commonly organized into memory banks in an array. Many computer systems available today permit as many as eight bank in the memory array. The SDRAM device derives its name from the fact that all of the input signals (or commands) are accepted by the DRAM device on the rising edge of the clock signal, and thus are 'synchronized' with the clock signal. The clock signal also allows data pipelining within the memory array and permits data to be output in a continuous stream.").

and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add this element to a '472 Anticipatory Reference or an Appendix C Reference to improve the function and utility of the same, *e.g.*, to facilitate the decoding process, and such a combination would have been within that person's skill. Therefore, adding this element to a '472 Anticipatory Reference or an Appendix C Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**16. "said processor is operative to run system software, middleware, and application software" (claim 22)**

Claim 22 requires "said processor is operative to run system software, middleware, and application software." To the extent TiVo contends that a '472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- TM/NX-2700
- Toshiba TC81220F
- Mpact2
- So 559

- Crump 785
- MacInnis 385
- Nguyen 054
- Samsung MSP
- STi5510

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, operating a layered software, *e.g.*, application software, middleware, and system software, on a processor, was a well-known design choice in the art by the time of the '472 patent's claimed invention. Thus, combining a '472 Anticipatory Reference or an Appendix C Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Purcell at 102 ("Mpact media processors enable powerful, flexible and cost-effective multimedia in a PC."); Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual



systems and improved integrated circuits used therein.”); So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”), 2:46-67 (incorporating by reference prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, operating a layered software, *e.g.*, application software, middleware, and system software, on a processor would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**17. “said system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components” (claim 23)**

Claim 23 requires “said system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components.” To the extent TiVo contends that a ’472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- So 559
- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))

- MacInnis 385
- Nguyen 054
- Samsung MSP
- STi5510

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it was well-known in the art by the time of the '472 patent's claimed invention for system software to (1) include at least an operating system kernel and device drivers and (2) to initialize and control hardware components. Thus, combining a '472 Anticipatory Reference or an Appendix C Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 ("This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers."), 2:46-67 (incorporating by reference prior art related to software including "Microsoft Corporation: publications" and the Microsoft Windows "Software Development

Kit”); MacInnis 385 at 1:37-40 (“The present invention relates generally to integrated circuits and systems, and more particularly to a system for processing and displaying video and graphics.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references. Alternatively, each ’472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, including an operating system kernel and device drivers in the overall system would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**18. “a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in said media manager” (claim 30)**

Claim 30 requires “a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in said media manager.” To the extent TiVo contends that a ’472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Coelho (see corresponding disclosure cited for the limitation requiring “a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system,” present in claims 31 and 61 of the ’389 patent)

- Griffiths 038 and related references describing the same or similar Microsoft technology including Ennis, Legault, Glass 665, Chatterjee (see corresponding disclosure cited for the limitation requiring “a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system,” present in claims 31 and 61 of the ’389 patent)
- Chauvel 855 (and associated disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5500
- So 559
- Bolash 220 (discussed below)
- Bi 875 (discussed below)
- Shin 449
- Dunnihoo 819

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the ’472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, GPIO was well-known in the art by the time of the ’472 patent’s claimed invention. *See, e.g.*, Bolash at

6:1-5, 6:15-42; Bi at Abstract, fig. 12e, 17:11-28, 18:61-19:5, 20:22-44, 31:63-32:14; Dunnihoo at 3:36-4:13, 4:27-51, 6:12-27; Shin at Abstract, [0020], [0023], [0026], [0027]. Moreover, as shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, coupling a front panel navigation cluster to a GPIO was a well-known design choice in the art by the time of the '472 patent's claimed invention. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."), 2:15-30 (referencing MPEG standards); Griffiths 038 at 1:13-16 ("The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams."); Coelho at XXIII ("Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . ."). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add "a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in said media manager" to a '472 Anticipatory Reference or an Appendix C Reference. Thus, adding this element to a '472 Anticipatory Reference or an Appendix C Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**19. “said second bus element comprises a system bus” (claim 32)**

Claim 32 requires “said second bus element comprises a system bus.” To the extent TiVo contends that a ’472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Chauvel (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- Lenihan 843
- TM/NX-2700
- Mpact2
- So 959
- MacInnis 385
- Fujii 695
- Owen 459
- Nguyen 054

In addition, to the extent TiVo contends that any of the Appendix C References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the ’472 Anticipatory References or the Appendix C References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such

a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, utilizing a system bus, *e.g.*, a PCI bus (as one non-limiting example) to connect components of a system, was well-known in the art by the time of the '472 patent's claimed invention. The '472 Anticipatory References, the Appendix C References, and the foregoing exemplary Secondary References seek to, at least in part, interconnect the different components of the system and thus, combining these references would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '472 Anticipatory References, the Appendix C References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Lenihan 843 at 1:8-13 ("The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs."); So 959 at 2:15-17 ("This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers."). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '472 Anticipatory Reference and Appendix C Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious to add this limitation to a '472 Anticipatory Reference or an Appendix C Reference to improve the function and utility of the same, *e.g.*, connect the components of the system using a system bus, and such a combination would have been within that person's skill. Thus, adding this element to a '472 Anticipatory Reference or an Appendix C Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**D. '476 Patent****1. “an input section that acquires an input signal, the input section creates a transport stream from the input signal” (claim 1)**

Claim 1 requires “an input section that acquires an input signal, the input section creates a transport stream from the input signal.” To the extent TiVo contends that a '476 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- STi5510
- STi5500
- So 559
- Lenihan 843
- Baronetti 804
- Charles 949 (and corresponding disclosures in AViA DMX-GTX)
- Chauvel 855 (and the corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- Ryan 976
- ESS Chipset
- LSI Integra Chipset
- MediaStation 5000
- Fujii 695
- Thomason 612
- Beard 712
- Lang 298
- Hoffberg 750



- Ottesen 878
- Patki 185
- Weaver 226
- Porter 539
- Lynch 423

In addition, to the extent TiVo contends that any of the prior art references for which claim charts have been provided in Appendix D (“Appendix D References”) fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the ’476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff’s apparent interpretation of this claim limitation and application of this limitation to the accused products, creating a transport stream from an acquired input signal was a well-known design choice in the art by the time of the ’476 patent’s claimed invention. Indeed, the MPEG standard had been developed and successfully implemented well before the ’476 patent’s claimed invention. Furthermore, the ’476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing and seek to solve a similar problem (*e.g.*, storing, transmitting, and retrieving media using limited resources). *See, e.g.*, So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”);

Baronetti 804 at 1:6-11 (“The present invention relates to processing systems for digitized audio and video signals, and in particular, to a device for receiving, transmitting and decoding compressed audio-visual streams, arranged in accordance with international standard ISO/IEC 11172, also known as ISO/MPEG-1); Charles 949 at 1:7-14 (“The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications.”); Ryan 976 at 1:6-10 (“The present invention relates generally to data reception, processing and transmission according to the MPEG-2 standards and, more particularly, the present invention relates to the operation and interfacing of a transport decoder which handles an MPEG-2 format datastream.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add “an input section that acquires an input signal, the input section creates a transport stream from the input signal” to a ’476 Anticipatory Reference or an Appendix D Reference, amounting to applying a known technique to a known device ready for improvement to yield predictable results.

## **2. “a processor” (claim 1)**

Claim 1 requires “a processor.” To the extent TiVo contends that a ’476 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references

(“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Baronetti 804
- Ryan 976
- Charles 949 (and corresponding disclosures in AViA DMX-GTX)
- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- Owen 459
- STi5510
- STi5500
- ESS Chipset
- So 559
- Nguyen 054
- Fujii 695
- Samsung MSP
- MacInnis

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the ’476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same, and such a combination would have been within that person’s skill. As shown in the teachings of the

foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this limitation to the accused products, utilizing a processor in a media processing system was well-known by the time of the '476 patent's claimed invention. Furthermore, the '476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."); Nguyen at 3:31-43 ("[M]ultimedia computing such as audio and video data compression and decompression requires many repetitive calculations on pixel arrays and strings of audio data. To perform real-time multimedia operations, a general purpose processor which manipulates scalar data . . . must operate at a high clock frequency. . . . Therefore, the vector processor can perform real-time multimedia operations at a fraction of the clock frequency required for a general purpose processor to perform the same function."). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, utilizing a processor in a media processing system would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

3. **"a decoder subsystem that decodes the transport stream, the decoder subsystem is communicatively connected to the processor" (claim 1); "the decoder subsystem further comprising a transport stream decoder/graphics subsystem" (claim 6); "the transport stream decoder/graphics subsystem further comprising at least one transport**

**stream interface, wherein the transport stream interface receives the transport stream from the input section” (claim 8)**

Claim 1 requires “a decoder subsystem that decodes the transport stream, the decoder subsystem is communicatively connected to the processor.” Relatedly, claim 6 requires “the decoder further comprising a transport stream decoder/graphics subsystem” and claim 8 requires “the transport stream decoder/graphics subsystem further comprising at least one transport stream interface, wherein the transport stream interface receives the transport stream from the input section.” To the extent TiVo contends that a ’476 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious these claim limitations under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- MacInnis 385
- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- ESS Chipset
- LSI Integra Chipset
- Owen 459
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Lenihan 843
- Fujii 695
- Lenihan 843
- Samsung MSP

- Nguyen 054
- So 559
- Toshiba TC81220F
- Crump 785

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same, and such a combination would have been within that person's skill. In particular, and to the extent Samsung understands TiVo's apparent interpretation of these limitations and application of these limitations to the accused products, a decoder subsystem receiving a transport stream, *e.g.*, via a transport interface, and outputting the decoded data, *e.g.*, to a television, was a well-known design choice in the art by the time of the '476 patent's claimed invention. Thus, combining a '476 Anticipatory Reference or an Appendix D Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Crump 785 at 1:46-56 ("This invention relates to consumer use of what is here called the 'television space'. That is, the use of video/audio signal streams such as in the past have been distributed by broadcast over radio frequency bands or by cable distribution, or made available from video recorder/player devices

such as cassette recorders or video disc player, or made available from direct, live sources such as cameras, game systems or computers. Such video/audio signal streams, whether carrying analog or digitally encoded information, have come to represent a significant resource to most consumers for information and entertainment.”); Charles 949 at 1:7-14 (“The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’476 Anticipatory Reference and Appendix D Reference alone renders these elements obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of these claim limitations and application of these claim limitations to the accused products, it would have been obvious as an ordinary design choice for a decoder subsystem to receive a transport stream via a transport stream interface, and output the decoded data, *e.g.*, to a television. Thus, adding “a decoded subsystem that decodes [a] transport stream” to a ’476 Anticipatory Reference or an Appendix D Reference would have been within the skillset of one of ordinary skill and would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

4. **“a media switch communicatively connected to the decoder subsystem, the media switch operative to interface a plurality of system components and operates asynchronously from the processor”; “a storage subsystem communicatively connected to the media switch” (claim 1)**

Claim 1 requires “a media switch communicatively connected to the decoder subsystem, the media switch operative to interface a plurality of system components and operates

asynchronously from the processor.” Relatedly, claim 1 further requires “a storage subsystem communicatively connected to the media switch.” To the extent TiVo contends that a ’476 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious these claim limitations under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- Lenihan 843
- LSI Integra Chipset
- MacInnis 385
- So 559
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Baronetti 804
- Toshiba TC81220F
- Ryan 976
- Nguyen 054
- TM-2700
- Samsung MSP
- Thomason 612
- Inoue 280
- Sampat 724
- Kim 868
- O’Callaghan 263
- Obha 022



- Lang 298
- Lenihan 843
- Ottesen 878
- Patki 185
- Weaver 226
- Porter 539
- Lynch 423
- Niemczyk
- Hanna
- Wang
- Krause 714
- Sasaki 756
- Goldwasser 428

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of these claim limitations and application of this limitation to the accused products, a media switch mediating between different system components and operating asynchronously of the processor was a well-known design choice in the art by the time of the '476 patent's claimed invention.

Thus, combining a '476 Anticipatory Reference or an Appendix D Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”); Charles 949 at 1:7-13 (“The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of these claim limitations and application of these limitations to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add “a media switch communicatively connected to the decoder subsystem, the media switch operative to interface a plurality of system components and operates

asynchronously from the processor” and “a storage subsystem communicatively connected to the media switch” to a ’476 Anticipatory Reference or an Appendix D Reference. One of ordinary skill in the art would have been motivated to add these components to improve the function and utility of the same, *e.g.*, at least in part, offloading the system’s media processing needs from the processor, and such a combination would have been within that person’s skill. Thus, adding these elements to a ’476 Anticipatory Reference or an Appendix D Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

#### **5. “a host controller” (claim 1)**

Claim 1 requires “a host controller.” To the extent TiVo contends that a ’476 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Crump 785
- So 559
- Chauvel 855 (and associated disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- Baronetti 804
- Lenihan 843
- Owen 459
- Fujii 695
- Glover 045 (discussed below)
- Colligan 711 (discussed below)

- Mano 892 (discussed below)

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, utilizing a host controller in a system was well-known in the art by the time of the '476 patent's claimed invention. *See, e.g.*, Glover at 5:38-47 ("Server hard disk drive integrated circuit 12 includes a disk control circuitry 24 and a digital signal processor (DSP) 26 that may be implemented using any of a variety of interface circuitry and/or software to allow server hard disk drive 10 to couple to essentially any available network or computer. For example, disk control circuitry 24 and DSP 26 may be implemented to interface hard disk drive integrated circuit 12 with client 20 through a Universal Serial Bus (USB), a 1394 data transport bus, or any other bus or interface."), 5:47-6:25; Mano at [0008] ("Video programs are preferably recorded on a mass storage device. Preferably, the mass storage device is a hard disk drive coupled to the television through an IEEE 1394 serial bus network."), [0009], [0011], [0014] ("The user also has the ability to fast forward and rewind through the already recorded portion of the program while the remainder of

the program is recorded. The user can also record one video broadcast while concurrently watching another previously recorded video broadcast. The concurrency of these operations is aided by the IEEE 1394 serial bus network. This bus protocol operates sufficiently fast that both the record and playback operations can occur concurrently . . . .”), [0017], figs. 2-4; Colligan at 3:38-43 (“Types of interfaces for hard disks include SCSI, EIDE and 1394. Data is organized on a hard disk into cylinders, heads and sectors. Modern hard disks have sector sizes that can be changed and no longer have anything to do with the physical geometry of the hard drive.”). In addition, combining a ’476 Anticipatory Reference or an Appendix D Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique, *e.g.*, enabling communication between a host system and a device, ready for improvement to yield predictable results. Furthermore, the ’476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards). Given the design needs and market pressures, and combined with a finite number of identified, predictable

solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, adding "a host controller" to a '476 Anticipatory Reference or an Appendix D Reference would have amounted to applying a known technique, *e.g.*, enabling communication between a host system and a device (as one non-limiting example), to a known device ready for improvement to yield predictable results.

#### **6. "a DMA controller" (claim 1)**

Claim 1 requires "a DMA controller." To the extent TiVo contends that a '472 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- STi5500
- TM2700
- Toshiba TC81220F
- Ryan 976
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Fujii 695

- So 559
- Nguyen 054
- MacInnis 385
- Samsung MSP

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, "a DMA controller" was a well-known design choice in the art by the time of the '476 patent's claimed invention. Furthermore, the '476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, AV7110 at 7, § 1 ("The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box."); Nguyen 054 at 3:31-43 ("[M]ultimedia computing such as audio and video data compression and decompression requires many repetitive calculations on pixel arrays and strings of audio data. To perform real-time multimedia operations, a general purpose processor which manipulates scalar data . . . must operate at a high clock frequency. . . . Therefore, the vector processor can perform real-time multimedia operations at a fraction of the clock frequency required for a general purpose processor to perform the same function."). Moreover, the '476 Anticipatory References, the

Appendix D References, and the exemplary Secondary references seek to solve a similar problem (*e.g.*, efficient and/or direct access to memory) and given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add "a DMA controller" to a '476 Anticipatory Reference or an Appendix D Reference. One of ordinary skill in the art would have been motivated to add "a DMA controller" to improve the function and utility of the same, *e.g.*, facilitating efficient and/or direct access to memory, and such a combination would have been within that person's skill.

#### **7. "a bus arbiter" (claim 1)**

Claim 1 requires "a bus arbiter." To the extent TiVo contends that a '476 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- Charles 949 (and corresponding disclosures in AViA DMX-GTX)
- Baronetti 804
- MacInnis 385
- Fujii 695
- So 559



- STi5510
- TM/NX-2700
- LSI Integra chipset
- Crump 785
- Demura (discussed below)
- Pollman 538 (discussed below)
- Leung 542 (discussed below)

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, "a bus arbiter" was a well-known design choice in the art by the time of the '476 patent's claimed invention. *See, e.g.*, Demura at 1 ("The second improvement is on the DRAM interface. . . . A memory bandwidth problem occurs, however, in the sharing of 64b memory bus between reading from and writing to these buffers. To solve this problem, the BU (bus arbitration unit), several FIFOs, and memories are used to avoid data conflict on the memory bus. Figure 3 shows a state diagram of the algorithm in the BU. The basic idea of this algorithm is a combination of priority assignment and polling. Five requests for the memory bus are classified into the three

priority groups as shown in Figure 3 and a grant to use the memory bus is given corresponding to the priority group.”); Pollman at 2:45-3:11 (“The arbiter is tuned to efficiently time-multiplex access to a DRAM among a number of client processes which are required in an Motion Pictures Experts Group (MPEG) or similar digital television delivery system. These processes include, for example, an on-screen display (OSD) graphics processor, host microprocessor interface, graphics accelerator functions, a compressed digital audio processor, and a digital data processor. The arbiter also receives packetized data from an MPEG transport layer in the received signal for subsequent distribution to the DRAM. When access to the DRAM bus is granted by the arbiter, the selected client process will be granted a predetermined amount of time to read data from or write data to the DRAM. Those processes which are bidirectional (i.e., can either read from or write to the DRAM) will only be able to read or write in a given access period or time slot. . . . However, in accordance with the present invention, an arbiter optimizes the bandwidth allocation of a DRAM bus. . . . The arbiter is particularly applicable to MPEG digital television delivery systems.”); Leung at 2:21-25 (“A particularly complicated system is a system having a PCI bus and an MCA bus. Both the PCI bus and the MCA bus allow bus masters to assume control of that particular bus. Therefore, both of these buses have arbiters for arbitrating control of their respective buses.”).

Furthermore, the ‘476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Baronetti 804 at 1:6-11 (“The present invention relates to processing systems for digitized audio and video signals, and in particularly, to a device for receiving, transmitting and decoding compressed audio-visual streams, arranged in accordance with international standard ISO/IEC 11172, also known as ISO/MPEG-1); AV7110 at 7, § 1 (“The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box.”). Moreover, the ‘476 Anticipatory References, the Appendix D References, and the foregoing exemplary Secondary References seek to solve a similar problem (*e.g.*, using a bus to connect components) and thus, combining any one or more of them would have amounted to applying a

known technique to a known device ready for improvement to yield predictable results. In addition, given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add "a bus arbiter" to a '476 Anticipatory Reference or an Appendix D Reference. One of ordinary skill in the art would have been motivated to add "a bus arbiter" to improve the function and utility of the same, *e.g.*, efficient use of a bus, and such a combination would have been within that person's skill. As demonstrated in the Secondary References listed above, "a bus arbiter" was well-known in the art by the time of the '476 patent's claimed invention and thus, adding it to a '476 Anticipatory Reference or an Appendix D Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

#### **8. "a multimedia data stream processor" (claim 1)**

Claim 1 requires "a multimedia data stream processor." To the extent TiVo contends that a '476 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- Charles 949 (and corresponding disclosures in AViA DMX-GTX)

- MediaStation 5000
- Baronetti 804
- Charles 949
- Lenihan 843
- STi5510
- Toshiba TC81220F
- Ryan 976
- MacInnis 385
- So 559
- Samsung MSP
- Nguyen 054
- Neuman
- Kim 868
- O'Callaghan 263
- Obha 022
- Lang 298
- Lenihan 843
- Ottesen 878
- Patki 185
- Weaver 226
- Porter 539
- Lynch 423
- Niemczyk
- Hanna

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious

this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this limitation to the accused products, a multimedia data stream processor was a well-known design choice in the art by the time of the '476 patent's claimed invention. In addition, combining a '476 Anticipatory Reference or an Appendix D Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique, *e.g.*, processing of media streams (as one non-limiting example based on Plaintiff's apparent interpretation of this claim limitation and application of this limitation to the accused products), to a known device ready for improvement to yield predictable results. Furthermore, the '476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Lenihan 843 at 1:8-13 ("The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs."); TC81220F Datasheet ("TC81220F integrates MPEG1/2 Main Profile/Main Level video, MPEG1/2 audio decoder with a Transport Stream (TS) processor and high performance MIPS RISC microcontroller. The MPEG decoder features audio and video decoding with automatic Audio/Video synchronization logic, utilizing STC, PTS and DTS time stamps, requiring no intervention from the CPU."). Given the design needs and market pressures, and

combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add "a multimedia data stream processor" to a '476 Anticipatory Reference or an Appendix D Reference. One of ordinary skill in the art would have been motivated to add this element to improve the function and utility of the same, *e.g.*, facilitating processing of media streams (as one non-limiting example based on Plaintiff's apparent interpretation of this claim limitation and application of this limitation to the accused products), and such a combination would have been within that person's skill. Thus, adding this element to a '476 Anticipatory Reference or an Appendix D Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

9. **"wherein multimedia data are stored on the storage subsystem and retrieved from the storage subsystem essentially simultaneously"; "a system for the simultaneous storage and retrieval of multimedia data" (claim 1)**

Claim 1 requires "multimedia data are stored on the storage subsystem and retrieved from the storage subsystem essentially simultaneously," and to the extent the preamble is limiting, claim 1 also requires "simultaneous storage and retrieval of multimedia data." To the extent TiVo contends that a '476 Anticipatory Reference fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- So 559

- Lenihan 843
- AV 7110 Specification (and related disclosures in Chauvel 855)
- Nguyen 054
- Logan 551
- Kageyama
- Sato (discussed below)
- Glover 045 (discussed below)
- Colligan 711 (discussed below)
- Mano 892 (discussed below)
- Krause 714
- Sampat 724
- Lang 298
- Sasaki 756
- Ottesen 878
- Goldwasser 428
- Inoue 881
- Camhi 444
- Schaefer 000
- Thomason 612

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '476 Anticipatory References or the Appendix D References with any one or more of the

above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of these elements and application of these elements to the accused products, the above limitations were well-known in the art by the time of the '476 patent's claimed invention. *See, e.g.*, Kageyama at § 3, 470 ("To better meet the needs of users, the proposed DVD video recorder is designed to enable quick viewing access of desired programs at any time. That is, what we call 'free timeshift viewing'. It frees viewers from restrictions on their viewing times by allowing a program to be played while the recorder continues to record other programs. It allows users to: (a) View reverse playback then fast forward, or to freeze selected frames of a live TV program; (b) Record a TV program on one channel while viewing a second program on another channel.; (c) Record a TV program while viewing a previously recorded program. It also makes it much easier for users to manage, record, view, and locate programs."), 470-72-72; Sato at 6 ("The DNW-A100 Hybrid Recorder is equipped with two built-in HDDs which provide 90 minutes of record playback time. This record time can be expanded incrementally up to 6.4 hours by connecting additional HDD storage units to the SCSI-2 port. The internal storage combined with an external RAID 3 level HDD storage array, gives a higher protection of the A/V data which is a significant benefit for on-air application. With this added array, it is also possible to replay fully edited programs while simultaneously recording source material. Simultaneous recording mode and playback is also done with the internal HDD with assembled scenes that have no audio/video split."), 6 (disclosure under "Simple Edit and Full Edit Modes"), 11 (disclosure under "Live Events with Simultaneous Recording and Editing"); Glover at 5:38-47 ("Server hard disk drive integrated circuit 12 includes a disk control circuitry 24 and a digital signal processor (DSP) 26 that may be implemented using any of a variety of interface circuitry and/or software to allow server hard disk drive 10 to couple to essentially any available network or computer. For example, disk control circuitry 24 and DSP 26 may be implemented to interface hard disk drive integrated circuit 12 with client 20 through a Universal Serial Bus (USB), a 1394 data transport



bus, or any other bus or interface.”), 5:47-6:25; Mano at [0008] (“Video programs are preferably recorded on a mass storage device. Preferably, the mass storage device is a hard disk drive coupled to the television through an IEEE 1394 serial bus network.”), [0009], [0011], [0014] (“The user also has the ability to fast forward and rewind through the already recorded portion of the program while the remainder of the program is recorded. The user can also record one video broadcast while concurrently watching another previously recorded video broadcast. The concurrency of these operations is aided by the IEEE 1394 serial bus network. This bus protocol operates sufficiently fast that both the record and playback operations can occur concurrently . . . .”), [0017], figs. 2-4; Colligan at 3:38-43 (“Types of interfaces for hard disks include SCSI, EIDE and 1394. Data is organized on a hard disk into cylinders, heads and sectors. Modern hard disks have sector sizes that can be changed and no longer have anything to do with the physical geometry of the hard drive.”).

In addition, combining a ’476 Anticipatory Reference or an Appendix D Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the ’476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”), 2:46-67 (incorporating by reference prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”); AV7110 at 7, § 1 (“The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box.”); Ottesen 878 at 1:26-29 (“The present invention relates

generally to communication systems, and, more particularly, to a system and method for locally controlling multimedia programming received from a remote media-on-demand communication system server.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’476 Anticipatory Reference and Appendix D Reference alone renders these elements obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of these elements and application of these elements to the accused products, it would have been obvious in the view of one of ordinary skill in the art to add these elements to a ’476 Anticipatory Reference or an Appendix D Reference. One of ordinary skill in the art would have been motivated to add essentially simultaneous storage and retrieval or simultaneous storage and retrieval to improve the function and utility of the same, *e.g.*, storing while viewing, as one non-limiting example based on Plaintiff’s apparent interpretation of these limitations, and such a combination would have been within that person’s skill. As demonstrated in the Secondary References listed above, these concepts were well-known in the art by the time of the ’476 patent’s claimed invention at least based on Plaintiff’s apparent interpretation of these limitations, and thus, adding it to a ’476 Anticipatory Reference or an Appendix D Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**10. “the transport stream decoder/graphics subsystem includes at least one of: a host bridge; a memory controller; an MPEG-3 transport demultiplexer; an MPEG-3 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller” (claim 7)**

Claim 7, which depends from claim 6, requires that a “transport stream decoder/graphics subsystem includes at least one of: a host bridge; a memory controller; an MPEG-3 transport demultiplexer; an MPEG-3 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller.” To the extent TiVo contends that a ’476 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures

from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- MacInnis 385
- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- ESS Chipset
- LSI Integra Chipset
- Owen 459
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Lenihan 843
- Fujii 695
- Lenihan 843
- Samsung MSP
- Nguyen 054
- So 559
- Toshiba TC81220F
- Crump 785

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement

Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, *e.g.*, applying this claim limitation requiring "MPEG-3" components in the same manner as asserted claim 14 of the '472 patent requiring "MPEG-2" components, components such as a host bridge, a memory controller, an MPEG-2 transport demultiplexer, an MPEG-2 decoder, an audio/video decoder, a graphics processor, a bus bridge, or a bus controller were well-known in the art by the time of the '476 patent's claimed invention. Thus, combining a '476 Anticipatory Reference or an Appendix D Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, MacInnis 385 at 1:37-40 ("The present invention relates generally to integrated circuits and systems, and more particularly to a system for processing and displaying video and graphics."); STi5510 at 7, § 1 ("The STi5510 is one of the OMEGA family of integrated multimedia decoder engines for DVB set top box systems."); Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."), 2:15-30 (referencing MPEG standards); Charles 949 at 1:7-13 ("The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video, audio, graphics

and input/output processing functions and is particularly well-suited for use in set top box applications.”); Lenihan 843 at 1:8-13 (“The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs.”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, *e.g.*, applying this claim limitation requiring “MPEG-3” components in the same manner as asserted claim 14 of the ’472 patent requiring “MPEG-2” components, it would have been obvious to add “any combination of: a host bridge; a memory controller; an MPEG-2 transport demultiplexer; an MPEG-2 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller” to a ’476 Anticipatory Reference or an Appendix D Reference because doing so would result in implementing a well-known design choice based on well-known components. Thus, adding this element to a ’476 Anticipatory Reference or an Appendix D Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**11. “the transport stream is demultiplexed into audio and video packet streams, wherein the audio and video packet streams are stored and played back through an output side of the transport stream decoder/graphics subsystem” (claim 9)**

Claim 9 requires “the transport stream is demultiplexed into audio and video packet streams, wherein the audio and video packet streams are stored and played back through an output side of the transport stream decoder/graphics subsystem.” To the extent TiVo contends that a ’476 Anticipatory Reference fails to disclose this element, such reference(s) can be

combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- ESS Chipset
- Ryan 976
- Charles 949 (and corresponding disclosures in AViA GTX-DMX)
- Baronetti 804
- Fujii 695
- Toshiba TC81220F
- Lenihan 843
- MacInnis 385
- ESS Chipset
- LSI Integra Chipset
- Owen 459

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the ’476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such

a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, by the time of the '476 patent's claimed invention, it was well-known design choice: (1) to demultiplex a transport stream into audio and video packet streams, (2) to store the demultiplexed audio and video packet streams, and (3) to play back the audio and video packet streams through an output side of the transport stream decoder/graphics subsystem. One of ordinary skill in the art would have been motivated to add this claim element to a '476 Anticipatory Reference or an Appendix D Reference to improve the function and utility of the same, *e.g.*, facilitating storage and playback of media data, and such a combination would have been within that person's skill. Thus, combining a '476 Anticipatory Reference or an Appendix D Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

Furthermore, the '476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Baronetti 804 at 1:6-11 ("The present invention relates to processing systems for digitized audio and video signals, and in particular, to a device for receiving, transmitting and decoding compressed audio-visual streams, arranged in accordance with international standard ISO/IEC 11172, also known as ISO/MPEG-1); AV7110 at 7, § 1 ("The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box."); Lenihan 843 at 1:8-13 ("The present invention relates to recording and playback of hierarchically organized audio-video signals. More particularly, the present invention relates to recording and playback of transport packets in a transport stream which includes multiplexed audio and video data streams from one or more data sources or programs."); Charles 949 at 1:7-13 ("The present invention relates generally to video, audio, graphics, input/output and other processing functions in set top box applications. More particularly, the present invention relates to a processing system with an application specific integrated circuit (ASIC) processor which provides video,

audio, graphics and input/output processing functions and is particularly well-suited for use in set top box applications.”); Ryan 976 at 1:6-10 (“The present invention relates generally to data reception, processing and transmission according to the MPEG-2 standards and, more particularly, the present invention relates to the operation and interfacing of a transport decoder which handles an MPEG-2 format datastream.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each ’476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, and based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious to add this element to a ’476 Anticipatory Reference or an Appendix D Reference to improve the function and utility of the same, *e.g.*, facilitating storage and play back of media data.

**12. “a SDRAM connected to the transport stream decoder/graphics subsystem” (claim 10)**

Claim 10 requires “a SDRAM connected to the transport stream decoder/graphics subsystem.” To the extent TiVo contends that a ’476 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- LSI Integra Chipset
- Lenihan 843



- Nguyen 054
- Samsung MSP
- So 559
- Chauvel 855 (and corresponding disclosures in the AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5510
- TM/NX-2700
- Toshiba TC81220F
- STi5500
- Olarig 638 (discussed below)

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, connecting memory, *e.g.*, SDRAM (a well-known type of DRAM memory<sup>30</sup>), to at least a decoder

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<sup>30</sup> See, *e.g.*, Olarig at 1:66-2:12 ("Recently, memory device manufacturers have introduced synchronous DRAM ("DRAM") to alleviate the memory bottleneck that occurs using conventional DRAM devices. Synchronous DRAM devices require a clock signal as a control input signal. SDRAM devices, like DRAM chips, are commonly organized into memory banks in an array. Many computer systems available today permit as many as eight bank in the memory

subsystem was a well-known design choice in the art by the time of the '476 patent's claimed invention. In addition, the '476 Anticipatory References, Appendix D References, and exemplary Secondary References seek to solve a similar problem (*e.g.*, providing memory to facilitate the decoding process) and thus, combining a '476 Anticipatory Reference or an Appendix D Reference with any one of the exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, TC81220F Datasheet ("TC81220F integrates MPEG1/2 Main Profile/Main Level video, MPEG1/2 audio decoder with a Transport Stream (TS) processor and high performance MIPS RISC microcontroller. The MPEG decoder features audio and video decoding with automatic Audio/Video synchronization logic, utilizing STC, PTS and DTS time stamps, requiring no intervention from the CPU."); So 559 at 2:15-17 ("This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers."); Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."), 2:15-30 (referencing MPEG standards). Moreover, given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it would have been obvious in the

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array. The SDRAM device derives its name from the fact that all of the input signals (or commands) are accepted by the DRAM device on the rising edge of the clock signal, and thus are "synchronized" with the clock signal. The clock signal also allows data pipelining within the memory array and permits data to be output in a continuous stream.").

view of one of ordinary skill in the art to add this element to a '476 Anticipatory Reference or an Appendix D Reference to improve the function and utility of the same, *e.g.*, to facilitate the decoding process, and such a combination would have been within that person's skill.

Therefore, adding this element to a '476 Anticipatory Reference or an Appendix D Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**13. “the processor is operative to run system software, middleware, and application software” (claim 11)**

Claim 11 requires “the processor is operative to run system software, middleware, and application software.” To the extent TiVo contends that a '476 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- TM/NX-2700
- Toshiba TC81220F
- Mpact2
- So 559
- Crump 785
- MacInnis 385
- Nguyen 054
- Samsung MSP
- STi5510

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, operating a layered software, *e.g.*, application software, middleware, and system software, on a processor, was a well-known design choice in the art by the time of the '476 patent's claimed invention. Thus, combining a '476 Anticipatory Reference or an Appendix D Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

Furthermore, the '476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Purcell at 102 ("Mpact media processors enable powerful, flexible and cost-effective multimedia in a PC."); Chauvel 855 at 1:28-31 ("This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein."); So 559 at 2:15-17 ("This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers."), 2:46-67 (incorporating by reference prior art related to software including "Microsoft Corporation: publications" and the Microsoft Windows "Software Development Kit"). Given the design needs and market pressures, and

combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, operating a layered software, *e.g.*, application software, middleware, and system software, on a processor would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**14. "a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in the media switch" (claim 13)**

Claim 13 requires "a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in the media switch." To the extent TiVo contends that a '476 Anticipatory Reference fails to disclose this element, such reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references ("Secondary References") to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered:

- Coelho (see corresponding disclosure cited for the limitation requiring "a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system," present in claims 31 and 61 of the '389 patent)
- Griffiths 038 and related references describing the same or similar Microsoft technology including Ennis, Legault, Glass 665, Chatterjee (see corresponding disclosure cited for the limitation requiring "a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system," present in claims 31 and 61 of the '389 patent)

- Chauvel 855 (and associated disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- STi5500
- So 559
- Bolash 220 (discussed below)
- Bi 875 (discussed below)
- Shin 449 (discussed below)
- Dunnihoo (discussed below)

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo's Infringement Contentions and apparent claim constructions and application of the claims to Samsung's accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the '476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, GPIO was well-known in the art by the time of the '476 patent's claimed invention. *See, e.g.*, Bolash at 6:1-5, 6:15-42; Bi at Abstract, fig. 12e, 17:11-28, 18:61-19:5, 20:22-44, 31:63-32:14; Dunnihoo at 3:36-4:13, 4:27-51, 6:12-27; Shin at Abstract, [0020], [0023], [0026], [0027]. Moreover, as shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, coupling a front panel navigation cluster to a GPIO was a well-known design choice in the art by the time of the '476 patent's claimed invention. Furthermore, the

'476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards); Griffiths 038 at 1:13-16 (“The present invention relates generally to processing of multimedia data and, more particularly, is directed to constructing a graph by connecting filter components to process multimedia data streams.”); Coelho at XXIII (“Who Should Read This Book. Ok so, who do we think we could help? It was clear to us that our readers would . . . understand multimedia concepts and terminology [and] be familiar with programming with C, C++ . . .”). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, it would have been obvious in the view of one of ordinary skill in the art to add “a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in the media switch” to a '476 Anticipatory Reference or an Appendix D Reference. Thus, adding this element to a '476 Anticipatory Reference or an Appendix D Reference would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

15. **“the system software includes at least: an operating system kernel and device drivers, the system software operative to initialize and control hardware components” (claim 14)**

Claim 14 requires “the system software includes at least: an operating system kernel and device drivers, the system software operative to initialize and control hardware components.” To the extent TiVo contends that a '476 Anticipatory Reference fails to disclose this element, such

reference(s) can be combined with the corresponding disclosures from any one or more of the following prior art references (“Secondary References”) to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered:

- So 559
- Chauvel 855 (and corresponding disclosures in AV7110, [AV7110 Preview](#), [AV7100 Preview](#))
- MacInnis 385
- Nguyen 054
- Samsung MSP
- STi5510

In addition, to the extent TiVo contends that any of the Appendix D References fails to disclose these elements, such reference(s) can be combined with the corresponding disclosures from any one or more of the above-described exemplary Secondary References to render obvious this claim limitation under 35 U.S.C. § 103(a), at least based on TiVo’s Infringement Contentions and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered.

One of ordinary skill in the art would have been motivated to combine any one or more of the ’476 Anticipatory References or the Appendix D References with any one or more of the above exemplary Secondary References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing exemplary Secondary References, and based on Plaintiff’s apparent interpretation of this claim limitation and application of this claim limitation to the accused products, it was well-known in the art by the time of the ’476 patent’s claimed invention for system software to (1) include at least an operating system kernel and device drivers and (2) to initialize and control hardware components. Thus, combining a ’476 Anticipatory Reference or an Appendix D



Reference with any one of the above exemplary Secondary References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, the '476 Anticipatory References, the Appendix D References, and the exemplary Secondary References are in the same field of endeavor, *e.g.*, media processing. *See, e.g.*, So 559 at 2:15-17 (“This invention generally relates to improved integrated circuits, computer systems, software products, and processes of operating integrated circuits and computers.”), 2:46-67 (incorporating by reference prior art related to software including “Microsoft Corporation: publications” and the Microsoft Windows “Software Development Kit”); MacInnis 385 at 1:37-40 (“The present invention relates generally to integrated circuits and systems, and more particularly to a system for processing and displaying video and graphics.”); Chauvel 855 at 1:28-31 (“This invention generally relates to audio-visual systems and integrated circuits used therein, and more particularly, to improved audio-visual systems and improved integrated circuits used therein.”), 2:15-30 (referencing MPEG standards). Given the design needs and market pressures, and combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

Alternatively, each '476 Anticipatory Reference and Appendix D Reference alone renders this element obvious, in view of the knowledge and skill of one of ordinary skill in the art. That is, based on Plaintiff's apparent interpretation of this claim limitation and application of this claim limitation to the accused products, including an operating system kernel and device drivers in the overall system would have amounted to applying a known technique to a known device ready for improvement to yield predictable results.

**E. Additional Combinations and Motivation/Reasons to Combine**

To the extent not anticipated, the asserted claims represent no more than simple and obvious substitution of one known element for another or the mere obvious application of a known technique to a piece of prior art ready for the improvement. Samsung further believes

that no showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have no unexpected results, and at most would simply represent a known alternative to one of skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1739-40 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 1742. As the Supreme Court has explained: "[A]s progress beginning from higher levels of achievement is expected in the normal course, the results of ordinary innovation are not the subject of exclusive rights under the patent laws. Were it otherwise patents might stifle, rather than promote, the progress of useful arts." *Id.*

One or more combinations of the prior art references identified above pursuant to P.R. 3-3(a) would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above pursuant to P.R. 3-3(a) because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. In addition, the combination of the prior art references identified above pursuant to P.R. 3-3(a) would have been obvious because the combination represents the known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above pursuant to P.R. 3-3(a) includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the asserted claims; the existence of a known need or problem in the field of the endeavor at the time of the invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

For example, Coelho, Griffiths 038, Ennis, Legault, Glass 665, and Chatterjee all disclose interrelated teachings describing object-oriented software architectures for processing multimedia data streams like Microsoft's ActiveMovie and DirectShow APIs and Software Development Kits. As such, a person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings of these prior art references because each reference describes aspects of the same or similar technology (collectively, "ActiveMovie/DirectShow Art"). *Compare, e.g.,* Coelho at 82 ("DirectShow defines three major types of filters: source, transform, and rendering. A source filter has no input pins and has one or more output pins. Typically a source filter is responsible for reading the raw data from a source file, network, or any other media."), *with* Griffiths 038 at 10:47-54 ("In general, filters components can be categorized into one of three filter types: source, transform, or renderer. . . . A source filter 210, which accepts and reads data from a source 216, such as a file stored on a storage medium or information fed via a satellite feed, and introduces it into the filter graph 203.").

Similarly, AV7110, [AV7110 Preview](#), [AV7100 Preview](#), Chauvel 855, Gass, and So 559 all disclose similar multimedia processing hardware and software technologies from Texas

Instruments for implementation in set-top boxes and other multimedia computing applications.

*Compare, e.g.,* AV7110 at 7 (“The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECD), an MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/ PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infrared (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.”), *with* Chauvel 855 at Abstract (“An improved audio-visual circuit is provided that includes a transport packet parsing circuit for receiving a transport data packet stream, a CPU circuit for initializing said integrated circuit and for processing portions of said data packet stream, a ROM circuit for storing data, a RAM circuit for storing data, an audio decoder circuit for decoding audio portions of said data packet stream, a video decoder circuit for decoding video portions of said data packet stream, an NTSC/PAL encoding circuit for encoding video portions of said data packet stream, an OSD coprocessor circuit for processing OSD portions of said data packets, a traffic controller circuit moving portions of said data packet stream between portions of said integrated circuit, an extension bus interface circuit, a P1394 interface circuit, a communication coprocessors circuit, an address bus connected to said circuits, and a data bus connected to said circuits”). As such, a person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings of these prior art references because each reference describes aspects of the same hardware components like systems-on-a-

chip or related software for controlling multimedia data stream processing (collectively, “Texas Instruments Art”).

As another example, Soo, Bescós, Kaleido, Wolf, Sampat 724, Gibbs, Miller, and Coulson also disclose similar object-oriented multimedia processing architectures. As such, a person of ordinary skill in the art at the time of the invention would have been motivated to combine the teachings of these prior art references because each reference describes overlapping software architectures addressing efficient processing of multimedia data streams (collectively, “Object-Oriented Multimedia Processing Architecture Art”). *Compare, e.g.*, Soo at 29 (“NetPlay itself is composed of components implemented in C++ called MediaObj objects. The output of an object can be connected to the input of another to build a media pipeline through which the video system logically flows.”), with Bescós at 136 (“At this point, we present a basic model based on several stream-based models and implementations on multimedia data flows, and built on the basis of the source-stream-sink paradigm.”).

As another example, a person of ordinary skill in the art would have been motivated to combine the teachings of Ryan 976, LSI Integra, ESS Chipset, and Fujii 695, all of which disclose similar modular multimedia processing architectures for, *e.g.*, set-top box, DVD, and PC applications (collectively, “Modular Hardware Architecture Art”). *Compare, e.g.*, Ryan 976 at Abstract (“A transport decoder 110, for receiving and processing a transport data stream using MPEG-2 formats, includes connections to a physical layer channel interface (channel interface) 112, a buffer memory 114, a host microprocessor 116, audio and video decoders 118/120, and clock signal circuitry 122.”), *with* Fujii 695 at 11:8-19 (“In FIG. 17, reference numeral 200 represents a demodulator, reference numeral 201 represents an error correction demodulator, reference numeral 202 represents a channel. demultiplexer, reference numeral 203 represents a

random access memory (hereinafter called RAM), reference numeral 204 represents a microcomputer, reference numeral 205 represents a program memory, reference numeral 206 represents an on-screen display processor (hereinafter called an OSD processor), reference numeral 207 represents a video decoder, and reference numeral 208 represents an audio decoder. In FIG. 17, a tuner and other blocks of the reception apparatus for compressed video and audio data are not shown because they are the same as FIGS. 1 and 11.”).

Similarly, TM-2700, STi5500, STi5510, Toshiba TC81220F, and MacInnis 385 all disclose integrated multimedia processing hardware architectures for, *e.g.*, set-top box, DVD, and PC applications (“Integrated Hardware Architecture Art”). *Compare, e.g.*, STi5510 at 7 (“The STi5510 is one of the OMEGA family of integrated multimedia decoder engines for DVB set top box systems. It offers a high level of integration by reducing the complete set-top box decoding chain from transport demultiplexing to PAL/NTSC/SECAM encoder onto one chip. At the same time it dramatically enhances CPU and graphics performance, and cuts down total system memory cost.”), *with* Toshiba TC81220F Datasheet at 1 (“TC81220F combines Toshiba’s MPEG1/2 audio and MPEG2 video decoder, Transport Stream (TS) processor, and a high performance 32-bit RISC MIPS compatible R3900 CPU into one integrated device”). As a further example, MediaStation 5000, Baronetti 804, Lenihan 843, Owen 459, Nguyen 054, and Samsung MSP all disclose similar multimedia processing architectures with teachings in the desktop/personal computer (PC) context (“Multimedia Computer Architecture Art”). *Compare, e.g.*, Baronetti 804 at 7:7-12 (“In addition to carrying out reception and decoding functions, the device can also operate as a storage device or as a transmitter (or playback unit) of MPEG streams. The device can be used in applications such as access to data bases of multimedia information, video-on-demand services, etc.”), *with* Lenihan 843 at 4:9-14 (“It should also be

recognized that the invention is well-suited for use in a variety of applications, including terrestrial, CATV and satellite broadcasting and telephony-based multimedia services. Other suitable applications include MPEG video recorders, optical disk based digital recording systems and personal computers equipped with tape drives or other recording mechanisms”).

A person of ordinary skill in the art would have been motivated to combine the teachings of these individual groups of prior art because they all address multimedia data processing and other overlapping technologies. For example, a person of ordinary skill in the art would have been motivated to combine the teachings of the Object-Oriented Multimedia Processing Architecture Art with the similar object-oriented designs and teachings of the ActiveMovie/DirectShow Art. *Compare, e.g.,* Bescós at 139 (“The sink and the source are independent functional units (both also defined as C++ classes) that make use of the available services (communication, presentation, information, management,... ) to throw or extract data to or from their location respectively.”), *with* Coelho at 82 (“What’s nice about the filter graph model is that you can easily replace one of the filters without even touching the remainder of the graph. For example, you can easily replace the source filter that reads the MPEG file from a hard disk or a CD-ROM with another source filter that reads it off the Internet or from a digital satellite link. This is a big win for developers since they only need to implement and distribute one filter rather than the entire filter graph or an entire VFW driver.”).

As another example, a person of ordinary skill in the art would have been motivated to combine the object-oriented architecture and other teachings of the ActiveMovie/DirectShow Art with the hardware architecture and other teachings of the Texas Instruments Art. Indeed, So 559 discloses a system architecture in which Microsoft ActiveMovie/DirectShow is implemented on a Texas Instruments hardware architecture. *See, e.g.,* So 559 at figs. 92-93, 72:21-74:3. For

similar reasons, a person of ordinary skill in the art would have been motivated to combine the teachings of the Object-Oriented Multimedia Processing Architecture Art with the hardware architecture and other teachings of the Texas Instruments Art. *Compare, e.g.,* Bescós at 143 (“Monomedia Stream Object[:] . . . Allocates resources to fulfill source-sink data transmission requirements (rate, delay, jitter, buffer sizes, ...)[:] Implements flow control handling functions.”), *with* Chauvel 855 at 18:66-19:11 (“The traffic controller module 310 manages interrupt requests and authorizes and manages DMA transfers. It provides SDRAM interface and manages the extension bus 300. It provides memory access protection and manages the data flow between processors and memories such as: TPP/DES to/from internal Data RAM; Data RAM to/from extension bus; SDRAM to OSD; OSD to/from Data RAM; audio/video decoder to/from SD RAM; and SD RAM to/from Data RAM. It also generates chip selects (CS) for all the internal modules and devices on the extension bus 300 and generates programmable wait states for devices on the extension bus. It also provides 3 breakpoint registers and 64 32-bit patch RAM”).

As another example, a person of ordinary skill in the art would have been motivated to combine the teachings of the Texas Instruments Art with the teachings of the Modular Hardware Architecture Art because they all address related and overlapping hardware architectures for multimedia processing systems. *Compare, e.g.,* AV7110 at 7 (“The TMS320AV7110 Integrated Set-top Box Decoder is the major component of a Digital Video Broadcast (DVB) Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECD), an MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infrared



(IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.”), *with* LSI Integra Chipset at L64007 Manual at 1-3 (“The L64007 MPEG-2 Transport Demultiplexer was designed for use with upstream and downstream LSI Logic decoders. The L64007 input channel decoder interface allows the L64007 to connect seamlessly to LSI Logic devices such as the L64704 Single-Chip Direct Broadcast Satellite (DBS) Receiver. The audio/video output interface port allows seamless connection to LSI Logic audio and video decoders, such as the L64002 and L64005 MPEG-2 decoders.”). For similar reasons, a person of ordinary skill in the art would have been motivated to combine the teachings of the Texas Instruments Art with the teachings of the Integrated Hardware Architecture Art or related Multimedia Computer Architecture Art.

Thus, the motivation to combine the teachings of the prior art references disclosed herein is found in the references themselves and: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art, (4) the fact that the prior art is generally directed toward computer operating systems and environments, and (5) the predictable results obtained in combining the different elements of the prior art. Additionally, one would be motivated to address at least the alleged problems or achieve the purported objectives identified in the description of the TiVo patents-in-suit.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim because every element of each dependent claim was known by a person of ordinary skill at the

time of the alleged invention, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation.

Accordingly, Samsung contends that each asserted claim would have been obvious not only by the combinations explicitly defined in these contentions, but also by any combination of references that renders obvious an asserted claim.

#### **F. General Admissions**

Each of the TiVo patents-in-suit make general admissions concerning the state of the respective art, and Samsung may rely on those admissions to demonstrate the invalidity of the asserted claims. These admissions include, among other things, acknowledging known problems and needs in the prior art and the advantages of prior art techniques and elements. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417-422 (2007). For example, the specifications of the '389, '472, and '476 patents admit that the prior art, including Logan 551 (U.S. Patent No. 5,371,551 to Logan), already disclosed a "method for concurrent video recording and playback" using "digital computer systems," including a "microprocessor controlled broadcast and playback device." *See, e.g.*, '472 patent at 1:52-56.

#### **VI. CONTENTIONS UNDER 35 U.S.C. § 112 PURSUANT TO P.R. 3-3(D)**

The following contentions, made pursuant to P.R. 3-3(d), are subject to revision and amendment pursuant to Federal Rule of Civil Procedure 26(e) and the Orders of record in this matter to the extent appropriate in light of further investigation and discovery regarding the defenses, the Court's construction of the claims at issue, and/or the review and analysis of expert witnesses.

Subject to the reservation of rights above, Samsung provides below an identification of asserted claims along with an identification of the specific limitations that are invalid pursuant to

35 U.S.C. § 112 ¶ 1 as lacking written description and/or enablement support and/or 35 U.S.C. § 112 ¶ 2 as indefinite.

To the extent an asserted claim includes a limitation under 35 U.S.C. § 112, ¶ 6, and the written description either does not provide support for the recited function or does not clearly link disclosed structure to performance of the recited function, that claim is invalid for indefiniteness.

To the extent an asserted claim includes a limitation under 35 U.S.C. § 112, ¶ 6, in which the associated structure involves a general purpose processor, but for which there is no, or insufficient, disclosure in the specification of the algorithms executed by the processor to accomplish the recited function, that claim is invalid for indefiniteness.

To the extent an asserted apparatus claim includes both apparatus and method limitations, that claim is invalid for indefiniteness. *See, e.g., IPXL Holdings, LLC v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005).

#### **A. '389 Patent**

##### **1. Indefiniteness – 35 U.S.C § 112 ¶ 2**

At least in view of TiVo's apparent construction of the claims in its Infringement Contentions, Claims 31 and 61 of the '389 patent are invalid under § 112 ¶ 2 regarding the claim language, "said source object is automatically flow controlled by said transform object" and "said sink object is automatically flow controlled by said transform object." TiVo appears to contend that automatic flow control means that the transform object "self-regulates" both the source object and the sink object. A person of ordinary skill in the art would not understand how, if at all, the claimed transform object "self-regulates" another object.

Claim 32 is invalid under § 112 ¶ 2 regarding the claim language, "a module for accepting television (TV) broadcast signals," "a module for tuning said TV signals to a specific

program,” “module for storing said video and audio components on a storage device,” and “Output Section . . . .” Each of these limitations are subject to 35 U.S.C. § 112 ¶ 6, but the ’389 patent specification fails to clearly link and/or disclose structure corresponding to the recited functions of each of these limitations. Claim 32 is therefore invalid for indefiniteness under 35 U.S.C. § 112 ¶ 2.

## **2. Written Description and/or Enablement – 35 U.S.C. § 112 ¶ 1**

At least in view of TiVo’s apparent construction of the claims in its Infringement Contentions, claims 5, 31, 36, and 61 are invalid because the specification as filed does not contain a written description of the claimed inventions. In particular, the patent disclosure would not lead a person of ordinary skill in the art to understand that the named inventors had possession of the purported inventions as claimed and in view of TiVo’s apparent construction of the claims in its Infringement Contentions.

Claims 5 and 36 are invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable a “storing and extracting of said video and audio components . . . simultaneously.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, the specification fails to describe how simultaneous storage and extraction of video and audio components is achieved. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed.

Claims 31 and 61 are invalid under § 112 ¶ 1 at least in view of TiVo’s apparent construction of the claims in its Infringement Contentions for failing to meet the written description and/or enablement requirements because the specification as filed does not provide

an adequate written description or enable a transform object self-regulating source and sink objects (Plaintiff's apparent construction of "automatically flow controlled"). The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed.

**B. '195 Patent**

**1. Indefiniteness – 35 U.S.C § 112 ¶ 2**

All asserted claims are invalid under § 112 ¶ 2 because the specification fails to clearly link and/or disclose structure corresponding to the recited functions of the following means-plus-function limitations:

- "cache access means for selecting a portion of the linear cache for streaming access to information stored therein" (claims 58 and 78)
- "cache control means for controlling a rate of said streaming access to said linear cache; . . . wherein said cache control means controls a rate and direction of said streaming access" (claim 58)
- "synchronization means for synchronizing streamed information from said linear cache for delivery to said cache access means" (claims 58 and 78)
- "presentation means for presenting the streaming access from said cache access means to a storage device" (claims 64 and 83)
- "cache control means for controlling a rate of said streaming access to said linear cache; . . . cache control means sends clock events to said cache access means to control a rate and direction of said streaming access" (claim 78)

- “cache access means for selecting a portion of said linear caches for streaming access” (claim 119)
- “cache control means for controlling a rate of streaming access from said linear caches; wherein said cache control means controls a rate and direction of streaming access” (claim 119)

Claim 119 is also invalid under § 112 ¶ 2 regarding the claim language “wherein said linear cache maintains a window that represents a time span into a past history of said data stream that includes a most recently stored portion of said data stream” and “wherein said linear cache discard any information that falls outside of said window.” To which of the claimed plurality of “linear caches” and “data streams” these claim limitations refer cannot be ascertained by a person of ordinary skill in the art with reasonable certainty.

### **C. '472 Patent**

#### **1. Indefiniteness – 35 U.S.C § 112 ¶ 2**

All asserted claims of the '472 patent are invalid under § 112 ¶ 2 regarding the claim language, “media manager.” The meaning of the term, “media manager,” cannot be ascertained by a person of ordinary skill in the art with reasonable certainty when read in light of the specification and prosecution history, because a person of ordinary skill in the art would not understand how, if at all, the claimed “media manager” differs from the claimed “media switch.” Neither the claims, the specification, nor the prosecution history provides any description that would enable a person of ordinary skill in the art to determine what constitutes a “media manager” and how that is different from a “media switch.”

Claim 13 is invalid under § 112 ¶ 2 regarding the claim language, “said decoder,” which lacks any antecedent basis. This deficiency renders claim 13 invalid because a person of ordinary skill in the art would find that the inconsistency of the term “said decoder” without an

antecedent basis renders the scope of the claim not reasonably certain when read in light of the specification and prosecution history. *See Young*, 492 F.3d at 1346. Accordingly, claim 13 fails to particularly point and distinctly claim the subject matter that the inventor regards as the invention and is therefore indefinite and invalid under § 112 ¶ 2.

## **2. Written Description and/or Enablement – 35 U.S.C. § 112 ¶ 1**

At least in view of TiVo's apparent construction of the claims in its Infringement Contentions, the asserted claims are invalid because the specification as filed does not contain a written description of the claimed inventions. In particular, the patent disclosure would not lead a person of ordinary skill in the art to understand that the named inventors had possession of the purported inventions as claimed, either as a whole or in view of specific elements (examples of which are given below).

Claim 1 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable a "system for the simultaneous storage and playback of multimedia data" to the extent the preamble serves as a limitation of the claim. The specification—both as filed in the 1998 Application No. 09/126,071 ("’071 Application") and the new matter added in the 2001 continuation-in-part Application No. 09/935,426 ("the ’426 CIP Application")—does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, neither the ’071 Application nor the ’426 CIP Application describe simultaneous storage and playback of multimedia data. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “input section,” should that term be construed as broadly as TiVo appears to be asserting in its infringement contentions. The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, neither the ’071 Application nor the ’426 CIP Application describe an “input section” comprising a camera, video-camera, or “wifi, mobile communication connection and/or a USB.” (Ex. G to TiVo’s Infring. Cont. at 40.) In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element should those terms be construed as broadly as TiVo appears to be asserting in its infringement contentions.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “output section including . . . a storage subsystem.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe a storage subsystem as part of the claimed “output section.” Rather, the ’071 Application only describes a storage subsystem as separate from the claimed “output section.” Accordingly, to the extent the ’472 patent is entitled to the priority date of the ’071 Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to



meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element as it does not enable a skilled artisan to construct a system with the storage subsystem as part of the claimed output section.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “decoder subsystem.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any decoder subsystem, which is described for the first time, if at all, in the 2001 ’426 CIP Application. Accordingly, to the extent the ’472 patent is entitled to the priority date of the ’071 Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the terms, “media switch” and “media manager,” should those terms be construed as broadly as TiVo appears to be asserting in its infringement contentions. The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate

the written description requirement of § 112 ¶ 1. For example, neither the '071 Application nor the '426 CIP Application describe either a “media switch” or “media manager” as a collection of disparate, distributed components. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element should those terms be construed as broadly as TiVo appears to be asserting in its infringement contentions.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “host controller.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, the '071 Application does not describe any host controller, which is described for the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '472 patent is entitled to the priority date of the '071 Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “DMA controller.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description

requirement of § 112 ¶ 1. For example, the '071 Application does not describe any DMA controller, which is described for the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '472 patent is entitled to the priority date of the '071 Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “bus arbiter.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, the '071 Application does not describe any bus arbiter, which is described for the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '472 patent is entitled to the priority date of the '071 Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “multimedia data stream processor.” The specification does not allow a person of ordinary skill in the art to

recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, the '071 Application does not describe any multimedia data stream processor, which is described for the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '472 patent is entitled to the priority date of the '071 Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 1 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable “a storage subsystem connected to said media switch, wherein multimedia data are stored on said storage subsystem and retrieved from said storage subsystem essentially simultaneously.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, neither the '071 Application nor the '426 CIP Application describe how the claimed system would store and retrieve multimedia data to and from a storage subsystem essentially simultaneously. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed.

Claim 13 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “decoder/graphics subsystem.” The specification does not allow a person of ordinary skill in the art to recognize

that the applicant invented what is claimed, and claim 13 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the '071 Application does not describe any decoder/graphics subsystem, which is described for the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '472 patent is entitled to the priority date of the '071 Application—as TiVo contends—claim 13 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 14 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “decoder/graphics subsystem includes any combination of . . . .” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 14 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the '071 Application does not describe any decoder/graphics subsystem, let alone one including the additional components recited in claim 14, all of which are described for the first time, if at all,, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '472 patent is entitled to the priority date of the '071 Application—as TiVo contends—claim 14 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element. Moreover, to the extent a decoder/graphics subsystem can be satisfied by the presence of an MPEG-2 decoder and a graphics processor, claim 14 is invalid

under § 112 ¶ 4 because it does not “specify a further limitation of the subject matter claimed” in a previously set-forth claim. For example, TiVo appears to contend that claim 14 may be satisfied in the presence of a decoder/graphics subsystem (already claimed in claim 13), which includes at least an MPEG-2 decoder and a graphics processor.

Claim 15 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “wherein said transport stream interface receives said transport stream from said input section.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 15 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any “transport stream interface [that] receives said transport stream from said input section,” which is described for the first time, if at all, in the 2001 ’426 CIP Application. Accordingly, to the extent the ’472 patent is entitled to the priority date of the ’071 Application—as TiVo contends—claim 15 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 16 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “wherein said transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet streams are stored and played back though [sic] an output side of said transport

stream decoder/graphics subsystem.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 16 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe this element, which is described for the first time, if at all, in the 2001 ’426 CIP Application. Accordingly, to the extent the ’472 patent is entitled to the priority date of the ’071 Application—as TiVo contends—claim 16 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 20 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “a SDRAM connected to said transport stream decoder/graphics subsystem.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 20 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any “SDRAM connected to said transport stream decoder/graphics subsystem,” which is described for the first time, if at all, in the 2001 ’426 CIP Application. Accordingly, to the extent the ’472 patent is entitled to the priority date of the ’071 Application—as TiVo contends—claim 20 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 22 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “wherein said processor is operative to run system software, middleware, and application software.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 22 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any “processor [] operative to run system software, middleware, and application software,” which is described for the first time, if at all, in the 2001 ’426 CIP Application. Accordingly, to the extent the ’472 patent is entitled to the priority date of the ’071 Application—as TiVo contends—claim 22 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 23 is also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 23 thus violates the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any “system software [that] includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components” which is described for



the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '472 patent is entitled to the priority date of the '071 Application—as TiVo contends—claim 23 is invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 30 is also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in said media manager.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 30 thus violates the written description requirement of § 112 ¶ 1. For example, the '071 Application does not describe any “front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in said media manager” which is described for the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '472 patent is entitled to the priority date of the '071 Application—as TiVo contends—claim 30 is invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 32 is also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “wherein said second bus element comprises a system bus.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 32 thus violates the written description

requirement of § 112 ¶ 1. For example, the '071 Application does not describe “wherein said second bus element comprises a system bus,” which is described for the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '472 patent is entitled to the priority date of the '071 Application—as TiVo contends—claim 32 is invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

**D. '476 Patent**

**1. Indefiniteness – 35 U.S.C § 112 ¶ 2**

Claim 6 is invalid under § 112 ¶ 2 regarding the claim language, “said decoder,” which lacks any antecedent basis. This deficiency renders claim 6 invalid because a person of ordinary skill in the art would find that the inconsistency of the term “said decoder” without an antecedent basis renders the scope of the claim not reasonably certain when read in light of the specification and prosecution history. *See Young*, 492 F.3d at 1346. Accordingly, claim 13 fails to particularly point and distinctly claim the subject matter that the inventor regards as the invention and are therefore indefinite and invalid under § 112 ¶ 2.

**2. Written Description and/or Enablement – 35 U.S.C. § 112 ¶ 1**

At least in view of TiVo’s apparent construction of the claims in its Infringement Contentions, the asserted claims are invalid because the specification as filed does not contain a written description of the claimed inventions. In particular, the patent disclosure would not lead a person of ordinary skill in the art to understand that the named inventors had possession of the purported inventions as claimed, either as a whole or in view of specific elements (examples of which are given below).

Claim 1 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable a “system for the simultaneous storage and retrieval of multimedia data” to the extent the preamble serves as a limitation of the claim. The specification—both as filed in the 1998 Application No. 09/126,071 (“’071 Application”) and the new matter added in the 2001 continuation-in-part Application No. 09/935,426 (“the ’426 CIP Application”)—does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, neither the ’071 Application nor the ’426 CIP Application describe simultaneous storage and retrieval of multimedia data. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “input section,” should that term be construed as broadly as TiVo appears to be asserting in its infringement contentions. The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, neither the ’071 Application nor the ’426 CIP Application describe an “input section” comprising a camera or video-camera, an antenna for cellular, wifi, or Bluetooth telecommunication, or a USB connection. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element should

those terms be construed as broadly as TiVo appears to be asserting in its infringement contentions.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “decoder subsystem.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any decoder subsystem, which is described for the first time, if at all, in the 2001 ’426 CIP Application. Accordingly, to the extent the ’472 patent is entitled to the priority date of the ’071 Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “media switch,” should that terms be construed as broadly as TiVo appears to be asserting in its infringement contentions. The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, neither the ’071 Application nor the ’426 CIP Application describe either “media switch” as a collection of disparate, distributed components. In addition, for at least the same reasons, the specification would not have enabled

one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element should those terms be construed as broadly as TiVo appears to be asserting in its infringement contentions.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “host controller.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any host controller, which is described for the first time, if at all, in the 2001 ’426 CIP Application. Accordingly, to the extent the ’476 patent is entitled to the priority date of the ’071 Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “DMA controller.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any DMA controller, which is described for the first time, if at all, in the 2001 ’426 CIP Application. Accordingly, to the extent the ’476 patent is entitled to the priority date of the ’071

Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “bus arbiter.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any bus arbiter, which is described for the first time, if at all, in the 2001 ’426 CIP Application. Accordingly, to the extent the ’476 patent is entitled to the priority date of the ’071 Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 1 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “multimedia data stream processor.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any multimedia data stream processor, which is described for the first time, if at all, in

the 2001 '426 CIP Application. Accordingly, to the extent the '476 patent is entitled to the priority date of the '071 Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 1 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable “a storage subsystem communicatively connected to said media switch, wherein multimedia data are stored on said storage subsystem and retrieved from said the storage subsystem essentially simultaneously.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and the asserted claims thus violate the written description requirement of § 112 ¶ 1. For example, neither the '071 Application nor the '426 CIP Application describe how the claimed system would store and retrieve multimedia data to and from the storage subsystem essentially simultaneously. Accordingly, to the extent the '476 patent is entitled to the priority date of the '071 Application—as TiVo contends—the asserted claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed.

Claim 6 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “decoder/graphics subsystem.” The specification does not allow a person of ordinary skill in the art to recognize

that the applicant invented what is claimed, and claim 6 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the '071 Application does not describe any decoder/graphics subsystem, which is described for the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '476 patent is entitled to the priority date of the '071 Application—as TiVo contends—claim 6 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 7 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “decoder/graphics subsystem includes at least one of . . . .” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 7 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the '071 Application does not describe any decoder/graphics subsystem, let alone one including the additional components recited in claim 7, all of which are described for the first time, if at all (in the context of MPEG-2, in the 2001 '426 CIP application. Accordingly, to the extent the '476 patent is entitled to the priority date of the '071 Application—as TiVo contends—claim 7 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element. Moreover, to the extent a decoder/graphics subsystem can be satisfied by the presence of an MPEG-2 decoder and a graphics processor, claim 7 is invalid



under § 112 ¶ 4 because it does not “specify a further limitation of the subject matter claimed” in a previously set-forth claim. For example, TiVo appears to contend that claim 7 may be satisfied in the presence of a decoder/graphics subsystem (already claimed in claim 6), which includes at least an MPEG-2 decoder and a graphics processor. Moreover, claim 7 recites an “MPEG-3 transport demultiplexer” and an “MPEG-3 decoder,” but the specification as filed does not provide an adequate written description or enable the full scope of “MPEG-3” components. For this additional reason, claim 7 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements.

Claim 8 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “wherein the transport stream interface receives the transport stream from the input section.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 8 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any “transport stream interface [that] receives the transport stream from the input section,” which is described for the first time, if at all, in the 2001 ’426 CIP Application. Accordingly, to the extent the ’476 patent is entitled to the priority date of the ’071 Application—as TiVo contends—claim 6 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 9 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “wherein the transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet streams are stored and played back through an output side of the transport stream decoder/graphics subsystem.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 9 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe this element, which is described for the first time, if at all, in the 2001 ’426 CIP application. Accordingly, to the extent the ’476 patent is entitled to the priority date of the ’071 Application—as TiVo contends—claim 7 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 10 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “a SDRAM connected to the transport stream decoder/graphics subsystem.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 10 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the ’071 Application does not describe any “SDRAM connected to the transport stream decoder/graphics subsystem,” which is described for the first time, if at all, in the 2001 ’426 CIP Application. Accordingly, to the extent the ’476 patent is entitled to the priority date of

the '071 Application—as TiVo contends—claim 10 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 11 and its dependent claims are also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “wherein the processor is operative to run system software, middleware, and application software.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 11 and its dependent claims thus violate the written description requirement of § 112 ¶ 1. For example, the '071 Application does not describe any “processor [] operative to run system software, middleware, and application software,” which is described for the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '476 patent is entitled to the priority date of the '071 Application—as TiVo contends—claim 11 and its dependent claims are invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 13 is also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in the media switch.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is

claimed, and claim 13 thus violates the written description requirement of § 112 ¶ 1. For example, the '071 Application does not describe any “front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in the media switch” which is described for the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '476 patent is entitled to the priority date of the '071 Application—as TiVo contends—claim 13 is invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

Claim 14 is also invalid under § 112 ¶ 1 for failing to meet the written description and/or enablement requirements because the specification as filed does not provide an adequate written description or enable the full scope of the term, “system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components.” The specification does not allow a person of ordinary skill in the art to recognize that the applicant invented what is claimed, and claim 14 thus violates the written description requirement of § 112 ¶ 1. For example, the '071 Application does not describe any “system software [that] includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components” which is described for the first time, if at all, in the 2001 '426 CIP Application. Accordingly, to the extent the '476 patent is entitled to the priority date of the '071 Application—as TiVo contends—claim 14 is invalid under § 112 ¶ 1 for failing to meet the written description requirement. In addition, for at least the same reasons, the specification would not have enabled one of ordinary skill in the art at the time of the purported invention to make and use it as claimed with respect to this element.

## **VII. P.R. 3-4 DOCUMENT PRODUCTION**

Samsung further reserves the right to supplement its P.R. 3-4 document production should it later find additional, responsive documents.

### **A. Documents Related to Accused Instrumentalities Under P.R. 3-4(a)**

Based on its investigations to date, Samsung also produces and/or makes available for inspection documents and/or source code pursuant to P.R. 3-4(a), which directs the production of “[s]ource code, specifications, schematics, flow charts, artwork, formulas, or other documentation sufficient to show the operation of any aspects or elements of an Accused Instrumentality identified by the patent claimant in its P.R. 3-1(c) chart.” *See* source code to be made available for inspection at the downtown Los Angeles office of O’Melveny & Myers, LLP (pursuant to procedures established in the the Court’s Protective Order (Dkt. No. 55)), as described in E. Alper’s letter to T. Werner dated April 22, 2016 and N. Graubart email to T. Werner dated April 25, 2016; *see also* documents previously produced to TiVo’s counsel, including user manuals, service manuals, data sheets, and web pages bearing the production numbers below:

SAM0001610 – 6652; SAM0006653 – 8570; SAM0008571 – 63443;  
SAM0063445 – 67249; SAM0067250 – 69125; SAM0069126 – 69259

In addition, Samsung directs TiVo to the additional documents Samsung is producing concurrently with these P.R. 3-3 Disclosures, bearing production numbers:

SAM0087796-161584

### **B. Documents Related to Prior Art Under P.R. 3-4(b)**

Based on its investigation to date, pursuant to P.R. 3-4(b), Samsung hereby produces documents currently within its possession, custody, or control that are the prior art references identified above and/or in the attached charts in connection with Samsung’s P.R. 3-3(a)

disclosures, including publications, software, source code and related documentation. P.R. 3-4(b)

documents include:

SAM0075939 – 87699; SAM0161585 – 185336; SAM0222473 – 222498;  
SAM0227336 – 227351; [TI-0000001 – TI-0016157](#)

Dated: May 5, 2016

Respectfully submitted,

/s/ Thad C. Kodish

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**CERTIFICATE OF SERVICE**

The undersigned certifies that on this 5th day of May 2016, the above document was served on counsel for Plaintiff by electronic mail.

/s/ Thad C. Kodish  
Thad C. Kodish



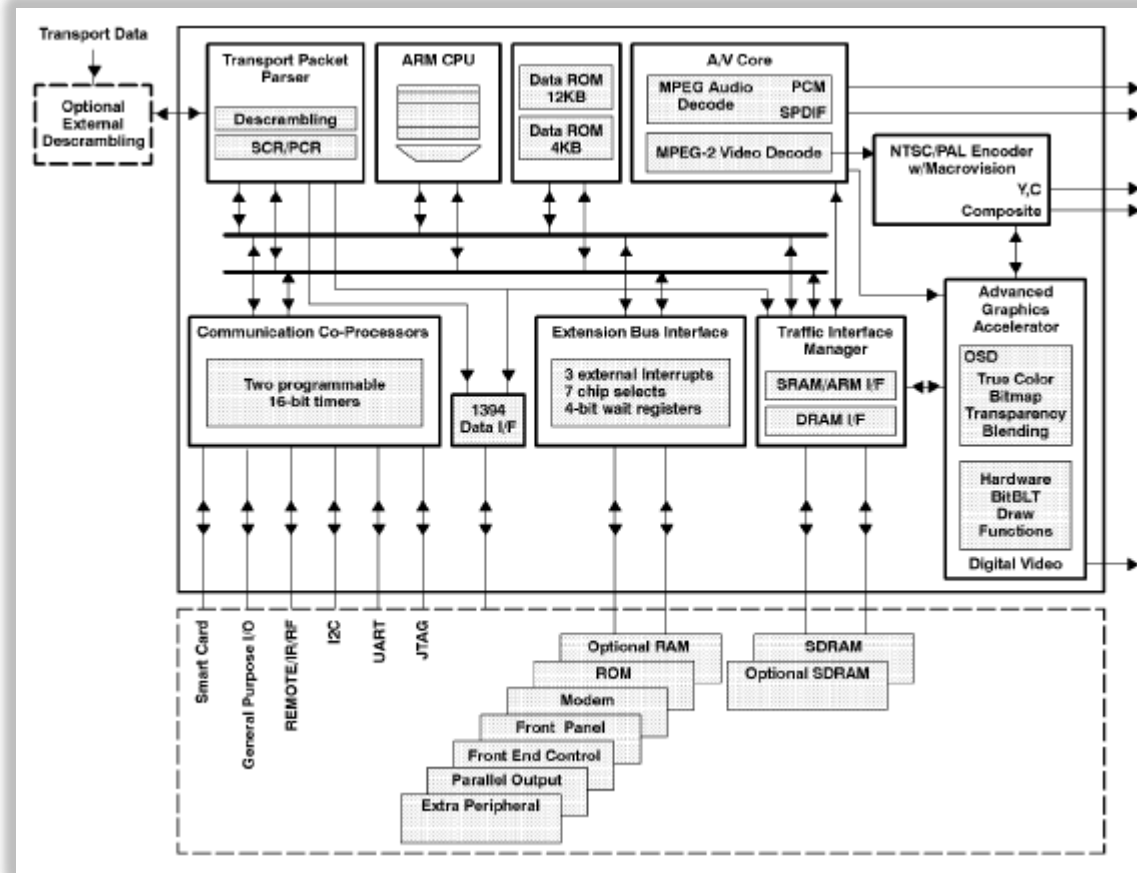
**Invalidity Contentions for U.S. Patent No. 6,233,389**  
**Based on TMS320AV7100 Integrated Set-Top Digital Signal Processor by Texas Instruments (“AV7100 Preview”)**

Based upon TiVo’s Complaint, Infringement Contentions, and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered, the reference charted below anticipates or at least renders obvious the asserted claims. These invalidity contentions are not an admission by Samsung that the accused products are covered by or infringe the asserted claims, particularly when these claims are properly construed and applied. These invalidity contentions are not an admission that Samsung concedes or acquiesces to any claim construction implied or suggested by TiVo’s Complaint or Infringement Contentions. Nor is Samsung asserting any claim construction positions through these charts, including whether the preamble is a limitation. The portions of the prior art reference cited below are not exhaustive but are exemplary in nature.

<b>’389 Patent Claim</b>	<b>Exemplary Prior Art Disclosure</b>
[1pre]. A process for the simultaneous storage and play back of multimedia data, comprising the steps of:	<p>To the extent that the preamble is limiting, AV7100 Preview discloses or at least renders obvious a process for the simultaneous storage and play back of multimedia data based on at least the following exemplary disclosures:</p> <p>“The TMS320AV7100 Integrated Digital Satellite System (DSS) Set-Top Digital Signal Processor (‘AV7100) is designed to be the core of a digital set-top box. It incorporates an Advanced RISC Machines (ARM) central processor, a transport bit stream decoder, an MPEG video and audio decoder, an NTSC/PAL (National Television Standards Committee/Phase Alternating Line) video encoder, an on-screen display controller to mix graphics and video, a 1394 interface to an external 1394 device, two universal asynchronous receiver transmitter (UART) serial data interfaces, infra red (IR) and radio frequency (RF) remote control inputs, REMOTE input and output, a smart card interface, and an extension bus to connect peripherals, such as additional RS232 ports, display and control panels, and additional read-only memory (ROM) and dynamic RAM (DRAM). External program and data memory expansion allows the ‘AV7100 to support a range of set-top boxes from low- to high-end.” AV7100 Preview at 1.</p>

## '389 Patent Claim

## Exemplary Prior Art Disclosure



AV7100 Preview at 9 fig. 1.

“trick mode decoding

When decoding a picture from a digital recorder, the ‘AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors.

During trick mode decoding, the video decoder repeats the following steps:

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li> </ul> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p> <div> <pre> graph LR     In(( )) --&gt; I1394[1394 Interface]     I1394 --&gt; MUX[MUX]     MUX --&gt; TPP[TPP]     TPP &lt;--&gt; DES[DES]     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM[RAM]     TPP --&gt; I1394 </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“extension bus read and write timing The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p>
[1a] accepting television (TV) broadcast signals, wherein said TV signals are based on a multitude of standards, including, but not limited to, National Television Standards Committee (NTSC) broadcast, PAL broadcast, satellite	<p>AV7100 Preview discloses or at least renders obvious “accepting television (TV) broadcast signals, wherein said TV signals are based on a multitude of standards, including, but not limited to, National Television Standards Committee (NTSC) broadcast, PAL broadcast, satellite transmission, DSS, DBS, or ATSC” based on at least the following exemplary disclosures:</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies</p>

'389 Patent Claim	Exemplary Prior Art Disclosure
transmission, DSS, DBS, or ATSC;	<p>whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention.” AV7100 Preview at 15.</p> <p>AV7100 Preview at 20, table 8 (e.g., “NewChannel”).</p> <p>“input interface The transport packet data from the FEC device is input to the ‘AV7100 eight bits at a time, using the byte clock, DCLK. A high on PACCLK signals valid packet data. During satellite sourced decode, a DERROR signal is received from the FEC device to indicate that a packet has data errors. The DERROR pin is valid on the first byte or one data byte cycle before the first data byte. It does not change until the following packet.” AV7100 Preview at 16; <i>see also id.</i> at 17 fig. 5 (illustrating input interface timing).</p> <p><i>See</i> AV7100 Preview at 1 (stating that the AV7100 “[a]ccepts Transport Bit Stream Up to 40-MBits per Second”).</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p>“During recording, it is assumed that input data originates from the FEC device. An FEC error signal sets the DERROR pin at or before the first byte of input data. This DERROR value is sent to the PERROR output on the 1394 interface coincident with the first valid PDATA. The PERROR value remains active as long as the FEC device keeps DERROR active. Typically, the FEC device retains DERROR until the beginning of the following packet. In this case, the 1394 link device may check for record errors at the first data byte of the packet.” AV7100 Preview at 54.</p>

'389 Patent Claim	Exemplary Prior Art Disclosure
[1b] tuning said TV signals to a specific program;	<p>AV7100 Preview discloses or at least renders obvious “tuning said TV signals to a specific program” based on at least the following exemplary disclosures:</p> <p><i>See</i> [1a].</p>
[1c] providing at least one Input Section, wherein said Input Section converts said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation;	<p>AV7100 Preview discloses or at least renders obvious “providing at least one Input Section, wherein said Input Section converts said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation” based on at least the following exemplary disclosures:</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“During recording, it is assumed that input data originates from the FEC device. An FEC error signal sets the DERROR pin at or before the first byte of input data. This DERROR value is sent to the PERROR output on the 1394 interface coincident with the first valid PDATA. The PERROR value remains active as long as the FEC device keeps DERROR active. Typically, the FEC device retains DERROR until the beginning of the following packet. In this case, the 1394 link device may check for record errors at the first data byte of the packet.” AV7100 Preview at 54.</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p><i>See</i> AV7100 Preview at 1 (stating that the AV7100 “[a]ccepts Transport Bit Stream Up to 40-MBits per Second”).</p> <p>“Video Decoder Decodes MPEG-1 (Moving Pictures Experts Group) and MPEG-2 Main Profile and Main Level Bit Stream</p> <ul style="list-style-type: none"> <li>• Audio Decoder Decodes MPEG-1 Layer I and II Bit Stream” AV7100 Preview at 1.</li> </ul> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Supports output data in both PCM and SPDIF formats</li> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p>“The video decoder is capable of producing decimated pictures using <math>\frac{1}{2}</math> or <math>\frac{1}{4}</math> decimation per dimension, which results in reduced areas of <math>\frac{1}{4}</math> or <math>\frac{1}{16}</math>, respectively. The decimated picture can be viewed in real time. Decimation is achieved by using field data out of a frame, skipping lines, and performing vertical filtering to smooth the decimated image.” AV7100 Preview at 19.</p> <p>See AV7100 Preview at 19 (describing (1) display formats supported by AV7100, (2) aspect ratio conversion supported by the AV7100).</p> <p>“Audio Output in Both Pulse Code Modulation (PCM) and SPDIF Formats On-Screen Display (OSD) Processor Enables Mixture of OSD and Video Data With Transparency” AV7100 Preview at 1.</p> <p>“On-Chip NTSC/PAL Encoder Incorporates Closed Caption and Video Aspect Ratio Identification Signal Encoding and the Macrovision® Logic for Anti-Taping Protection Analog Y, C, and Composite Video Outputs With 9-Bit Precision Internally or Externally Generated Video Synchronization Signals Digital Video Component Output That Also Contains Aspect Ratio Identification Code” AV7100 Preview at 1.</p> <p>“Both the video and audio decoders synchronize their presentation using the transmitted PTS. For DSS the PTS is transmitted as picture user data in the video bit stream and as an MPEG-1 system packet bit stream for audio. Dedicated hardware decodes the PTS if it is in the MPEG-1 system packet and forwards it to the audio decoder. The video decoder decodes PTS from picture user data. Both the video and audio decoders compare PTS to the</p>



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	<p>local system clock in order to synchronize presentation of reconstructed data. The local system clock is continuously updated by the ARM.</p> <p>When the PTS and local system clock do not match within tolerance, the video decoder either redisplay or skips a frame. At that time, the CC/EDS is handled as follows:</p> <ul style="list-style-type: none"> <li>• When the video decoder redisplay a frame, the second display does not contain CC/EDS.</li> <li>• When the video decoder skips a frame, the corresponding CC/EDS is also skipped.” AV7100 Preview at 20.</li> </ul> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending them with the video. The OSD module accepts video from the video decoder, reads OSD data from SDRAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces. OSD defaults to standby mode and simply routes video from the video decoder to both outputs. The ARM is responsible for turning on/off OSD operations and for setting specific window attributes of the OSD windows. Dedicated bitBLT hardware attached to the OSD module provides acceleration to memory block moves and graphics operations. OSD data may originate from the user data in the bit stream or may be generated by applications executed on the ARM. Regardless of the source, the OSD data is stored in the SDRAM and managed by the ARM. Memory space in the single 16 Mbits SDRAM is limited to approximately 241 kbytes for OSD, with capability to increase this to approximately 391 kbytes using the half resolution display mode. The OSD data may be represented in one of the following forms: bitmap, graphics 4:4:4 component, 4:2:2 component, or simply background color.” AV7100 Preview at 22; <i>see also id.</i> at 21, 22-24 (describing additional aspects of the OSD module).</p> <p>“The ‘AV7100 provides video output signals encoded for display on a video monitor. The encoded data may include video data or blended video and OSD data. The encoder supports the NTSC format and PAL B, D, G/H and I display formats. The NTSC/PAL pin selects between NTSC and PAL output. Changing between NTSC and PAL requires a hardware reset of the device.</p> <p>The encoder uses 9-bit D/A converters (DACs) to produce an analog S-video signal on separate luminance M and chrominance © channels. An analog composite (Comp) signal is also output. Output signals conform to the RS 170A standard. Application circuits for external connections to the DAG outputs are illustrated in Figure 24. With a single-ended 75 Q load, the output current for peak white is 20 mA.” AV7100 Preview at 26.</p> <p>“The ‘AV7100 also supports various features for video display and control. Closed caption (CC) and Extended Data Services (EDS) information which has been extracted by the video decoder is passed to the ‘AV7100 encoder. The encoder then presents CC data at video line 21 and EDS at video line 284. The video decoder also extracts aspect ratio data from the bit stream and sends it to the ARM, which in turn prepares data according to</p>

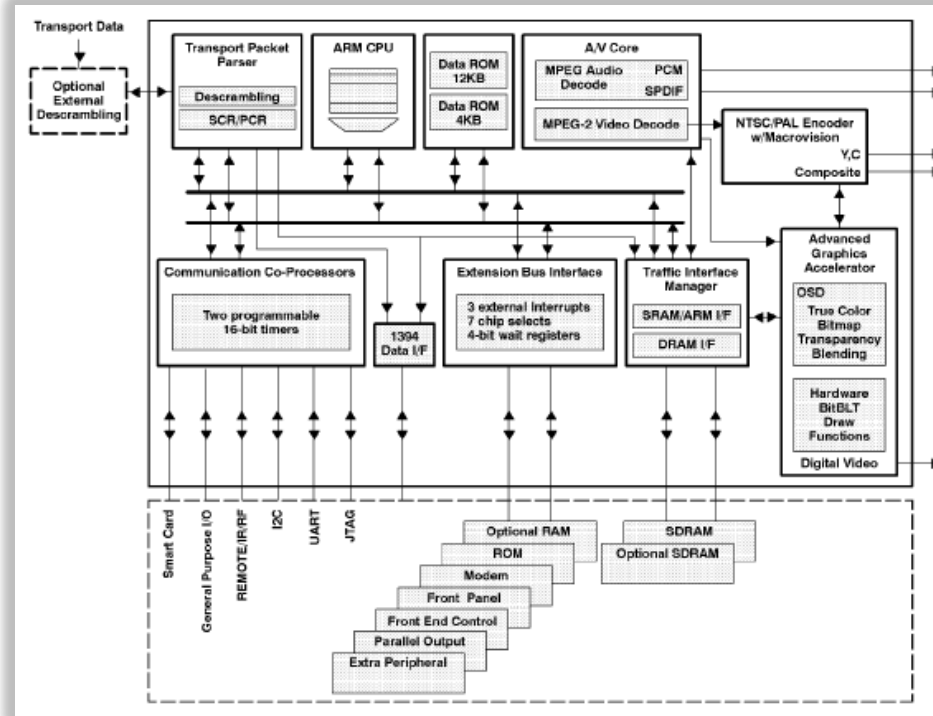
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	<p>the video aspect ratio identification signal (VARIS) standard, EIAJ CPX-1204. The ARM forwards VARIS codes to the 'AV7100 NTSC/PAL module where the codes are inserted onto the 20<sup>th</sup> video line for NTSC and 23<sup>rd</sup> line for PAL." AV7100 Preview at 26.</p> <p>"The 'AV7100 provides a digital output interface for pure video or blended video and OSD. The digital output includes video in either 4:4:4 or 4:2:2 YCrCb format. VARIS coding for aspect ratio is also provided at the beginning of each video frame. The video output format is programmable by the user, but defaults to 4:2:2. The pin assignments for the digital video output signals are:  8-bit Cb/Y/Cr/Y and VARIS multiplexed data output  27-MHz or 40.5-MHz clock output  YCOOUT(8)  YCCLK(1)  YCCTRL(2) 2-bit control signals to distinguish between YCrCb components and VARIS code" AV7100 Preview at 26; <i>see also id.</i> at 26-29 (describing additional aspects of the digital video output interface).</p> <p>"PCM audio output  The 2s complement PCM data is output serially on the PCM OUT pin using the serial clock ASCLK. ASCLK is derived from the PCM clock, PCMCLK, according to the PCMSEL 1 :O bits in the control register. The PCM clock  must be the proper multiple of the sampling frequency of the bit stream. The PCMCLK may be input to the device  or internally derived from an 36.864-MHz clock. The data on the PCMOUT pin alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value." AV7100 Preview at 31; <i>see id.</i> fig. 9 (showing timing for the PCM data).</p> <p>"SPDIF audio output  The SPDIF output conforms to a subset of the AES3 standard for serial transmission of digital audio data. The SPDIF format is a subset of the minimum implementation of AES3." AV7100 Preview at 31.</p> <p><i>See [1a].</i></p>

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[1d] providing a Media Switch, wherein said Media Switch parses said MPEG stream, said MPEG stream is separated into its video and audio components;

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AV7100 Preview discloses or at least renders obvious “providing a Media Switch, wherein said Media Switch parses said MPEG stream, said MPEG stream is separated into its video and audio components” based on at least the following exemplary disclosures:



AV7100 Preview at 9 fig. 1.

“traffic controller features

- Authorizes and manages direct memory access (DMA) transfers
- Provides SDRAM interface
- Provides memory access protection
- Manages interrupt requests
- Manages the data flow between processors and memories

TTP/DES to/from internal data RAM

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	<p>Data RAM to/from extension bus SDRAM to OSD Audio and video decoders to/from SDRAM SDRAM to/from data RAM</p> <ul style="list-style-type: none"> <li>• Manages extension bus</li> <li>• Generates chip selects for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus” AV7100 Preview at 12.</li> </ul> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware” AV7100 Preview at 15.</li> </ul> <p>“transport bit stream processing</p> <p>The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.</p> <p>The TPP also activates or deactivates the decryption engine based upon the content of the individual packet. The conditional access keys are stored in RAM and managed by firmware running on the ARM. The TPP will also detect packets lost from the transport stream. Using error concealment by the audio/video decoder and redundant</p>

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	<p>header information from the DSS bit stream, the 'AV7100 minimizes the effects of lost data." AV7100 Preview at 15.</p> <p>"ARM CPU features</p> <ul style="list-style-type: none"> <li>• Operates at 40.5 MHz</li> <li>• Supports byte (8-bit), half-word (16-bit), and word (32-bit) data types</li> <li>• Reads instructions from on-chip ROM or from the 'AV7100 extension bus</li> <li>• Switchable between ARM (32-bit) or THUMB (16-bit) instruction modes</li> <li>• 32-bit data and 32-bit address lines</li> <li>• Seven processing modes</li> <li>• Two interrupts, fast interrupt request (FIQ) and interrupt request (IRQ)" AV7100 Preview at 11.</li> </ul> <p>"The SDRAM interface supports 16-bit data width SDRAM operating at minimum 81 MHz. The SDRAM selected for use with the 'AV7100 should meet or exceed the timing requirements in Table 3 for proper operation. The TI TMS626162-12 is one example of a compatible 16 Mbit SDRAM." AV7100 Preview at 13.</p> <p>"system clock reference recovery</p> <p>Combined with the ARM, the TPP also handles system clock reference (SCR) recovery with an external VCXO. The TPP latches and transfers its internal system clock to the ARM upon the arrival of any packet which contains system clock information. After further processing of the packet and identification of the system clock, the ARM calculates the difference between the system clock from the bit stream and the internal system clock at the time the packet arrives. The ARM filters this difference and routes it through a Sigma-Delta digital-to-analog converter to control an external VCXO. Output from the 'AV7100 VCXO CTRL pin is a digital pulse train with 8-bit resolution for control. During startup, when there is no incoming SCR, the ARM drives the VCXO to its center frequency. Figure 4 provides an example circuit for the external VCXO." AV7100 Preview at 15; <i>see id.</i> tbl. 4.</p>



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	<p>circuit configuration is illustrated in Figure 23.” AV7100 Preview at 30; <i>see also id.</i> tbl. 17 (showing audio clock frequencies).</p> <p>“All firmware is stored in on-chip ROM, except the OSD graphics and some generic run-time support. The run-time support library (RTSL) and all user application software are stored outside the 'AV7100 in external memory attached to the extension bus. Details of the firmware, RTSL, and application program interface (API) are provided in the companion software document, TMS320AV7100 Software Guide.” AV7110 Product Preview at 11.</p> <p>“communication coprocessor features</p> <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> <li>• Provides three UARTs - one for smart card and two for general use</li> <li>• Accepts IR, REMOTE, and RF signals</li> <li>• Provides a REMOTE output</li> <li>• Provides two general purpose I/Os</li> <li>• Manages I2C and JTAG interfaces” AV7100 Preview at 33.</li> </ul> <p>“The communication coprocessor consists of a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR/RF, I2C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM. Interrupts are used to communicate between these interface modules and the ARM.” AV7100 Preview at 33.</p> <p>“The 'AV7100 includes an interface to the smart card access control system. The interface consists of a high-speed UART and logic to comply with the News Datacom specification (Document #HU-T052, Release E, dated November 1994, and Release F, dated January 1996) “DirecTV Project: Decoder-Smart Card Interface Requirements.” Applicable software drivers that control the interface are also included, and detailed in the companion software document for the 'AV7100.” AV7100 Preview at 33.</p> <p>“conditional access and DES processing</p> <p>The conditional access is triggered by the arrival of a control word packet (CWP). The ARM firmware recognizes that a CWP has been received and passes it to the verifier, which is the user-implemented News Datacom application software running on the ARM. The verifier reads the CWP and communicates with the</p>

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	<p>external smart card through a UART I/O interface. After verification, it passes the pointer to an 8-byte key back to the firmware, which then loads the key for the DES to decrypt succeeding packets.” AV7100 Preview at 33; <i>see id.</i> at 16 (describing additional aspects of processing transport data).</p> <p>“UART interfaces The ‘AV7100 includes two general purpose 2-wire UARTs that are memory mapped and fully accessible by application programs. The UARTs operate in asynchronous mode only and support baud rates of 1200, 2400, 4800, 9600, 14400, 19200, 28800, and 57600 kbps. The UARTs are full duplex. The transmitter is double buffered, and the receive interface is buffered with eight bytes of FIFO memory in addition to its internal register. The UARTs transmit/receive 1 start bit, 7 or 8 data bits, optional parity, and 1 or 2 stop bits. The outputs of the UARTs are digital and require external level shifters for RS232 compliance.” AV7100 Preview at 33; <i>see id.</i> at 33-34 (describing additional aspects of the UART interface).</p> <p>“The IR/RF remote control interface is a means of transmitting user commands to the set-top box. This interface consists of a custom hardware receiver implementing a bit frame-based communication protocol. A single bit frame represents a user command. The IR, RF, and REMOTEIN ports require a square wave input with no false transitions; therefore, the signal must reach its threshold prior to being applied to the pins. The interface accepts an IR, RF, or REMOTEIN data stream up to a frequency of 1.3 kHz. Since more than one data stream may be active at any given time, the ‘AV7100 hardware determines priority so that only one IR, RF, or REMOTE input is decoded.” AV7100 Preview at 35; <i>see id.</i> at 35-36 (describing additional aspects of the IR/RF remote control interface).</p> <p>“general purpose I/Os The ‘AV7100 includes two user-configurable I/O pins, 101 and 102. 101 and 102 are supported by dedicated 32-bit control/status registers, named IOSCR1 and IOSCR2, respectively.” AV7100 Preview at 36; <i>see id.</i> tbl. 20 (providing register descriptions for the control/status registers); <i>id.</i> at 37 (describing additional aspects of general purpose I/O).</p> <p>“I2C interface The ‘AV7100 includes an I2C serial bus interface that can act as either a master or slave. (Master mode is the default). In master mode, the ‘AV7100 initiates and terminates transfers and generates clock signals. Only the standard mode (100 kbit/s) I2C-bus system is implemented; fast mode is not supported. Multi-master mode is also not supported.</p>



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	<p>To put the device in slave mode the application program must set the slave mode select and a 7-bit address for the 'AV7100. The application must also send a software reset to the 12C to complete the transition to slave mode.</p> <p>In slave mode, when the programmable address bits match the applied address, the 'AV7100 responds accordingly. The 'AV7100 also responds to general call commands issued to address 0 (the general call address) that change the programmable part of the slave address. These commands are Ox04 and Ox06. No other general call commands are acknowledged, and no action is taken." AV7100 Preview at 37.</p> <p>"Note that there is no direct DMA transfer to/from extension bus memories from/to the SDRAM. However, the user can employ the bitBLT hardware (which uses data RAM) as an intermediate step to execute such a transfer. The only constraints for this type of transfer are that the block being transferred must consist of 32-bit multiples, and it must begin at a 32-bit word boundary." AV7100 Preview at 12.</p> <p>"The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers." AV7100 Preview at 12.</p> <p>"extension bus interface The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus. Each CS has its own defined memory space and a programmable wait register. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. . . .</p>

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	<p>The extension bus supports the connection of seven devices using the predefined chip selects. Additional devices may be used by externally decoding the address bus. . . . Table 22 and Table 23 show extension bus wait state and configuration registers. Each device on the extension bus is required to have data outputs in high-impedance state within one clock cycle following the removal of chip-select.” AV7100 Preview at 37.</p> <div><p><b>Table 21. Extension Bus Chip Selects</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 MBytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 32 MBytes)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7100 Preview at 37 tbl. 21 (showing name of device, its chip select, address range, and programmable wait state).</p> <p>“CS1 is intended for ARM application code, but writes are not prevented. DRAM is read/write accessible by the ARM. It is also accessed by the traffic controller for TPP and bitBLT DMA transfers.</p> <p>CS2, CS3, CS4, and CS5 all have the same characteristics. The ARM performs reads and writes to these devices through the extension bus.</p> <p>CS6 is read and write accessible by the ARM. It is also accessed by the traffic controller for TPP DMAs, and it is write only. The parallel port is one byte wide and accessed via the most significant byte.” AV7100 Preview at 38.</p> <p>“extension bus read and write timing</p> <p>The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)	N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE																														
CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)																														
N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)																														
CS2	3000 0000 – 31FF FFFF	1 – 7	Modem																														
CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel																														
CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device																														
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device																														
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port																														

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	<p>“EXTWAIT signal The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it must become active before the programmable wait cycle expires. The total number of wait states should not exceed the maximum allowed from Table 21. If the combined total wait states exceed the maximum, the decoder is not guaranteed to function properly. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT should be at least 24.7 ns. Because the EXTWAIT signal has the potential to stall the decoding process, the ARM will cap its wait at 500 ns. After this time, the ARM assumes the device that generated the EXTWAIT has failed and ignores EXTWAIT from that point forward. Only a software or hardware reset can activate the EXTWAIT signal again. . . .</p> <p>If an 8-bit device is connected to the extension bus, the EBI automatically converts the single ARM word access to four consecutive byte accesses, and the maximum wait time applies to the total of the four byte accesses. In the consecutive read access where the CS remains active during the reading of four bytes, each byte access has to complete within 125 ns. For a device that requires longer access delay, for example 250 ns, then the access from the ARM has to be limited only to half words. In a write access, where the CS toggles for each byte write, each write can take 500 ns.” AV7100 Preview at 42.</p> <p>“The extension bus supports access to 60 or 70 ns DRAM. The DRAM must have an 8-bit, 9-bit, or 10-bit column address and must have a data width of 8 or 16 bits. Byte access is allowed even when the DRAM has a 16-bit data width. The byte access is specified by the signal DCAS for EXTDATA[15:8] and CCAS for EXTDATA[7:0]. The system default DRAM configuration is 70 ns, 9-bit column address, and 16-bit data width. The firmware verifies the DRAM configuration during startup.” AV7100 Preview at 43; <i>see id.</i> at 43-50 (describing additional aspects of extension bus DRAM).</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24..” AV7100 Preview at 51-52.</p>

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	<div> <p style="text-align: center;"><b>Figure 19. 1394 Interface</b></p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<div> <pre> graph LR     In1[ ] --&gt; MUX     In2[ ] --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM     1394[1394 Interface] --&gt; MUX     1394 --&gt; TC   </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24.” AV7100 Preview at 52; <i>see id.</i> tbl. 24 (listing 1394 interface signals).</p> <p><i>See</i> AV7100 Preview at 3 (listing 1394 bus in pin descriptions table).</p> <p>“interrupts</p> <p>There are three externally accessible interrupt lines and three corresponding interrupt acknowledges on the ‘AV7100. These three interrupts, along with interrupts generated internally to the ‘AV7100, are handled by a centralized interrupt handler. Interrupt mask and priority are managed by the firmware. The three extension bus interrupts are connected to three different interrupt request lines which are visible to the user via the EXTINT2:0 pins. When the interrupt handler on the ARM begins servicing one of these interrupts, the ARM should first issue an interrupt acknowledge, which activates the corresponding EXTACK2:0 output. At the completion of the interrupt servicing, the ARM should reset the interrupt acknowledge, which returns EXTACK2:0 to the inactive state.” AV7100 Preview at 42.</p>

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	<p>“Based on programmable priority, the ARM responds to interrupt requests generated by internal modules and external devices on the extension bus. Some of the requests are for data transfers to internal RAM, whereas others are true interrupts to the ARM. The ‘AV7100s traffic controller handles data transfers, and the ARM provides services to true interrupts. Interrupts are grouped into FIQ and IRQ categories. The system software uses FIQ; the application software uses IRQ. The priorities for FIQs and IRQs are managed by the firmware.” AV7100 Preview at 11.</p> <p><i>See</i> AV7100 at 3-8, table 1 (e.g., “SMCLK,” “SMCLK2”)</p>
<p>[1e] storing said video and audio components on a storage device;</p>	<p>AV7100 Preview discloses or at least renders obvious “storing said video and audio components on a storage device” based on at least the following exemplary disclosures:</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24..” AV7100 Preview at 51-52.</p>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<div> <pre> graph TD     AV7100["'AV7100"]     EB[External Bus]     subgraph Box         direction TB         DP[DVCR Packetizer]         LI[LINK Interface]     end     DP --- Data[Data]     LI --- PI[PHY Interface]     EB --- EB_Line[ ]     EB_Line --- DP     EB_Line --- LI   </pre> <p>Figure 19. 1394 Interface</p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“During decoding, the ‘AV7100 allocates the first 16-Mbit SDRAM for NTSC mode, as shown in Figure 3.” AV7100 Preview at 14; see id. fig. 3 (showing memory allocation of 16-Mbit SDRAM).</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> </ul>

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	<ul style="list-style-type: none"> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p>“trick mode decoding</p> <p>When decoding a picture from a digital recorder, the ‘AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li> </ul> <p>“The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder AP ls. Consult the TMS320AV7100 Software Guide for details.” AV7100 Preview at 20; see id. tbl. 8 (showing video decoder commands).</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible</p>



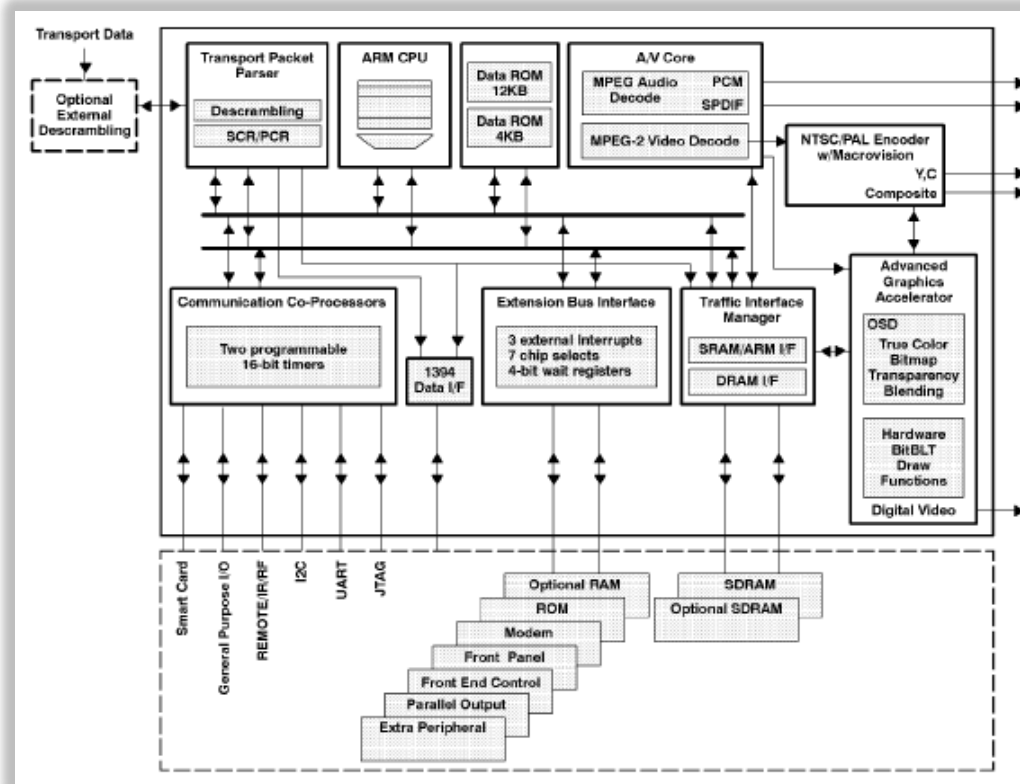
'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p> <div> <pre> graph LR     In(( )) --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM     TC --&gt; I1394[1394 Interface]     I1394 --&gt; MUX     </pre> <p>The diagram illustrates a functional block diagram of data flow. It includes a MUX (Multiplexer) block, a TPP (Transponder Processing) block, a DES (Data Encryption Standard) block, a Traffic Controller block, a RAM (Random Access Memory) block, and a 1394 Interface block. The data flow is as follows: Input data enters the MUX, which then feeds into the TPP. The TPP is bidirectionally connected to the DES block. The TPP also feeds into the Traffic Controller. The Traffic Controller is bidirectionally connected to the RAM block. The Traffic Controller feeds into the 1394 Interface, which then feeds back into the MUX.</p> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“During recording, it is assumed that input data originates from the FEC device. An FEC error signal sets the DERROR pin at or before the first byte of input data. This DERROR value is sent to the PERROR output on the 1394 interface coincident with the first valid PDATA. The PERROR value remains active as long as the FEC device keeps DERROR active. Typically, the FEC device retains DERROR until the beginning of the following packet. In this case, the 1394 link device may check for record errors at the first data byte of the packet.</p> <p>During playback mode, an error signal can cause an interrupt only once per packet. For the case of an error between packets, the 1394 link device must ensure that the PERROR of the 'AV7100 is held active until the first byte at PDATA is entered. If an error occurs within a packet, the PERROR pin must complete the transition to</p>

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	<p>high before the last byte of the packet is clocked. PERROR must then be returned low before the first byte of the following good packet.” AV7100 Preview at 54.</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“Fully Functional Decoder Using a Single 16-MBit External Synchronous Dynamic Random-Access Memory (SDRAM)” AV7100 Preview at 1.</p> <p>“The ‘AV7100 provides chip select signals for up to two SDRAMs. The minimum SDRAM size required by the decoder is 16 Mbit. Other supported sizes and configurations are:  16 Mbit --7 one 16 Mbit SDRAM  20 Mbit --7 one 16 Mbit and one 4 Mbit SDRAM  32 Mbit --7 two 16 Mbit SDRAM  The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 20 macroblock. The interface also supports decrement mode for bitBLT block transfer.  The two chip selects correspond to the following address ranges:  SCS1 --7 0xCC00 0000 - 0xCC1 F FFFF  SCS2 --7 0xCC20 0000 - 0xCDF FFFF” AV7100 Preview at 13.</p> <p>“During decoding, the ‘AV7100 allocates the first 16-Mbit SDRAM for NTSC mode, as shown in Figure 3.” AV7100 Preview at 14; see id. fig. 3 (showing memory allocation of 16-Mbit SDRAM).</p> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for</p>

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	<p>initialization and control of the video decoder. The output video is sent to the 'AV7100 on-screen display (OSD) module for further blending with OSD data." AV7100 Preview at 18.</p> <p>"The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The 'AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization." AV7100 Preview at 30.</p> <p>"extension bus read and write timing The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state." AV7100 Preview at 39.</p>
[1f] providing at least one Output Section, wherein said Output Section extracts said video and audio components from said storage device;	AV7100 Preview discloses or at least renders obvious "providing at least one Output Section, wherein said Output Section extracts said video and audio components from said storage device" based on at least the following exemplary disclosures:

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AV7100 Preview at 9 fig. 1.

“Video Decoder Decodes MPEG-1 (Moving Pictures Experts Group) and MPEG-2 Main Profile and Main Level Bit Stream

• Audio Decoder Decodes MPEG-1 Layer I and II Bit Stream” AV7100 Preview at 1.

“transport bit stream processing

The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only

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	<p>relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.</p> <p>The TPP also activates or deactivates the decryption engine based upon the content of the individual packet. The conditional access keys are stored in RAM and managed by firmware running on the ARM. The TPP will also detect packets lost from the transport stream. Using error concealment by the audio/video decoder and redundant header information from the DSS bit stream, the 'AV7100 minimizes the effects of lost data.' AV7100 Preview at 15.</p> <p>“video decoder features</p> <ul style="list-style-type: none"> <li>• Real-time video decoding of MPEG-2 Main Profile and Main Level Bit Stream and MPEG-1</li> <li>• Error detection and concealment</li> <li>• Internal 90 kHz/27-MHz system time clock</li> <li>• Sustained input rate of 15 Mbps</li> <li>• Supports trick mode with full trick mode picture</li> <li>• Provides 1/4 and 1/16 decimated picture size</li> <li>• Extracts closed caption and other picture user data from the bit stream</li> <li>• 3:2 pulldown in NTSC mode</li> <li>• Supports various display formats with polyphase horizontal resampling and vertical chrominance filtering</li> <li>• Pan-and-scan for 16:9 source material according to both DSS and MPEG syntax</li> <li>• High-level command interface</li> <li>• Synchronization using presentation time stamps (PTS)</li> <li>• Half resolution display mode allows additional OSD space in the SDRAM” AV7100 Preview at 18.</li> </ul> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The 'AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the 'AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps</p>

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	<p>(PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p> <p>“trick mode decoding  When decoding a picture from a digital recorder, the ‘AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors.  During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li> </ul> <p>“The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder AP ls. Consult the TMS320AV7100 Software Guide for details.” AV7100 Preview at 20; <i>see id.</i> tbl. 8 (showing video decoder commands).</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Supports output data in both PCM and SPDIF formats</li> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul> <p><i>See</i> AV7100 Preview at 31-32 (listing and describing audio decoder control and status registers).</p>

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	<p>“extension bus interface</p> <p>The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus. Each CS has its own defined memory space and a programmable wait register. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. . . .</p> <p>The extension bus supports the connection of seven devices using the predefined chip selects. Additional devices may be used by externally decoding the address bus. Table 21 shows the name of the device, its chip select, address range, and programmable wait state. Table 22 and Table 23 show extension bus wait state and configuration registers. Each device on the extension bus is required to have data outputs in high-impedance state within one clock cycle following the removal of chip-select.” AV7100 Preview at 37.</p> <div><p><b>Table 21. Extension Bus Chip Selects</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 MBytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 32 MBytes)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7100 Preview at 37 tbl. 21.</p> <p>“extension bus read and write timing</p> <p>The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)	N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE																														
CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)																														
N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)																														
CS2	3000 0000 – 31FF FFFF	1 – 7	Modem																														
CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel																														
CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device																														
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device																														
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port																														

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	<p>“EXTWAIT signal</p> <p>The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it must become active before the programmable wait cycle expires. The total number of wait states should not exceed the maximum allowed from Table 21. If the combined total wait states exceed the maximum, the decoder is not guaranteed to function properly. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT should be at least 24.7 ns. Because the EXTWAIT signal has the potential to stall the decoding process, the ARM will cap its wait at 500 ns. After this time, the ARM assumes the device that generated the EXTWAIT has failed and ignores EXTWAIT from that point forward. Only a software or hardware reset can activate the EXTWAIT signal again. . . .</p> <p>If an 8-bit device is connected to the extension bus, the EBI automatically converts the single ARM word access to four consecutive byte accesses, and the maximum wait time applies to the total of the four byte accesses. In the consecutive read access where the CS remains active during the reading of four bytes, each byte access has to complete within 125 ns. For a device that requires longer access delay, for example 250 ns, then the access from the ARM has to be limited only to half words. In a write access, where the CS toggles for each byte write, each write can take 500 ns.” AV7100 Preview at 42.</p> <p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p><i>See</i> AV7100 Preview at 1 (stating that the AV7100 “[a]ccepts Transport Bit Stream Up to 40-MBits per Second”).</p> <p>“Video Decoder Decodes MPEG-1 (Moving Pictures Experts Group) and MPEG-2 Main Profile and Main Level Bit Stream</p> <ul style="list-style-type: none"> <li>• Audio Decoder Decodes MPEG-1 Layer I and II Bit Stream” AV7100 Preview at 1.</li> </ul>



'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Supports output data in both PCM and SPDIF formats</li> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p>“The video decoder is capable of producing decimated pictures using <math>\frac{1}{2}</math> or <math>\frac{1}{4}</math> decimation per dimension, which results in reduced areas of <math>\frac{1}{4}</math> or <math>\frac{1}{16}</math>, respectively. The decimated picture can be viewed in real time. Decimation is achieved by using field data out of a frame, skipping lines, and performing vertical filtering to smooth the decimated image.” AV7100 Preview at 19.</p> <p><i>See</i> AV7100 Preview at 19 (describing (1) display formats supported by AV7100, (2) aspect ratio conversion supported by the AV7100).</p> <p>“Audio Output in Both Pulse Code Modulation (PCM) and SPDIF Formats On-Screen Display (OSD) Processor Enables Mixture of OSD and Video Data With Transparency” AV7100 Preview at 1.</p> <p>“On-Chip NTSC/PAL Encoder Incorporates Closed Caption and Video Aspect Ratio Identification Signal Encoding and the Macrovision® Logic for Anti-Taping Protection Analog Y, C, and Composite Video Outputs With 9-Bit Precision Internally or Externally Generated Video Synchronization Signals</p>

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	<p>Digital Video Component Output That Also Contains Aspect Ratio Identification Code” AV7100 Preview at 1.</p> <p>“Both the video and audio decoders synchronize their presentation using the transmitted PTS. For DSS the PTS is transmitted as picture user data in the video bit stream and as an MPEG-1 system packet bit stream for audio. Dedicated hardware decodes the PTS if it is in the MPEG-1 system packet and forwards it to the audio decoder. The video decoder decodes PTS from picture user data. Both the video and audio decoders compare PTS to the local system clock in order to synchronize presentation of reconstructed data. The local system clock is continuously updated by the ARM.</p> <p>When the PTS and local system clock do not match within tolerance, the video decoder either redisplay or skips a frame. At that time, the CC/EDS is handled as follows:</p> <ul style="list-style-type: none"> <li>• When the video decoder redisplay a frame, the second display does not contain CC/EDS.</li> <li>• When the video decoder skips a frame, the corresponding CC/EDS is also skipped.” AV7100 Preview at 20.</li> </ul> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending them with the video. The OSD module accepts video from the video decoder, reads OSD data from SDRAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces. OSD defaults to standby mode and simply routes video from the video decoder to both outputs. The ARM is responsible for turning on/off OSD operations and for setting specific window attributes of the OSD windows. Dedicated bitBLT hardware attached to the OSD module provides acceleration to memory block moves and graphics operations. OSD data may originate from the user data in the bit stream or may be generated by applications executed on the ARM. Regardless of the source, the OSD data is stored in the SDRAM and managed by the ARM. Memory space in the single 16 Mbits SDRAM is limited to approximately 241 kbytes for OSD, with capability to increase this to approximately 391 kbytes using the half resolution display mode. The OSD data may be represented in one of the following forms: bitmap, graphics 4:4:4 component, 4:2:2 component, or simply background color.” AV7100 Preview at 22; <i>see also id.</i> at 21, 22-24 (describing additional aspects of the OSD module).</p> <p>“The ‘AV7100 provides video output signals encoded for display on a video monitor. The encoded data may include video data or blended video and OSD data. The encoder supports the NTSC format and PAL B, D, G/H and I display formats. The NTSC/PAL pin selects between NTSC and PAL output. Changing between NTSC and PAL requires a hardware reset of the device.</p> <p>The encoder uses 9-bit D/A converters (DACs) to produce an analog S-video signal on separate luminance M and chrominance © channels. An analog composite (Comp) signal is also output. Output signals conform to the</p>

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	<p>RS 170A standard. Application circuits for external connections to the DAG outputs are illustrated in Figure 24. With a single-ended 75 <math>\Omega</math> load, the output current for peak white is 20 mA.” AV7100 Preview at 26.</p> <p>“The ‘AV7100 also supports various features for video display and control. Closed caption (CC) and Extended Data Services (EDS) information which has been extracted by the video decoder is passed to the ‘AV7100 encoder. The encoder then presents CC data at video line 21 and EDS at video line 284. The video decoder also extracts aspect ratio data from the bit stream and sends it to the ARM, which in turn prepares data according to the video aspect ratio identification signal (VARIS) standard, EIAJ CPX-1204. The ARM forwards VARIS codes to the ‘AV7100 NTSC/PAL module where the codes are inserted onto the 20<sup>th</sup> video line for NTSC and 23<sup>rd</sup> line for PAL.” AV7100 Preview at 26.</p> <p>“The ‘AV7100 provides a digital output interface for pure video or blended video and OSD. The digital output includes video in either 4:4:4 or 4:2:2 YCrCb format. VARIS coding for aspect ratio is also provided at the beginning of each video frame. The video output format is programmable by the user, but defaults to 4:2:2. The pin assignments for the digital video output signals are:  8-bit Cb/Y/Cr/Y and VARIS multiplexed data output  27-MHz or 40.5-MHz clock output  YCOOUT(8)  YCCLK(1)  YCCTRL(2) 2-bit control signals to distinguish between YCrCb components and VARIS code” AV7100 Preview at 26; <i>see also id.</i> at 26-29 (describing additional aspects of the digital video output interface).</p> <p>“PCM audio output  The 2s complement PCM data is output serially on the PCM OUT pin using the serial clock ASCLK. ASCLK is derived from the PCM clock, PCMCLK, according to the PCMSEL 1 :O bits in the control register. The PCM clock must be the proper multiple of the sampling frequency of the bit stream. The PCMCLK may be input to the device or internally derived from an 36.864-MHz clock. The data on the PCMOUT pin alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7100 Preview at 31; <i>see id.</i> fig. 9 (showing timing for the PCM data).</p> <p>“SPDIF audio output  The SPDIF output conforms to a subset of the AES3 standard for serial transmission of digital audio data. The</p>

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	<p>SPDIF format is a subset of the minimum implementation of AES3.” AV7100 Preview at 31.</p> <p><i>See</i> [1e].</p>
<p>[1g] wherein said Output Section assembles said video and audio components into an MPEG stream;</p>	<p>AV7100 Preview discloses or at least renders obvious “wherein said Output Section assembles said video and audio components into an MPEG stream” based on at least the following exemplary disclosures:</p> <p><i>See</i> [1e], [1d], and [1f].</p>
<p>[1h] wherein said Output Section sends said MPEG stream to a decoder;</p>	<p>AV7100 Preview discloses or at least renders obvious said “wherein said Output Section sends said MPEG stream to a decoder” based on at least the following exemplary disclosures:</p> <p><i>See</i> [1f] and [1g].</p>
<p>[1i] wherein said decoder converts said MPEG stream into TV output signals;</p>	<p>AV7100 Preview discloses or at least renders obvious “wherein said decoder converts said MPEG stream into TV output signals” based on at least the following exemplary disclosures:</p> <p><i>See</i> [1f].</p>
<p>[1j] wherein said decoder delivers said TV output signals to a TV receiver; and</p>	<p>AV7100 Preview discloses or at least renders “wherein said decoder delivers said TV output signals to a TV receiver” based on at least the following exemplary disclosures:</p> <p><i>See</i> [1f].</p>
<p>[1k] accepting control commands from a user, wherein said control commands are sent through the system and affect the flow of said MPEG stream.</p>	<p>AV7100 Preview discloses or at least renders obvious “accepting control commands from a user, wherein said control commands are sent through the system and affect the flow of said MPEG stream” based on at least the following exemplary disclosures:</p> <p>“communication coprocessor features</p> <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> <li>• Provides three UARTs - one for smart card and two for general use</li> </ul>

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	<ul style="list-style-type: none"> <li>• Accepts IR, REMOTE, and RF signals</li> <li>• Provides a REMOTE output</li> <li>• Provides two general purpose I/Os</li> <li>• Manages 12C and JTAG interfaces” AV7100 Preview at 33.</li> </ul> <p>“The communication coprocessor consists of a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR/RF, 12C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM. Interrupts are used to communicate between these interface modules and the ARM.” AV7100 Preview at 33.</p> <p>“The ARM is responsible for managing all hardware and software resources in the ‘AV7100. At powerup the ARM verifies the size of external memory. It then initializes all ‘AV7100 hardware modules by setting up control registers and tables and by resetting data pointers. The ARM then executes the default firmware. All firmware is stored in on-chip ROM, except the OSD graphics and some generic run-time support. The run-time support library (RTSL) and all user application software are stored outside the ‘AV7100 in external memory attached to the extension bus. Details of the firmware, RTSL, and application program interface (API) are provided in the companion software document, TMS320AV7100 Software Guide.</p> <p>Based on programmable priority, the ARM responds to interrupt requests generated by internal modules and external devices on the extension bus. Some of the requests are for data transfers to internal RAM, whereas others are true interrupts to the ARM. The 'AV7100s traffic controller handles data transfers, and the ARM provides services to true interrupts. Interrupts are grouped into FIQ and IRQ categories. The system software uses FIQ; the application software uses IRQ. The priorities for FIQs and IRQs are managed by the firmware.” AV7100 Preview at 11.</p> <p>“The ARM initializes and controls the audio decoder via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and oversampling ratio, and choose the output format for dual channel mode. The ARM also reads status information from the audio decoder via a 32-bit status register which provides the MPEG header information and sync, CRC, and PCM status.” AV7100 Preview at 30.</p> <p><i>See</i> AV7100 Preview at 20 tbl. 8 (listing use of OSD API).</p> <p>“The audio module has two registers: a read/write control register and a read-only status register. Both registers are read or written to through user software and 'AV7100 API routines.” AV7100 Preview at 31.</p>

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	<p>“The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder APIs. . . .” AV7100 Preview at 20.</p> <p>“The 'AV7100 includes an interface to the smart card access control system. The interface consists of a high-speed UART and logic to comply with the News Datacom specification (Document #HU-T052, Release E, dated November 1994, and Release F, dated January 1996) ‘DirecTV Project: Decoder-Smart Card Interface Requirements.’ Applicable software drivers that control the interface are also included, and detailed in the companion software document for the 'AV7100.” AV7100 Preview at 33.</p> <p>“The conditional access is triggered by the arrival of a control word packet (CWP). The ARM firmware recognizes that a CWP has been received and passes it to the verifier, which is the user-implemented News Datacom application software running on the ARM. The verifier reads the CWP and communicates with the external smart card through a UART I/O interface. After verification, it passes the pointer to an 8-byte key back to the firmware, which then loads the key for the DES to decrypt succeeding packets.” AV7100 Preview at 33.</p> <p>“To put the device in slave mode the application program must set the slave mode select and a 7-bit address for the 'AV7100. The application must also send a software reset to the 12C to complete the transition to slave mode.” AV7100 Preview at 37.</p> <p>“The initialization software should specify the data size of the device connected to the CS2 to CS6. CS1 and DRAM are always size 16, but CS2 to CS6 (including the parallel data port) can be programmed as a size 8 or size 16 interface. The extension bus interface does the routing between the internal 32-bit data and the 8-bit or 16-bit data on the extension bus. For example, the user program can write a word to an 8-bit device on the extension bus, and the extension bus interface performs four consecutive byte writes.” AV7100 Preview at 43.</p> <p>“device control interfaces reset</p> <p>The 'AV7100 requires a hardware reset on powerup. Reset of the device is initiated by pulling the RESET pin low for at least 100 ns while the clock is running. The following actions will then occur:</p> <ul style="list-style-type: none"> <li>• Input data on all ports is ignored.</li> <li>• External memory is sized.</li> <li>• Data pointers are reset.</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• All modules are initialized and set to a default state.</li> </ul> <p>TPP tables are initialized.  Audio decoder is set for 16 bit output with 256 x oversampling.  OSD background color is set to blue and video data is selected for the analog and digital outputs.  Macrovision is disabled.  The 12C port is set to master mode.  When the reset sequence completes, the device will begin to accept data. All data input prior to the end of the reset sequence is ignored.” AV7100 Preview at 55.</p> <p>“trick mode decoding  When decoding a picture from a digital recorder, the ‘AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors.  During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li> </ul> <p><i>See</i> [1pre], [1e], [1d], and [1f].</p>
2. The process of claim 1, wherein said Input Section directs said MPEG stream to the destination indicated by said control commands.	<p>AV7100 Preview discloses or at least renders obvious “said Input Section directs said MPEG stream to the destination indicated by said control commands” based on at least the following exemplary disclosures:</p> <p><i>See</i> claim 1 at [1a], [1pre], [1d], [1e], [1f].</p>
3. The process of claim 1, wherein said Output Section extracts said video and audio components from the storage device indicated by said control commands.	<p>AV7100 Preview discloses or at least renders obvious “said Output Section extracts said video and audio components from the storage device indicated by said control commands” based on at least the following exemplary disclosures:</p> <p><i>See</i> claim 1 at [1a], [1pre], [1d], [1e], and [1f].</p>

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5. The process of claim 1, wherein the storing and extracting of said video and audio components from said storage device are performed simultaneously.	AV7100 Preview discloses or at least renders obvious “storing and extracting of said video and audio components from said storage device are performed simultaneously” based on at least the following exemplary disclosures:  <i>See claim 1 at [1e] and [1pre].</i>
6. The process of claim 1, wherein said Media Switch calculates and logically associates a time stamp to said video and audio components.	AV7100 Preview discloses or at least renders obvious “said Media Switch calculates and logically associates a time stamp to said video and audio components” based on at least the following exemplary disclosures:  <i>See claim [1d].</i>
7. The process of claim 1, wherein said Media Switch extracts time stamp values from a digital TV stream and logically associates said time stamp values to said video and audio components.	AV7100 Preview discloses or at least renders obvious “said Media Switch extracts time stamp values from a digital TV stream and logically associates said time stamp values to said video and audio components” based on at least the following exemplary disclosures:  <i>See claim [1d].</i>
12. The process of claim 1, further comprising the step of: increasing the decoder system clock rate for fast playback or fast reverse playback.	AV7100 Preview discloses or at least renders obvious “increasing the decoder system clock rate for fast playback or fast reverse playback” based on at least the following exemplary disclosures:  <i>See claim 1 at [1pre], [1e], and [1f].</i>
13. The process of claim 1, further comprising the step of: decreasing the decoder system clock rate for slow playback or slow reverse playback.	AV7100 Preview discloses or at least renders obvious “decreasing the decoder system clock rate for slow playback or slow reverse playback” based on at least the following exemplary disclosures:  <i>See claim 1 at [1pre], [1e], and [1f].</i>
18. The process of claim 1, wherein said Media Switch has a	AV7100 Preview discloses or at least renders obvious “said Media Switch has a data bus connecting it to a CPU and DRAM” based on at least the following exemplary disclosures:

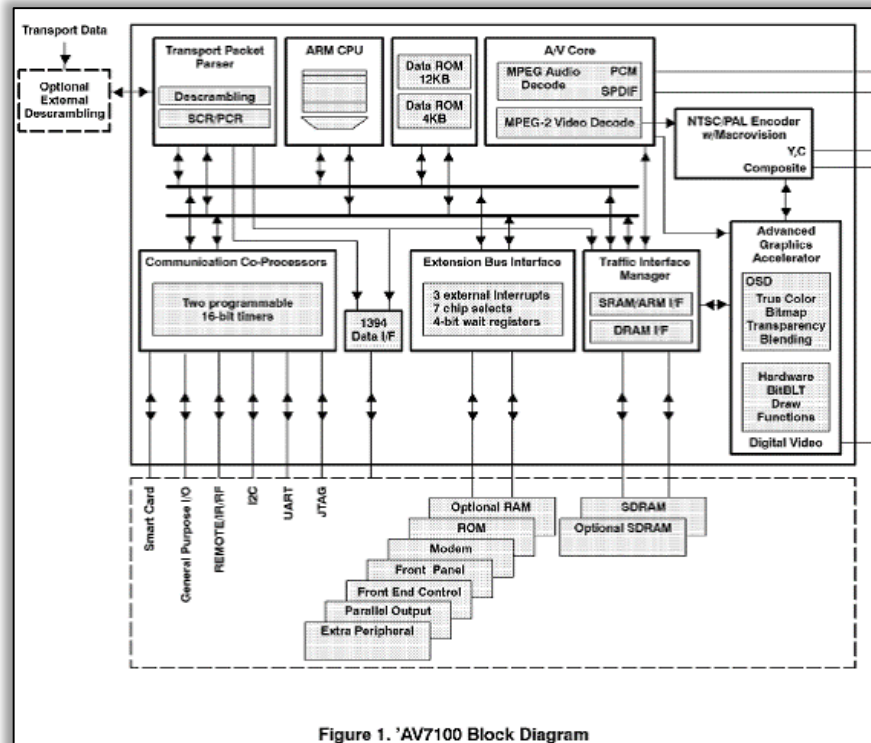


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data bus connecting it to a CPU and DRAM.	<i>See</i> claim [1d].
19. The process of claim 1, wherein said Media Switch shares an address bus with a CPU and DRAM.	AV7100 Preview discloses or at least renders obvious “said Media Switch shares an address bus with a CPU and DRAM” based on at least the following exemplary disclosures:  <i>See</i> claim [1d].
20. The process of claim 1, wherein said Media Switch operates asynchronously and autonomously with a CPU.	AV7100 Preview discloses or at least renders obvious “said Media Switch operates asynchronously and autonomously with a CPU” based on at least the following exemplary disclosures:  <i>See</i> claim [1d].
21. The process of claim 1, wherein said storage device is connected to said Media Switch.	AV7100 Preview discloses or at least renders obvious “said storage device is connected to said Media Switch” based on at least the following exemplary disclosures:  <i>See</i> claim [1d] and [1e].
22. The process of claim 1, wherein said Media Switch allows the CPU to queue up Direct Memory Access (DMA) transfers.	AV7100 Preview discloses or at least renders obvious “said Media Switch allows the CPU to queue up Direct Memory Access (DMA) transfers” based on at least the following exemplary disclosures:  <i>See</i> claim [1d].
23. The process of claim 1, wherein said Media Switch is implemented in hardware.	AV7100 Preview discloses or at least renders obvious “said Media Switch is implemented in hardware” based on at least the following exemplary disclosures:  <i>See</i> claim [1d].
[31pre]. A process for the simultaneous storage and play back of multimedia data, comprising the steps of:	To the extent that the preamble is limiting, AV7100 Preview discloses or at least renders obvious “a process for the simultaneous storage and play back of multimedia data” based on at least the following exemplary disclosures:

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	<ul style="list-style-type: none"> <li>• “The TMS320AV7100 Integrated Digital Satellite System (DSS) Set-Top Digital Signal Processor ('AV7100) is designed to be the core of a digital set-top box. It incorporates an Advanced RISC Machines (ARM) central processor, a transport bit stream decoder, an MPEG video and audio decoder, an NTSC/PAL (National Television Standards Committee/Phase Alternating Line) video encoder, an on-screen display controller to mix graphics and video, a 1394 interface to an external 1394 device, two universal asynchronous receiver transmitter (UART) serial data interfaces, infra red (IR) and radio frequency (RF) remote control inputs, REMOTE input and output, a smart card interface, and an extension bus to connect peripherals, such as additional RS232 ports, display and control panels, and additional read-only memory (ROM) and dynamic RAM (DRAM). External program and data memory expansion allows the 'AV7100 to support a range of set-top boxes from low- to high-end.” AV7100 Preview at 1.</li> <li>• <i>See</i> AV7100 Preview at Fig. 1:</li> </ul>

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- “In record mode, the packet exiting the TPP may be transferred to the 1394 interface to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder.” AV7100 Preview at 52

[31a] providing a physical data source, wherein said physical data source accepts broadcast data from an input device, parses video and audio data from said

AV7100 Preview discloses or at least renders obvious “providing a physical data source that accepts broadcast data from an input device, parses video and audio data from said broadcast data, and temporarily stores said video and audio data” based on at least the following exemplary disclosures:

- “The 'AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s.” AV7100 Preview at 15.

'389 Patent Claim	Exemplary Prior Art Disclosure
broadcast data, and temporarily stores said video and audio data;	<ul style="list-style-type: none"> <li>• “• Accepts Transport Bit Stream Up to 40-MBits per Second • On-Chip Data Encryption Standard (DES) Module For Descrambling • 1394 Interface Allows Connections to External 1394 Devices” AV7100 Preview at 1.</li> <li>• “It incorporates . . . a transport bit stream decoder.” AV7100 Preview at 1.</li> <li>• “The external SDRAM is used to store . . . video and audio bit streams, [etc.] The internal data RAM stores temporary buffers . . . and other tables and buffers for firmware.” AV7100 Preview at 12.</li> <li>• “transport packet parser features <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware” AV7100 Preview at 15.</li> </ul> </li> <li>• “The 'AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the 'AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SD RAM.” AV7100 Preview at 15.</li> </ul>

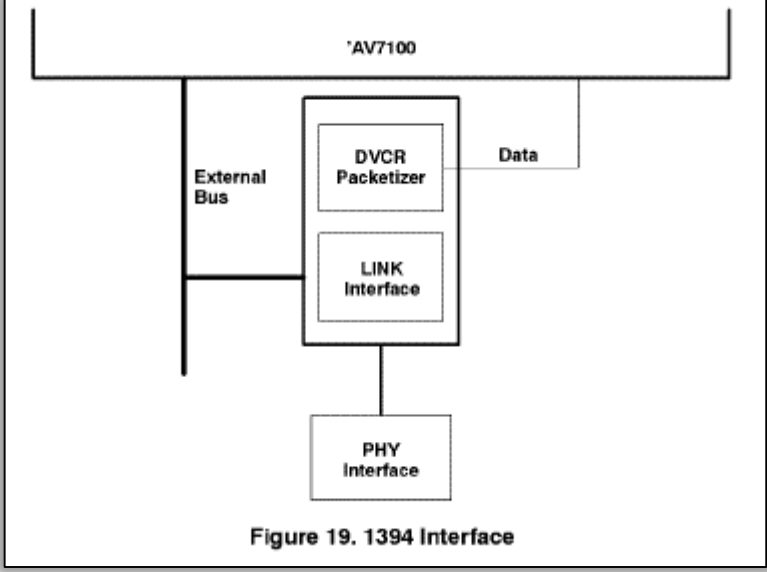
'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• “The TPP also activates or deactivates the decryption engine based upon the content of the individual packet. The conditional access keys are stored in RAM and managed by firmware running on the ARM.” AV7100 at 15.</li> <li>• “The 'AV7100 processes encrypted transport data per a DSS-specific Data Encryption Standard (DES). The conditional access and DES block is part of the packet header parsing function. A control flag (CF) bit in the packet header indicates whether the packet is clean or has been encrypted. A clean packet can be forwarded to the internal data RAM directly, whereas an encrypted packet must be passed through the DES block for decryption. The authorization and decryption key information are transmitted via control word packet (CWP). The external smart card guards this information and provides the proper key for the DES to work.” AV7100 Preview at 15.</li> <li>• “The transport packet data from the FEC device is input to the 'AV7100 eight bits at a time, using the byte clock, DCLK.” AV7100 Preview at 16.</li> <li>• “input interface The transport packet data from the FEC device is input to the 'AV7100 eight bits at a time, using the byte clock, DCLK. A high on PACCLK signals valid packet data. During satellite sourced decode, a DERROR signal is received from the FEC device to indicate that a packet has data errors. The DERROR pin is valid on the first byte or one data byte cycle before the first data byte. It does not change until the following packet.” AV7100 Preview at 16.</li> <li>• “During recording, it is assumed that input data originates from the FEC device.” AV7100 Preview at 54.</li> <li>• AV7100 Preview at Fig. 20 (e.g., “Mux”)</li> <li>• AV7100 Preview at Fig. 1 (e.g., “transport data,” “optional transport data descrambling,” “transport packet parser”)</li> </ul>
[31b] providing a source object, wherein said source object	AV7100 Preview discloses or at least renders obvious “providing a source object that extracts video and audio data from said physical data source” based on at least the following exemplary disclosures:

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extracts video and audio data from said physical data source;	<ul style="list-style-type: none"> <li>• “transport packet parser features <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware” AV7100 Preview at 15.</li> </ul> </li> <li>• “The 'AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the 'AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SD RAM.” AV7100 Preview at 15.</li> <li>• “In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder.” AV7100 Preview at 52.</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• AV7100 Preview at Fig. 1 (e.g., “Transport Packet Parser”)</li> </ul>
<p>[31c] providing a transform object, wherein said transform object stores and retrieves data streams onto a storage device;</p>	<p>AV7100 Preview discloses or at least renders obvious “providing a transform object that stores and retrieves data streams onto a storage device” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “traffic controller features <ul style="list-style-type: none"> <li>• Authorizes and manages direct memory access (DMA) transfers</li> <li>• Provides SDRAM interface</li> <li>• Provides memory access protection</li> <li>• Manages interrupt requests</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>TTP/DES to/from internal data RAM</li> <li>Data RAM to/from extension bus</li> <li>SDRAM to OSD</li> <li>Audio and video decoders to/from SDRAM</li> <li>SDRAM to/from data RAM</li> </ul> </li> <li>• Manages extension bus</li> <li>• Generates chip selects for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus” AV7100 Preview at 12.</li> </ul> </li> <li>• “• Firmware Controls Device Operation and Provides Application Access to Hardware Resources” AV7100 Preview at 1.</li> <li>• “The ARM is responsible for managing all hardware and software resources in the ’AV7100. . . . The ’AV7100s traffic controller handles data transfers, and the ARM provides services to true interrupts.” AV7100 at 11.</li> <li>• “The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time.” AV7100 Preview at 12.</p> <ul style="list-style-type: none"> <li>• “However, the user can employ the bitBLT hardware (which uses data RAM) as an intermediate step to execute such a transfer. AV7100 Preview at 12.</li> <li>• “The 'AV7100 provides a dedicated data interface for 1394 data.” AV7100 Preview at 51.</li> <li>• “The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus.” AV7100 Preview at 37.</li> <li>• “In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder.” AV7100 Preview at 52.</li> <li>• AV7100 Preview at Fig. 1 (e.g., “Traffic Interface Manager”)</li> <li>• See AV7100 Preview at Fig. 19 (e.g., “1394 Interface”):</li> </ul>



'389 Patent Claim	Exemplary Prior Art Disclosure
	 <p>The diagram shows a block labeled 'AV7100' at the top. Below it, on the left, is a vertical line labeled 'External Bus'. To the right of this bus is a large rectangular block containing two sub-blocks: 'DVCR Packetizer' on top and 'LINK Interface' on the bottom. A line labeled 'Data' connects the 'DVCR Packetizer' to the 'External Bus'. Below the 'LINK Interface' block is another block labeled 'PHY Interface', connected by a vertical line. The entire diagram is enclosed in a rectangular frame.</p> <p><b>Figure 19. 1394 Interface</b></p>
<p>[31d] wherein said source object obtains a buffer from said transform object, said source object converts video data into data streams and fills said buffer with said streams;</p>	<p>AV7100 Preview discloses or at least renders obvious “wherein said source object obtains a buffer from said transform object, said source object converts video data into data streams and fills said buffer with said streams” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• See Fig. 1 (e.g., “transport packet parser,” “traffic interface manager,” “SDRAM”)</li> <li>• “The 'AV7100s traffic controller handles data transfers, and the ARM provides services to true interrupts.” AV7100 Preview at 11</li> <li>• “traffic controller features             <ul style="list-style-type: none"> <li>• Authorizes and manages direct memory access (DMA) transfers</li> <li>• Provides SDRAM interface</li> <li>• Provides memory access protection</li> <li>• Manages interrupt requests</li> </ul> </li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Manages the data flow between processors and memories TTP/DES to/from internal data RAM Data RAM to/from extension bus SDRAM to OSD Audio and video decoders to/from SDRAM SDRAM to/from data RAM</li> <li>• Manages extension bus</li> <li>• Generates chip selects for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus” AV7100 Preview at 12.</li> <li>• “The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs.” AV7100 Preview at 12.</li> <li>• “Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 at 15.</li> <li>• “DRAM is read/write accessible by the ARM. It is also accessed by the traffic controller for TPP and bitBLT DMA transfers.” AV7100 Preview at 38.</li> <li>• “CS6 is read and write accessible by the ARM. It is also accessed by the traffic controller for TPP DMAs, and it is write only. The parallel port is one byte wide and accessed via the most significant byte.” AV7100 Preview at 38.</li> </ul>
[31e] wherein said source object is automatically flow controlled by said transform object;	<p>AV7100 Preview discloses or at least renders obvious “wherein said source object is automatically flow controlled by said transform object” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “traffic controller features</li> <li>• Authorizes and manages direct memory access (DMA) transfers</li> <li>• Provides SDRAM interface</li> <li>• Provides memory access protection</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>TTP/DES to/from internal data RAM</li> <li>Data RAM to/from extension bus</li> <li>SDRAM to OSD</li> <li>Audio and video decoders to/from SDRAM</li> <li>SDRAM to/from data RAM</li> </ul> </li> <li>• Manages extension bus</li> <li>• Generates chip selects for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus” AV7100 Preview at 12.</li> </ul> <ul style="list-style-type: none"> <li>• “The 'AV7100s traffic controller handles data transfers, and the ARM provides services to true interrupts. Interrupts are grouped into FIQ and I RQ categories. The system software uses FIQ; the application software uses IRQ. The priorities for FIQs and IRQs are managed by the firmware.” AV7100 Preview at 11.</li> <li>• “The ARM is responsible for managing all hardware and software resources in the 'AV7100. At powerup the ARM verifies the size of external memory. It then initializes all 'AV7100 hardware modules by setting up control registers and tables and by resetting data pointers. The ARM then executes the default firmware.” AV7100 Preview at 11.</li> <li>• “The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time.” AV7100 Preview at 12.</li> <li>• “Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SD RAM. The traffic controller repacks the data and removes voids created by the header</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>removal. The TPP also activates or deactivates the decryption engine based upon the content of the individual packet. The conditional access keys are stored in RAM and managed by firmware running on the ARM.” AV7100 Preview at 15.</p> <ul style="list-style-type: none"> <li>• “The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The 'AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder.” AV7100 Preview at 18.</li> <li>• “trick mode decoding When decoding a picture from a digital recorder, the 'AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors. During trick mode decoding, the video decoder repeats the following steps: <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li> </ul> </li> <li>• “The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. . . . The ARM initializes and controls the audio decoder via a 32-bit control register.” AV7100 Preview at 30.</li> <li>• “Firmware That Controls Device Operation and Provides Application Access to Hardware Resources” AV7100 Preview at 1.</li> <li>• AV7100 Preview at Fig. 1 (e.g., “transport packet parser,” “traffic interface manager,” “A/V core”)</li> <li>• AV7100 Preview at Fig. 2 (“AV7100 Memory Map”)</li> <li>• AV7100 Preview at Fig. 3 (“Memory Allocation of 16-Mbit SDRAM (NTSC)”)</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
<p>[31f] providing a sink object, wherein said sink object obtains data stream buffers from said transform object and outputs said streams to a video and audio decoder;</p>	<p>AV7100 Preview discloses or at least renders obvious “providing a sink object that obtains data stream buffers from said transform object and outputs said streams to a video and audio decoder” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. ... The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the 'AV7100 on-screen display (OSD) module for further blending with OSD data. In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag.” AV7100 Preview at 18.</li> <li>• “The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The 'AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization. The ARM initializes and controls the audio decoder via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and oversampling ratio, and choose the output format for dual channel mode. The ARM also reads status information from the audio decoder via a 32-bit status register which provides the MPEG header information and sync, CRC, and PCM status.” AV7100 Preview at 30.</li> <li>• “trick mode decoding When decoding a picture from a digital recorder, the 'AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures.” AV7100 Preview at 18.</li> <li>• “The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware.” AV7100 Preview at 12.</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• “traffic controller features             <ul style="list-style-type: none"> <li>• Authorizes and manages direct memory access (DMA) transfers</li> <li>• Provides SDRAM interface</li> <li>• Provides memory access protection</li> <li>• Manages interrupt requests</li> <li>• Manages the data flow between processors and memories                 <ul style="list-style-type: none"> <li>TTP/DES to/from internal data RAM</li> <li>Data RAM to/from extension bus</li> <li>SDRAM to OSD</li> <li>Audio and video decoders to/from SDRAM</li> <li>SDRAM to/from data RAM</li> </ul> </li> <li>• Manages extension bus</li> <li>• Generates chip selects for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus.” AV7100 Preview at 12.</li> </ul> </li> <li>• “DRAM is read/write accessible by the ARM. It is also accessed by the traffic controller for TPP and bitBLT DMA transfers.” AV7100 Preview at 38.</li> <li>• “• On-Chip SDRAM Controller for 16, 20, or 32-MBit SDRAM” AV7100 Preview at 1.</li> <li>• “The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SD RAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</li> <li>• “The OSD module accepts video from the video decoder, reads OSD data from SD RAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces. OSD defaults to standby mode and simply routes video from the video decoder to both outputs.” AV7100 Preview at 22.</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
<p>[31g] wherein said decoder converts said streams into display signals and sends said signals to a display;</p>	<p>AV7100 Preview discloses or at least renders obvious “wherein said decoder converts said streams into display signals and sends said signals to a display” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “video decoder features <ul style="list-style-type: none"> <li>• Real-time video decoding of MPEG-2 Main Profile and Main Level Bit Stream and MPEG-1</li> <li>• Error detection and concealment</li> <li>• Internal 90 kHz/27-MHz system time clock</li> <li>• Sustained input rate of 15 Mbps</li> <li>• Supports trick mode with full trick mode picture</li> <li>• Provides 1/4 and 1/16 decimated picture size</li> <li>• Extracts closed caption and other picture user data from the bit stream</li> <li>• 3:2 pulldown in NTSC mode</li> <li>• Supports various display formats with polyphase horizontal resampling and vertical chrominance filtering</li> <li>• Pan-and-scan for 16:9 source material according to both DSS and MPEG syntax</li> <li>• High-level command interface</li> <li>• Synchronization using presentation time stamps (PTS)</li> <li>• Half resolution display mode allows additional OSD space in the SDRAM” AV7100 Preview at 18.</li> </ul> </li> <li>• “The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The 'AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the 'AV7100 on-screen display (OSD) module for further blending with OSD data.” AV7100 Preview at 18.</li> <li>• “trick mode decoding When decoding a picture from a digital recorder, the 'AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors. During trick mode decoding, the video decoder repeats the following steps: <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> </ul> </li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li>   <li>• “The OSD module accepts video from the video decoder, reads OSD data from SD RAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces.” AV7100 Preview at 22.</li>   <li>• “The 'AV7100 provides video output signals encoded for display on a video monitor. The encoded data may include video data or blended video and OSD data.” AV7100 Preview at 26.</li>   <li>• “audio decoder features <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Supports output data in both PCM and SPDIF formats</li> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul> </li>   <li>• “The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The 'AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization. The ARM initializes and controls the audio decoder via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and oversampling ratio, and choose the output format for dual channel mode. The ARM also reads status information from the audio decoder via a 32-bit status register which provides the MPEG header information and sync, CRC, and PCM status.” AV7100 Preview at 30.</li> </ul>



'389 Patent Claim	Exemplary Prior Art Disclosure
[31h] wherein said sink object is automatically flow controlled by said transform object;	<p>AV7100 Preview discloses or at least renders obvious “wherein said sink object is automatically flow controlled by said transform object” based on at least the following exemplary disclosures:</p> <p><i>See [31e].</i></p>
[31i] providing a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system; and	<p>AV7100 Preview discloses or at least renders obvious “providing a control object that receives commands from a user, said commands control the flow of the broadcast data through the system” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “trick mode decoding When decoding a picture from a digital recorder, the 'AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors. During trick mode decoding, the video decoder repeats the following steps: <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li> </ul> </li> <li>• “The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder APIs.” AV7100 Preview at 20.</li> <li>• “audio decoder control and status registers The audio module has two registers: a read/write control register and a read-only status register. Both registers are read or written to through user software and 'AV7100 API routines.” AV7100 Preview at 31.</li> <li>• “communication coprocessor features <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> <li>• Provides three UARTs - one for smart card and two for general use</li> <li>• Accepts IR, REMOTE, and RF signals</li> <li>• Provides a REMOTE output</li> <li>• Provides two general purpose I/Os</li> </ul> </li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Manages 12C and JTAG interfaces” AV7100 Preview at 33.</li> <li>• “The communication coprocessor consists of a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR/RF, 12C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM. Interrupts are used to communicate between these interface modules and the ARM.” AV7100 Preview at 33.</li> <li>• “IR/REMOTE/RF interface The IR/RF remote control interface is a means of transmitting user commands to the set-top box. This interface consists of a custom hardware receiver implementing a bit frame-based communication protocol. A single bit frame represents a user command. The IR, RF, and REMOTEIN ports require a square wave input with no false transitions; therefore, the signal must reach its threshold prior to being applied to the pins. The interface accepts an IR, RF, or REMOTEIN data stream up to a frequency of 1.3 kHz. Since more than one data stream may be active at any given time, the 'AV7100 hardware determines priority so that only one IR, RF, or REMOTE input is decoded.” AV7100 Preview at 35.</li> <li>• “The IR/RF protocol has one receive interrupt, but it is generated to indicate two different conditions - start and finish of a user command. The first type of receive interrupt (start) is generated when the hardware interface detects a new frame. The second type of interrupt is generated when there has been no signal detected for the length of a hardware time-out period (user command time out).” AV7100 Preview at 35.</li> <li>• AV7100 Preview at Fig. 1 (e.g., “communication co-processors”)</li> <li>• <i>See</i> AV7100 Preview at Table 8 (e.g., “Freeze”):</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure																						
	<p style="text-align: center;"><b>Table 8. Video Decoder Commands</b></p> <table border="1"> <thead> <tr> <th>COMMAND</th><th>DESCRIPTION</th></tr> </thead> <tbody> <tr> <td>Play</td><td>Normal decoding</td></tr> <tr> <td>Freeze</td><td>Normal decoding, but continue to display the last picture.</td></tr> <tr> <td>Stop</td><td>Stops the decoding process. The display continues with the last picture.</td></tr> <tr> <td>Scan</td><td>Searches for the first I-picture, decodes it, continuously displays it, and flushes the buffer</td></tr> <tr> <td>NewChannel</td><td>Used for channel change. This command should be preceded by a Stop command.</td></tr> <tr> <td>Reset</td><td>Halts execution of the current command. The bit stream buffer is flushed and the video decoder performs an internal reset.</td></tr> <tr> <td>Decimate 1/2</td><td>Continues normal decoding and displays a 1/2×1/2 decimated picture (used by OSD API)</td></tr> <tr> <td>Decimate 1/4</td><td>Continues normal decoding and displays a 1/4×1/4 decimated picture (used by OSD API)</td></tr> <tr> <td>HalfResOn</td><td>Enable half resolution display mode</td></tr> <tr> <td>HalfResOff</td><td>Disable half resolution display mode</td></tr> </tbody> </table>	COMMAND	DESCRIPTION	Play	Normal decoding	Freeze	Normal decoding, but continue to display the last picture.	Stop	Stops the decoding process. The display continues with the last picture.	Scan	Searches for the first I-picture, decodes it, continuously displays it, and flushes the buffer	NewChannel	Used for channel change. This command should be preceded by a Stop command.	Reset	Halts execution of the current command. The bit stream buffer is flushed and the video decoder performs an internal reset.	Decimate 1/2	Continues normal decoding and displays a 1/2×1/2 decimated picture (used by OSD API)	Decimate 1/4	Continues normal decoding and displays a 1/4×1/4 decimated picture (used by OSD API)	HalfResOn	Enable half resolution display mode	HalfResOff	Disable half resolution display mode
COMMAND	DESCRIPTION																						
Play	Normal decoding																						
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HalfResOff	Disable half resolution display mode																						
[31j] wherein said control object sends flow command events to said source, transform, and sink objects.	<p>AV7100 Preview discloses or at least renders obvious “wherein said control object sends flow command events to said source, transform, and sink objects” based on at least the following exemplary disclosures:</p> <p><i>See</i> [31i].</p>																						
[32pre]. An apparatus for the simultaneous storage and play back of multimedia data, comprising:	<p>To the extent that the preamble is limiting, AV7100 Preview discloses or at least renders obvious “an apparatus for the simultaneous storage and play back of multimedia data” based on at least the following exemplary disclosures:</p> <p><i>See</i> claim [1pre].</p>																						
[32a] a module for accepting television (TV) broadcast signals, wherein said TV signals are based on a multitude of standards, including, but not limited to, National Television Standards Committee (NTSC) broadcast, PAL broadcast, satellite transmission, DSS, DBS, or ATSC;	<p>AV7100 Preview discloses or at least renders obvious “a module for accepting television (TV) broadcast signals, wherein said TV signals are based on a multitude of standards, including, but not limited to, National Television Standards Committee (NTSC) broadcast, PAL broadcast, satellite transmission, DSS, DBS, or ATSC” based on at least the following exemplary disclosures:</p> <p><i>See</i> claim [1a].</p>																						

'389 Patent Claim	Exemplary Prior Art Disclosure
[32b] a module for tuning said TV signals to a specific program;	AV7100 Preview discloses or at least renders obvious “a module for tuning said TV signals to a specific program” based on at least the following exemplary disclosures:  <i>See claim [1b].</i>
[32c] at least one Input Section, wherein said Input Section converts said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation;	AV7100 Preview discloses or at least renders obvious “at least one Input Section, wherein said Input Section converts said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation” based on at least the following exemplary disclosures:  <i>See claim [1c].</i>
[32d] a Media Switch, wherein said Media Switch parses said MPEG stream, said MPEG stream is separated into its video and audio components;	AV7100 Preview discloses or at least renders obvious “a Media Switch, wherein said Media Switch parses said MPEG stream, said MPEG stream is separated into its video and audio components” based on at least the following exemplary disclosures:  <i>See claim [1d].</i>
[32e] a module for storing said video and audio components on a storage device;	AV7100 Preview discloses or at least renders obvious “a module for storing said video and audio components on a storage device” based on at least the following exemplary disclosures:  <i>See claim [1e].</i>
[32f] at least one Output Section, wherein said Output Section extracts said video and audio components from said storage device;	AV7100 Preview discloses or at least renders obvious “at least one Output Section, wherein said Output Section extracts said video and audio components from said storage device” based on at least the following exemplary disclosures:  <i>See claim [1f].</i>
[32g] wherein said Output Section assembles said video and audio components into an MPEG stream;	AV7100 Preview discloses or at least renders obvious “wherein said Output Section assembles said video and audio components into an MPEG stream” based on at least the following exemplary disclosures:  <i>See claim [1g].</i>

'389 Patent Claim	Exemplary Prior Art Disclosure
[32h] wherein said Output Section sends said MPEG stream to a decoder;	AV7100 Preview discloses or at least renders obvious “wherein said Output Section sends said MPEG stream to a decoder” based on at least the following exemplary disclosures:  <i>See claim [1h].</i>
[32i] wherein said decoder converts said MPEG stream into TV output signals;	AV7100 Preview discloses or at least renders obvious “wherein said decoder converts said MPEG stream into TV output signals” based on at least the following exemplary disclosures:  <i>See claim [1i].</i>
[32j] wherein said decoder delivers said TV output signals to a TV receiver; and	AV7100 Preview discloses or at least renders obvious “wherein said decoder delivers said TV output signals to a TV receiver” based on at least the following exemplary disclosures:  <i>See claim [1j].</i>
[32k] accepting control commands from a user, wherein said control commands are sent through the system and affect the flow of said MPEG stream.	AV7100 Preview discloses or at least renders obvious “accepting control commands from a user, wherein said control commands are sent through the system and affect the flow of said MPEG stream” based on at least the following exemplary disclosures:  <i>See claim [1k].</i>
33. The apparatus of claim 32, wherein said Input Section directs said MPEG stream to the destination indicated by said control commands.	AV7100 Preview discloses or at least renders obvious “said Input Section directs said MPEG stream to the destination indicated by said control commands” based on at least the following exemplary disclosures:  <i>See claim 2.</i>
34. The apparatus of claim 32, wherein said Output Section extracts said video and audio components from the storage device indicated by said control commands.	AV7100 Preview discloses or at least renders obvious “said Output Section extracts said video and audio components from the storage device indicated by said control commands” based on at least the following exemplary disclosures:  <i>See claim 3.</i>

<b>'389 Patent Claim</b>	<b>Exemplary Prior Art Disclosure</b>
36. The apparatus of claim 32, wherein the storing and extracting of said video and audio components from said storage device are performed simultaneously.	AV7100 Preview discloses or at least renders obvious “storing and extracting of said video and audio components from said storage device are performed simultaneously” based on at least the following exemplary disclosures:  <i>See claim 5.</i>
37. The apparatus of claim 32, wherein said Media Switch calculates and logically associates a time stamp to said video and audio components.	AV7100 Preview discloses or at least renders obvious “said Media Switch calculates and logically associates a time stamp to said video and audio components” based on at least the following exemplary disclosures:  <i>See claim 6.</i>
38. The apparatus of claim 32, wherein said Media Switch extracts time stamp values from a digital TV stream and logically associates said time stamp values to said video and audio components.	AV7100 Preview discloses or at least renders obvious “said Media Switch extracts time stamp values from a digital TV stream and logically associates said time stamp values to said video and audio components” based on at least the following exemplary disclosures:  <i>See claim 7.</i>
43. The apparatus of claim 32, further comprising: a module for increasing the decoder system clock rate for fast playback or fast reverse playback	AV7100 Preview discloses or at least renders obvious “a module for increasing the decoder system clock rate for fast playback or fast reverse playback” based on at least the following exemplary disclosures:  <i>See claim 12.</i>
44. The apparatus of claim 32, further comprising: a module for decreasing the decoder system clock rate for slow playback or slow reverse playback.	AV7100 Preview discloses or at least renders obvious “a module for decreasing the decoder system clock rate for fast playback or fast reverse playback” based on at least the following exemplary disclosures:  <i>See claim 13.</i>

'389 Patent Claim	Exemplary Prior Art Disclosure
49. The apparatus of claim 32, wherein said Media Switch has a data bus connecting it to a CPU and DRAM.	AV7100 Preview discloses or at least renders obvious “said Media Switch has a data bus connecting it to a CPU and DRAM” based on at least the following exemplary disclosures:  <i>See claim 18.</i>
50. The apparatus of claim 32, wherein said Media Switch shares an address bus with a CPU and DRAM.	AV7100 Preview discloses or at least renders obvious “said Media Switch shares an address bus with a CPU and DRAM” based on at least the following exemplary disclosures:  <i>See claim 19.</i>
51. The apparatus of claim 32, wherein said Media Switch operates asynchronously and autonomously with a CPU.	AV7100 Preview discloses or at least renders obvious “said Media Switch operates asynchronously and autonomously with a CPU” based on at least the following exemplary disclosures:  <i>See claim 20.</i>
52. The apparatus of claim 32, wherein said storage device is connected to said Media Switch.	AV7100 Preview discloses or at least renders obvious “said storage device is connected to said Media Switch” based on at least the following exemplary disclosures:  <i>See claim 21.</i>
53. The apparatus of claim 32, wherein said Media Switch allows the CPU to queue up Direct Memory Access (DMA) transfers.	AV7100 Preview discloses or at least renders obvious “said Media Switch allows the CPU to queue up Direct Memory Access (DMA) transfers” based on at least the following exemplary disclosures:  <i>See claim 22.</i>
[61pre]. An apparatus for the simultaneous storage and play back of multimedia data, comprising:	To the extent that the preamble is limiting, AV7100 Preview discloses or at least renders obvious “an apparatus for the simultaneous storage and play back of multimedia data” based on at least the following exemplary disclosures:  <i>See claim [31pre].</i>

'389 Patent Claim	Exemplary Prior Art Disclosure
[61a] a physical data source, wherein said physical data source accepts broadcast data from an input device, parses video and audio data from said broadcast data, and temporarily stores said video and audio data;	AV7100 Preview discloses or at least renders obvious “a physical data source, wherein said physical data source accepts broadcast data from an input device, parses video and audio data from said broadcast data, and temporarily stores said video and audio data” based on at least the following exemplary disclosures:  <i>See claim [31a].</i>
[61b] a source object, wherein said source object extracts video and audio data from said physical data source;	AV7100 Preview discloses or at least renders obvious “a source object, wherein said source object extracts video and audio data from said physical data source” based on at least the following exemplary disclosures:  <i>See claim [31b].</i>
[61c] a transform object, wherein said transform object stores and retrieves data streams onto a storage device;	AV7100 Preview discloses or at least renders obvious “a transform object, wherein said transform object stores and retrieves data streams onto a storage device” based on at least the following exemplary disclosures:  <i>See claim [31c].</i>
[61d] wherein said source object obtains a buffer from said transform object, said source object converts video data into data streams and fills said buffer with said streams;	AV7100 Preview discloses or at least renders obvious “wherein said source object obtains a buffer from said transform object, said source object converts video data into data streams and fills said buffer with said streams” based on at least the following exemplary disclosures:  <i>See claim [31d].</i>
[61e] wherein said source object is automatically flow controlled by said transform object;	AV7100 Preview discloses or at least renders obvious “wherein said source object is automatically flow controlled by said transform object” based on at least the following exemplary disclosures:  <i>See claim [31e].</i>
[61f] a sink object, wherein said sink object obtains data stream buffers from said transform object and outputs said streams to a video and audio decoder;	AV7100 Preview discloses or at least renders obvious “a sink object, wherein said sink object obtains data stream buffers from said transform object and outputs said streams to a video and audio decoder” based on at least the following exemplary disclosures:  <i>See claim [31f].</i>



<b>'389 Patent Claim</b>	<b>Exemplary Prior Art Disclosure</b>
[61g] wherein said decoder converts said streams into display signals and sends said signals to a display;	AV7100 Preview discloses or at least renders obvious “wherein said decoder converts said streams into display signals and sends said signals to a display” based on at least the following exemplary disclosures:  <i>See claim [31g].</i>
[61h] wherein said sink object is automatically flow controlled by said transform object;	AV7100 Preview discloses or at least renders obvious “wherein said sink object is automatically flow controlled by said transform object” based on at least the following exemplary disclosures:  <i>See claim [31h].</i>
[61i] a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system; and	AV7100 Preview discloses or at least renders obvious “a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system” based on at least the following exemplary disclosures:  <i>See claim [31i].</i>
[61j] wherein said control object sends flow command events to said source, transform, and sink objects.	AV7100 Preview discloses or at least renders obvious “wherein said control object sends flow command events to said source, transform, and sink objects” based on at least the following exemplary disclosures:  <i>See claim [31j].</i>

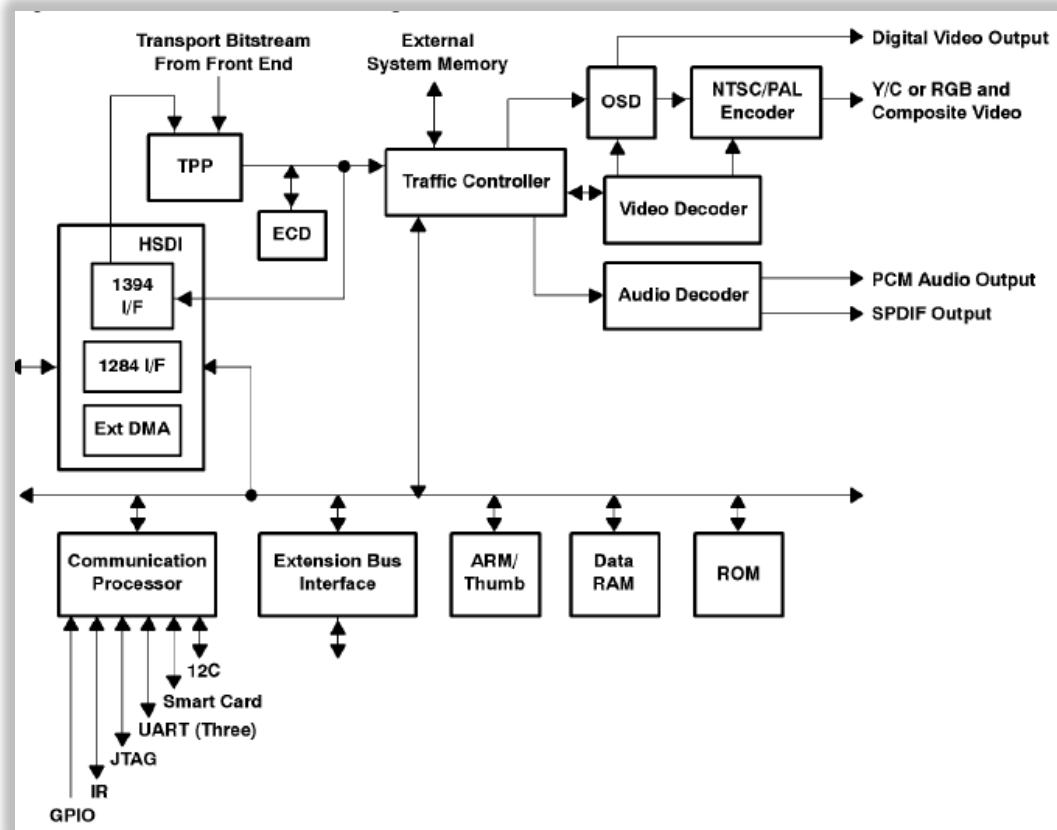
**Invalidity Contentions for U.S. Patent No. 6,233,389**  
**Based on TMS320AV7110 Product Preview by Texas Instruments (“AV7110 Preview”)**

Based upon TiVo’s Complaint, Infringement Contentions, and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered, the reference charted below anticipates or at least renders obvious the asserted claims. These invalidity contentions are not an admission by Samsung that the accused products are covered by or infringe the asserted claims, particularly when these claims are properly construed and applied. These invalidity contentions are not an admission that Samsung concedes or acquiesces to any claim construction implied or suggested by TiVo’s Complaint or Infringement Contentions. Nor is Samsung asserting any claim construction positions through these charts, including whether the preamble is a limitation. The portions of the prior art reference cited below are not exhaustive but are exemplary in nature.

<b>’389 Patent Claim</b>	<b>Exemplary Prior Art Disclosure</b>
[1pre]. A process for the simultaneous storage and play back of multimedia data, comprising the steps of:	<p>To the extent that the preamble is limiting, AV7110 Preview discloses or at least renders obvious a process for the simultaneous storage and play back of multimedia data based on at least the following exemplary disclosures:</p> <p>“The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO), and MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infra-red (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.” AV7110 Preview at 1.</p>

## '389 Patent Claim

## Exemplary Prior Art Disclosure



AV7110 Preview at 12 fig. 1.

“After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards.” AV7110 Preview at 13.

“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM  
Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PID table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.</p> <p>The only difference between the two scenarios is that in the case where there is no TPP traffic, the TPP buffer pool can be used. In the case where there is active TPP data, a general purpose buffer needs to be used. Additionally, when TPP data traffic is active, the end of packet (EOP) interrupt generation will require an indication data type configured in the header, which describes where the data to be processed is to be found.” AV7110 Preview at 21.</p> <p>“trick mode</p> <p>When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error</li> <li>• Continuously displays the decoded I frame.” AV7110 Preview at 26; <i>see id.</i> tbl. 6 (showing video decoder commands enabling trick mode functionality).</li> </ul> <p>“The HSDI supports the following concurrent data transfers.</p> <ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/program to 1394 (using dedicated I/F - see NOTE XXXX of Table 29)</li> <li>• TPP/program to decoder; 1394/OMA to/from memory</li> <li>• TPP/program to decoder; memory/DMA to/from HSDI</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/DMA to HSDI</li> <li>• TPP/program to decoder; TPP/program to 1394; memory/DMA to/from 1394</li> <li>• TPP/program to decoder; 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; TPP/DMA to 1394” AV7110 Preview at 61.</li> </ul> <p>AV7110 Preview at 61 (showing the functional blocks of the HSDI); <i>see also id.</i> at 62-65 (showing describing AV7110's reading and writing of data from/to the 1394 interface).</p> <p>“AV7110 internal data path for 1394</p> <p>In recording mode, the 'AV7110 sends either encrypted or clean packets to the 1394 interface. The packet will be transferred as soon as it arrives. When recording encrypted data, the ECO module is bypassed. In the case of recording decrypted byte, the TPP sends the encrypted part of the payload to the ECD module, and then forwards each byte to the 1394 interface. No CPU processing is done to the packet during recording. The TPP automatically modifies the header if the packet is decrypted.</p> <p>Note that the same team cannot be sent to the 1394 interface twice (such as, once after decryption, and twice as part of a full transport stream with the by-pass capability). Both Timon and the 'AV7110 support only one MPEG-2 transport stream channel on the bulky data interface.</p> <p>During playback mode, MPEG-2 transport packets coming from the 1394 interface go directly to the TPP module.</p> <p>Figure 29 shows the functional block diagram of the data flow between the TPP, ECD, and 1394 interface. Note that the major portion of the 1394 interface function is implemented in the HSDI module. Dedicated data lines are used for the 1394 interface that allows the 'AV7110 to work in different modes.</p> <ul style="list-style-type: none"> <li>• Decode/decrypt/display one channel and record it</li> <li>• Decode/decrypt/display one channel and record it encrypted (pay-per-view)</li> <li>• Decode/display one channel while recording all or part of 32 PIDs from a transponder, with each selected PIDs either encrypted or decrypted. In addition non selected PIDs can also be recorded in their original format (decryption is not possible for non selected PIDs).</li> <li>• While the TPP is receiving MPEG-2 data from the 1394 port, the 'AV7110 can also record part of the bit stream it is receiving to the 1394 port</li> <li>• Send the whole transport stream from the FEC to the 1394 port without any filtering or decryption and, at the same time, decode/decrypt/display a program from either the same transport stream or from another transport stream received through the 1394 port..” AV7110 Preview at 65.</li> </ul>

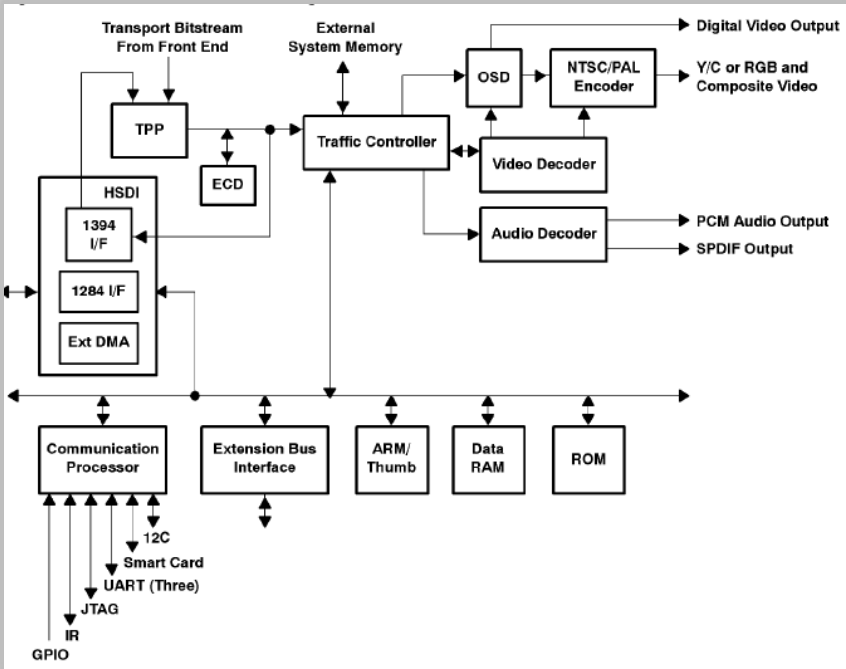
'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>AV7110 Preview at 65 fig. 29 (showing functional block diagram of data flow between TPP, ECD, and 1394 interface).</p> <p>“When configured for EDMA operation (HSDI_ STATUS[1 LO] = 01), the HSDI is capable of a glue less connection to an external enhanced SCSI controller (ESC) device such as the NCR 53CF94-1 /53CF96-1. Figure 30 shows the connections for this example configuration.</p> <p>....</p> <p>Since there is only an 8-bit bus on the HSDI, the ESC is limited to an 8-bit, single bus architecture so its mode selection inputs should be set to mode 0. The upper data bits can be left floating since they have internal pullups on the ESC. Likewise, the AD?-0 inputs of the ESC will not be used for this mode and can be left unconnected. The ESC requires an external clock source from 10 MHz to 40 MHz. Since the CLK40 signal of the 'AV7110 is actually a 40.5 MHz clock it cannot be used directly for this controller without violating its specification. Table 32 shows the signals needed for the EDMA interface.</p> <p>....</p> <p>All data transfers (using the HSDI DMA unit) as well as external controller communications (using the A[3:0] output signals), are controlled by the firmware. Firmware will handle MPEG-2 program stream and MPEG-1 system stream input. This firmware will not be available with the initial samples of the 'AV7110. The other input data formats will be handled by user application software. This includes specific interfaces such as the ESC. Table 33 details the EDMA register which allows the user to configure the wait states and other factors of the EDMA port.” AV7110 Preview at 66-67.</p>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p>The diagram, labeled 'Figure 26. 1394 Interface', shows a block diagram of the 1394 interface. At the top is a block labeled 'AV7100'. Below it, on the left, is an 'External Bus' connected to the AV7100. To the right of the External Bus is a vertical stack of three blocks: 'DVCR Packetizer' at the top, 'LINK Interface' in the middle, and 'PHY Interface' at the bottom. To the right of the DVCR Packetizer is a 'Data BD Port'. To the right of the LINK Interface is a block labeled 'TIMON (TSB12LV41)'. To the right of the PHY Interface is a block containing three ports: '1394 Port 1', '1394 Port 2', and '1394 Port 3'. Lines indicate connections: AV7100 to External Bus; External Bus to DVCR Packetizer; DVCR Packetizer to Data BD Port; DVCR Packetizer to LINK Interface; LINK Interface to TIMON; TIMON to PHY Interface; and PHY Interface to each of the three 1394 ports.</p> </div> <p>AV7110 Preview at 62 fig. 26 (showing connection between AV7110 and external packetizer, link layer controller, and physical layer device); <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) packets to and from the internal data RAM. This data can then be processed by the user software as needed.”).</p> <p>“The application software interfaces with the peripheral interface controller via RTSL API calls. To send data to the host the application software will issue an API call to transfer the data from memory to the peripheral interface via a DMA. To receive data from the host, the application software will issue an API to transfer a predetermined number of bytes from the peripheral interface to internal data memory via the HSDI DMA unit. The user application software must have a way to determine the number of bytes of data that is expected from the host.” AV7110 Preview at 70.</p>
[1a] accepting television (TV) broadcast signals, wherein said TV signals are based on a	AV7110 Preview discloses or at least renders obvious “accepting television (TV) broadcast signals, wherein said TV signals are based on a multitude of standards, including, but not limited to, National Television Standards

'389 Patent Claim	Exemplary Prior Art Disclosure
<p>multitude of standards, including, but not limited to, National Television Standards Committee (NTSC) broadcast, PAL broadcast, satellite transmission, DSS, DBS, or ATSC;</p>	<p>Committee (NTSC) broadcast, PAL broadcast, satellite transmission, DSS, DBS, or ATSC” based on at least the following exemplary disclosures:</p> <p>“The ‘AV7110 accepts a DVB transport bit-stream from the output of a Forward Error Correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet).” AV7110 Preview at 13.</p> <p>“The ARM will drive the VCXO to its center frequency during start-up or, if enabled by an API, after channel change when there is no incoming PCR.” AV7110 Preview at 13.</p> <p>“The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO), and MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infra-red (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.” AV7110 Preview at 1.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PID table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case. When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types</p>

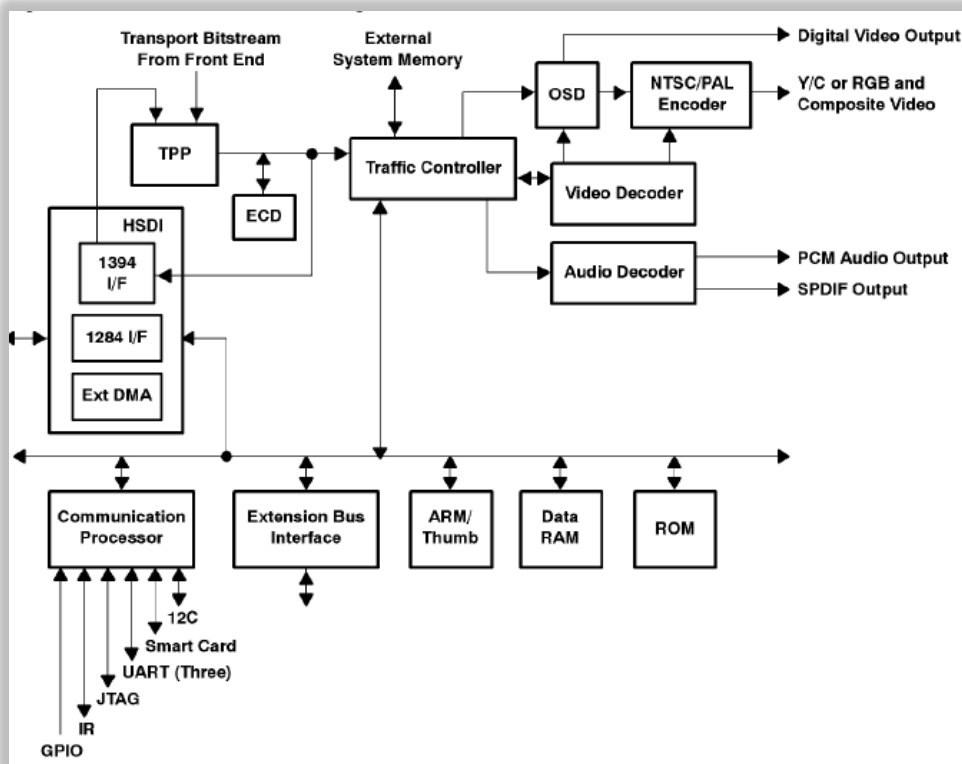


'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.” AV7110 Preview at 21.</p> <p>“Decode/display one channel while recording all or part of 32 PIDs from a transponder, with each selected PIDs either encrypted or decrypted. In addition non selected PIDs can also be recorded in their original format (decryption is not possible for non selected PIDs).” AV7110 Preview at 65.</p> <p>“transport parser input interface The ‘AV7110 accepts DVB transport packet data from a front end such as a Forward Error Correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB Conditional Access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23; <i>see also id.</i> at 24 tbl. 4 (describing transport packet input interface pin description).</p>

'389 Patent Claim	Exemplary Prior Art Disclosure
	 <p>AV7110 Preview at 12 fig. 1.</p> <p>AV7110 Preview at 26 table 6 (e.g., “NewChannel”).</p>
[1b] tuning said TV signals to a specific program;	<p>AV7110 Preview discloses or at least renders obvious “tuning said TV signals to a specific program” based on at least the following exemplary disclosures:</p> <p><i>See</i> [1a].</p>
[1c] providing at least one Input Section, wherein said Input Section converts said specific program to an Moving Pictures	<p>AV7110 Preview discloses or at least renders obvious “providing at least one Input Section, wherein said Input Section converts said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation” based on at least the following exemplary disclosures:</p>

**'389 Patent Claim**

Experts Group (MPEG) formatted stream for internal transfer and manipulation;

**Exemplary Prior Art Disclosure**

AV7110 Preview at 12 fig. 1.

“The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.” AV7110 Preview at 13.

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The TPP hardware is capable of detecting packets lost from the transport stream. With error concealment by the audio and the video decoders the ‘AV7110 minimizes the effect of lost data.” AV7110 Preview at 13.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PID table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case. When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.” AV7110 Preview at 21.</p> <p>“MPEG transport decoder (TPP) TPP module features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps</p> <p>Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps</p> <p>Maximum input bit rate through the 1394 interface ..... 64.8 Mbps</p> <p>Maximum video bit rate ..... 15 Mbps</p>

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	<p>Maximum audio bit rate ..... 1.13 Mbps</p> <p>Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec</p> <p>Maximum number of PIDs that can be filtered ..... 32</p> <p>Maximum number of PIDs that can be descrambled ..... 32</p> <p>Maximum number of pairs of keys for the descrambler ..... 16</p> <p>Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PID and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PID at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination. The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p>

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	<p>“transport parser input interface  The ‘AV7110 accepts DVB transport packet data from a front end such as a Forward Error Correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB Conditional Access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23; <i>see also id.</i> at 24 tbl. 4 (describing transport packet input interface pin description).</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SDRAM, and produces three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs. After being configured and activated by the ARM CPU, the OSD module reads OSD data and mixes it with the video output. The CPU is responsible for turning on and off OSD operations. The bitBLT hardware which is attached to the OSD module provides acceleration for memory block moves and graphics operations.” AV7110 Preview at 33.</p> <div> <pre> graph LR     OSDData[OSD Data] --&gt; FIFO[FIFO]     FIFO --&gt; OSDL1[OSD Component Latch]     VideoDecoder[Video Decoder] --&gt; OSDL2[OSD Component Latch]     OSDL1 --&gt; CLUT[CLUT and Window Attributes]     OSDL2 --&gt; CLUT     CLUT --&gt; OCS[Output Channel Selection]     OCS --&gt; Ch0[Analog CVBS]     OCS --&gt; Ch2[Analog RGB]     OCS --&gt; Ch1[Digital Y/C]     XPos[X Position] --&gt; WinSel[Window Selection]     YPos[Y Position] --&gt; WinSel     WinSel --&gt; DispCtrl[Display Control]     DispCtrl --&gt; Blending[Blending]     Blending --&gt; OCS </pre> <p>The diagram illustrates the OSD module architecture. It starts with 'OSD Data' entering a 'FIFO' block, which then feeds into an 'OSD Component Latch'. Simultaneously, 'Video Decoder' output goes into another 'OSD Component Latch'. Both latches feed into a 'CLUT and Window Attributes' block. This block's output goes to an 'Output Channel Selection' block, which drives three output channels: 'Analog CVBS' (labeled Ch0), 'Analog RGB' (labeled Ch2), and 'Digital Y/C' (labeled Ch1). Additionally, 'X Position' and 'Y Position' inputs feed into a 'Window Selection' block, which outputs to a 'Display Control' block. The 'Display Control' block feeds into a 'Blending' block, which then feeds into the 'Output Channel Selection' block.</p> </div> <p>AV7110 Preview at 33 fig. 8 (showing block diagram of the OSD module).</p>

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	<div> </div> <p>AV7110 Preview at 36 fig. 9.</p> <p>“video output interfaces</p> <p>analog video output - NTSC/PAL encoder module</p> <ul style="list-style-type: none"> <li>• Supports NTSC and PAL B, D, G/H, and I display formats</li> <li>• Outputs Y/C or RGB, and composite video with 9-bit DACs</li> <li>• Generates 100/75 format color bar for PAL mode testing</li> <li>• Complies to the RS170A standard</li> <li>• Composite and RGB signals comply with ITU-R BT.470-3 and ITUR BT.471-1</li> <li>• Supports Macro Vision anti-taping function on composite video</li> <li>• Provides sync signals with option to accept external sync signals</li> </ul> <p>The composite video output can be either PAL or NTSC format. The default output format is PAL at powerup. Changing between NTSC and PAL mode can be done via an API which selects the output mode of the NTSC/PAL encoder. Note that the video decoder microcode ROM is specific to NTSC or PAL and required for proper operation.</p> <p>The sync signal pins Vsync and Hsync on the 'AV7110 are defaulted to 3-state mode at powerup, where internally generated sync signals will be used by the NTSC/PAL encoder. The user can then select the source of video sync signals via an API. If internal source is selected then the Vsync and Hsync pins will be configured as output pins.</p>

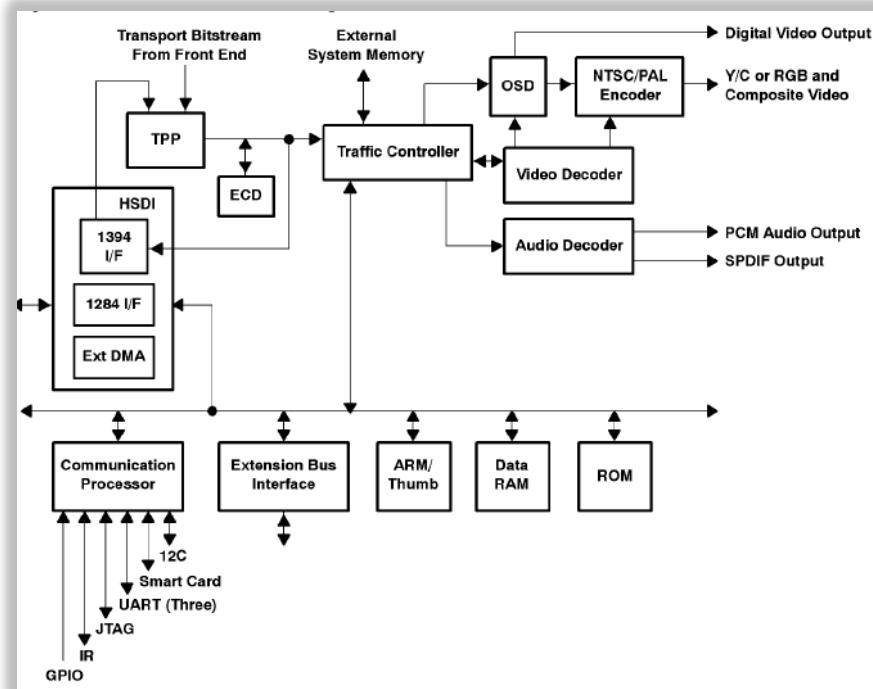
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	<p>In addition to composite video, the 'AV7110 also provides either an analog S-video (Y - luminance , C - chrominance) signal or an analog RGB output with 720 pixel resolution. All outputs conform to the RS170A standard. Selection of RGB or S-video output is done via API software. Macro Vision version 7 is enabled via an API; the default state is off. A version of the 'AV7110 where the MacroVision anti-taping circuitry is permanently disabled is also available.” AV7110 Preview at 39.</p> <p>“digital video output (not supported when 32-bit EBI is used)  PAL mode digital video output  The digital output is in 4:2:2 component format. The content of the video could be either pure video or the blended combination of video and OSD. The pin assignments for the digital video output signals are:  YCOUT(8) 8-bit Cb/Y/Cr/Y data output  YCCLK(1) 27 MHz clock output  The timing of 4:2:2 digital video output is shown in Figure 12.  ...  NTSC mode digital video output  The digital output includes video in either 4:4:4 or 4:2:2 component format, plus the aspect ratio VARIS code at the beginning of each video frame. The video output format is programmable by the user but defaults to 4:2:2. The content of the video could be either pure video or the blended combination of video and OSD.  The pin assignments for the digital video output signals are:  YCOUT(8) 8-bit Cb/Y/Cr/Y and VARIS multiplexed data output  YCCLK(1) 27 MHz clock output  YCCTRL(2) 2-bit control signals to distinguish between Y/Cb/Cr components and VARIS code  The interpretation of YCCTRL is defined in Table 20. . . .” AV7110 Preview at 41.</p> <p>“PCM audio output  The PCM audio output from the 'AV7110 is a serial PCM data line, with associated bit clock (ASCLK) and left/right clock (LRCLK). PCM data is output serially on PCM OUT using the serial clock ASCLK as shown in Figure 15. The data output of PCM OUT alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7110 Preview at 46; <i>see generally id.</i> at 46-47 (describing additional aspects of PCM audio output).</p> <p>“elementary stream playback</p>



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	<p>In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.</p> <p>SPDIF audio output</p> <p>The SPDIF output conforms to the consumer format of the AES3 standard for serial transmission of digital audio data. When using an external PLL (PCMSRC=1), SPDIF is supported only if Bx over-sampled PCMCLK is supplied (that is, PCMSEL[0]=1).” AV7110 Preview at 48.</p> <p><i>See [1a].</i></p>
[1d] providing a Media Switch, wherein said Media Switch parses said MPEG stream, said MPEG stream is separated into its video and audio components;	<p>AV7110 Preview discloses or at least renders obvious “providing a Media Switch, wherein said Media Switch parses said MPEG stream, said MPEG stream is separated into its video and audio components” based on at least the following exemplary disclosures:</p>

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AV7110 Preview at 12 fig. 1.

“traffic controller (TC)

features

- Manages interrupt requests
- Authorizes and manages DMA transfers
- Provides SDRAM interface
- Manages extension bus
- Provides memory access protection
- Manages the data flow between processors and memories
  - TPP to/from internal data RAM
  - Data RAM to/from extension bus
  - SDRAM to OSD

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- OSD to/from internal data RAM
- Audio/video decoder to/from SDRAM
- SDRAM to/from internal data RAM
- High speed data interface to/from internal data RAM
- Generates chip selects (CS) for all internal modules and devices on the extension bus
- Generates programmable wait states for devices on the extension bus
- Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.

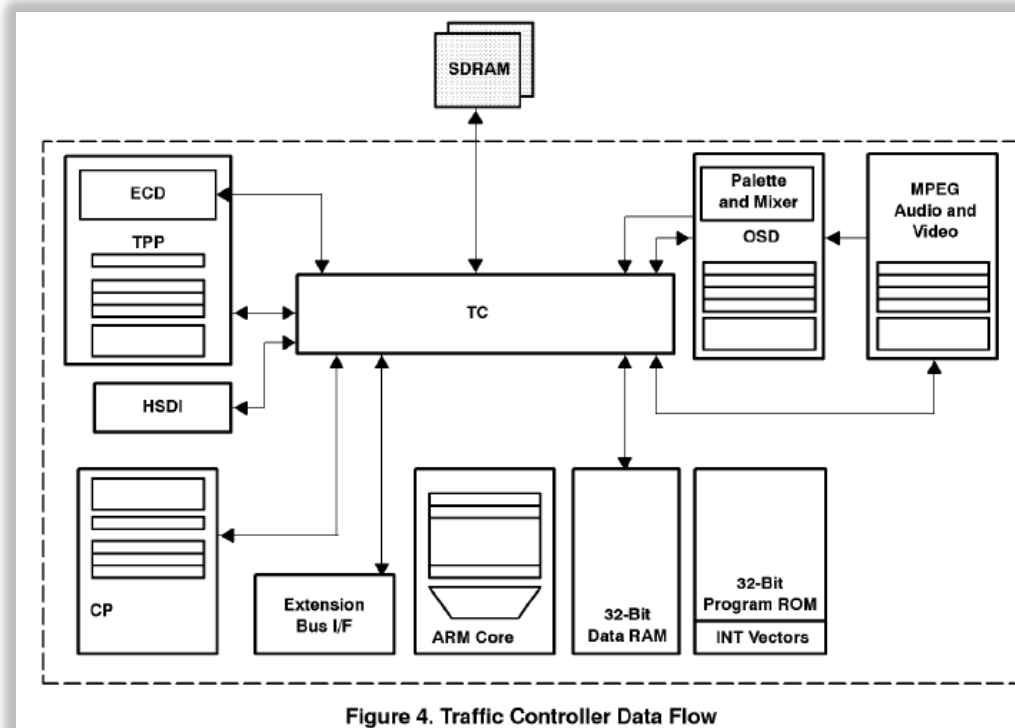


Figure 4. Traffic Controller Data Flow

AV7110 Preview at 18 fig. 4.

“extension bus interface (EBI)

The extension bus interface is a 32-bit or 16-bit bidirectional data bus with a 25-bit address. It also provides 3 external interrupts and a wait line. All the external memories or I/O devices are mapped to the 32-bit address

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space of the ARM. There are six internally generated chips selects (CSx) for devices such as EEPROM memory, modem, front panel, front panel, front end control, parallel output port, and 1394 link device. Each CS has its own defined memory space and a programmable wait register which has a default of maximum allowable values as defined in Table 27. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. These are all programmable by user application software using APIs.” AV7110 Preview at 50.

“CS1 is intended for ARM application code, but writes will not be prevented. CS2, CS3, CS4, and CS5 all have the same characteristics. The ARM performs reads and writes to these devices through the extension bus. CS6 is read and write accessible by the ARM. It is also accessed by the TC for TPP DMAs, and it is write only. User C application software selects the PID of the packets to be sent through this port, the TPP will then send the data Q via DMAs. The parallel port is one byte wide and it is accessed via the least significant byte.” AV7110 Preview at 51.

**Table 27. An Example of Extension Bus Chip Select Assignment**

CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE
CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)
N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)
N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)
CS2	3000 0000 – 31FF FFFF	1 – 7	Modem
CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel
CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port

AV7110 Preview at 51 tbl. 27.

“The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it has to become active before the programmable wait cycle expires. If the combined total wait states exceeds its maximum, the decoder is not guaranteed to function properly. The EXTWAIT signal is synchronized internally with the on-chip 81 MHz clock. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT

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	<p>signal should be at least 24.7 ns. Since the EXTWAIT signal has the potential to stall the whole decoding process, the ARM will cap its wait to 500 ns. Afterwards, the ARM assumes the device that generated the EXTWAIT has failed and will ignore EXTWAIT from then on. Only a software or hardware reset can activate the EXTWAIT signal again. The timing diagram shown in Figure 19 is an example of a read using the EXTWAIT signal.” AV7110 Preview at 53.</p> <p>“The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 32-bit or 16-bit data and 25-bit address. It also supports DMA transfers to/from the extension bus. DMA transfers within the extension bus are not supported directly. They may be accomplished from user application software by using one DMA to the internal data RAM, followed by a second DMA to transfer back to the EBI. Extension bus single read and write cycle timings are shown in Figure 17 and Figure 18 respectively.” AV7110 Preview at 51; <i>see also id.</i> at 52 figs. 17 and 18.</p> <p>“The descrambling of the incoming data is performed automatically with minimum intervention by the CPU. The TPP module detects which transport packets are scrambled, at either the program elementary stream (PES) or the transport stream level, and routes the data through the ECD as necessary. The ECD stores the descrambler keys locally and automatically selects the correct key of a specific PID. Up to 16 sets of keys are stored in the key table for use by the ECD. It is possible for more than one PID to use the same key. The descrambler keys are derived by the conditional access software using the command packet from the bit-stream.” AV7110 Preview at 23.</p> <p>“The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.</p> <p>Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM,</p>

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	<p>and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.” AV7110 Preview at 13.</p> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PID and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PID at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.” AV7110 Preview at 22.</p> <p>Together with the ARM, the TPP also handles program clock reference (PCR) recovery with an external VCXO. The TPP will latch and transfer to the ARM its internal system clock upon the arrival of any packet which contains a PCR. After further processing on the packet and identifying the system clock, the ARM calculates the difference between the system clock from a bit-stream and the actual system clock at the time the packet arrives. Then, the ARM filters the difference and sends it through an 8-bit sigma-delta DAC to control the external VCXO. The ARM will drive the VCXO to its center frequency during start-up or, if enabled by an API, after channel change when there is no incoming PCR.” AV7110 Preview at 13.</p> <p>“At startup the hardware STC counter is free running and the increments to the software extension of the system STC take place every 1 .4 ms. Both audio and video decoders are initialized to free-run. This condition is identical for system startup as well as for re-synchronization after a channel change. Once a PCR channel is activated by user software through an API, the on-chip software will monitor the incoming data in the PCR designated channel and reset the system common reference counter STCs<sub>sys</sub> to the first PCR that arrives in the designated stream (full 42 bits). At the same time, the video and audio STC are initialized to the same value, if they are enabled via the appropriate API calls.” AV7110 Preview at 48.</p> <p>“Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a</p>

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	<p>PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PC Rs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“The video synchronization of STC and PTS can be enabled/disabled via an API. The STC for the video decoder is clocked by the 27 MHz system clock. The initial value of the video STC (STCvid) is written to the video decoder from the firmware. This happens at the time that the first PCR from the designated PCR channel arrives at the AF. In some cases the PTS can consistently be off by a certain amount, causing the video buffer to eventually over- or under-run. If this occurs, the firmware will detect the under/over-runs via FIQ-s and adjust the video STC with an offset, such that the under/over-run ceases.” AV7110 Preview at 50.</p> <p>“Together with the ARM, the TPP also handles program clock reference (PCR) recovery with an external VCXO.</p> <p>The TPP will latch and transfer to the ARM its internal system clock upon the arrival of any packet which contains a PCR. After further processing on the packet and identifying the system clock, the ARM calculates the difference between the system clock from a bit-stream and the actual system clock at the time the packet arrives. Then, the ARM filters the difference and sends it through an 8-bit sigma-delta DAC to control the external VCXO. The ARM will drive the VCXO to its center frequency during start-up or, if enabled by an API, after channel change when there is no incoming PCR.” AV7110 Preview at 13; <i>see also id.</i> at 22-23.</p> <p>“The 'AV7110 uses the STC and PTS to determine the play back time of the decoded audio and video data. The relationship between STC and PTS is determined at the time of the generation of the generation of the respective elementary streams (ES). Upon reception, the demultiplexing software in the 'AV7110 extracts the video PTS and inserts it in an array of PTS and byte-count information maintained for the video decoder. For the audio the PTS information is extracted by the audio decoder front end from the PES. The video decoder contains an STC counter that is clocked by the system clock (27 MHz) and normalized to a 90 kHz reference. The audio decoder does not contain a counter. Instead, it gets updated from the system time reference counter every 1 .4 ms.” AV7110 Preview at 48.</p> <p>“The audio synchronization of STC and PTS can be enabled/disabled through an API. The STC for the audio decoder time reference is loaded by the firmware every time the system reference counter (STCsys) rolls over. This roll over will occur every 26 ticks of the 90 kHz portion of the hardware system clock counter in the</p>

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	<p>AV7110. This is approximately every 1.4 ms. The firmware will receive an FIQ from the counter and write STCsyst + aud_offset to the STC register in the audio decoder. The value for aud_offset is 0 by default after initialization and after audio channel change.” AV7110 Preview at 49.</p> <p>“IEEE 1394 interface On power-up the IEEE 1394 interface is enabled on the HSDI. An API call can be used to configure the HSDI for another mode or to return to the 1394 interface if necessary. To complete the 1394 implementation, the 'AV7110 requires an external packetizer and link layer controller, and a physical layer device. Figure 26 shows the connection between the 'AV7110 and these devices.” AV7110 Preview at 62; <i>see id.</i> at fig. 26.</p> <p>“IEEE 1284 interface The IEEE 1284 interface on the 'AV7110 has the following characteristics:</p> <ul style="list-style-type: none"> <li>• Supports transfer of up to 10 Mbits/sec</li> <li>• Supports the compatibility, nibble and byte mode</li> <li>• Supports the ECP mode except for run length coding compression</li> <li>• Does not support the EPP mode</li> <li>• Peripheral mode only</li> </ul> <p>The IEEE 1284 interface is used to connect the 'AV7110 to an external host. The 'AV7110 side of the protocol can be handled by an IEEE 1284 peripheral interface controller on the chip such as the SN54ACT1284/SN74ACT1284. Since the signals on the HSDI are 5-V-tolerant, they can be connected directly to this external 1284 driver.” AV7110 Preview at 69; <i>see id.</i> fig.33; <i>see also id.</i> at 69-70.</p> <p>“high speed data interface (HSDI) The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device. Logic for these three interfaces share signal pins and hence only one can be active at any given time. Table 28 shows the pin definitions for the HSDI in its various configurations. Switching from one interface to another will require a predefined sequence of API calls. Two signal pins (HSDI_STATUS[1:0]) indicate which of the three interfaces is active. They can be used to control external logic for interface arbitration. The definition of these signals is shown at the bottom of Table 28.” AV7110 Preview at 60.</p> <p>“The 32-bit ARM processor running at 40.5 MHz and its associated firmware provide the following:</p> <ul style="list-style-type: none"> <li>• Initialization and management of all hardware modules</li> </ul>



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	<ul style="list-style-type: none"> <li>• Service for selected interrupt generated by hardware modules and I/O ports</li> <li>• Application program interface (API) for users to develop their own applications” AV7110 Preview at 15.</li> </ul> <p>“The CPU in the 'AV7110 is a 32-bit RISC processor, the ARM7TDM I/Thumb, which has the capability to execute instructions in 16- or 32-bit format at a clock frequency of 40.5 MHz. The regular ARM instructions are exactly one word (32-bit) long, and the data operations are only performed on word quantities. The LOAD and STORE instructions however, can transfer either byte, half-word or word quantities.</p> <p>The Thumb uses the same 32-bit architecture with an 16-bit instruction set. That is, it retains the 32-bit performance but reduces the code size with 16-bit instructions. With 16-bit instruction, the Thumb still gives 70-80% of the performance of the ARM when running ARM instructions from 32-bit memory.” AV7110 Preview at 15; <i>see also id.</i> (stating that ARM and Thumb are used interchangeably in the AV7110 Preview’s disclosure).</p> <p>“The 'AV7110 includes three general purpose UARTs that are memory mapped and fully accessible by user application programs. A set of APIs exists to assist in programming them. The output of the UARTs are digital and require external level shifters for RS232 compliance. These UARTs support full duplex mode and are double buffered with sufficient FIFO space to minimize the interrupt frequency to the ARM even when they are operating at their maximum transmission speeds.” AV7110 Preview at 75.</p> <p>“general purpose I/Os</p> <p>The 'AV7110 has four dedicated (101, 102, 104, and 105) and five multiplexed general purpose I/O pins (103 and 106 to 109) which are user configurable. Each I/O port has its own 32-bit control/status register, IOCSRn, where n ranges from 1 to 9.</p> <p>If an I/O is configured as an input and the delta interrupt mask is cleared, an IRQ is generated whenever an input changes state. If the delta interrupt mask is set, interrupts to the ARM are disabled. If no other device drives the I/O pin while it is configured as an input, it will be held high by an internal pullup resistor.</p> <p>If an I/O is configured as an output (by setting the cio bit in the corresponding control/status register), the value contained in the io_out) bit of the control/status register is output. Interrupt generation is disabled when an I/O is configured as an output.” AV7110 Preview at 77; <i>see also id.</i> tbl. 37.</p> <p>“Hardware is provided on the 'AV7110 to generate drive signal on the output pin according to input data bit and format control signals provided by user software or to just retransmit the input signal received at the IR input port. External buffering is required to drive an IR LED.</p>

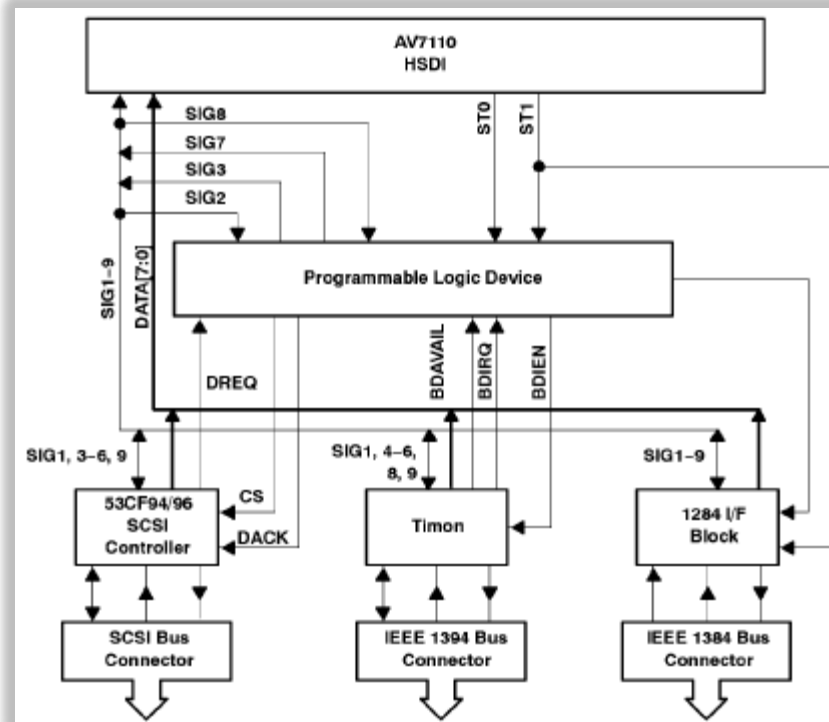
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	<p>In order to communicate with IR receivers of different IR formats, the 'AV7110s IR output encoder supports a very flexible IR frame format. The format of the frame is specified through APIs and can be changed as frequently as per IR command transmission.” AV7110 Preview at 75.</p> <p>“The smart card interface on the 'AV7110 supports clock frequencies of: 2.025, 3.375, 4.05, 4.5, 6.0, 6.75, 8.1, and 13.5 MHz. All these clock frequencies are generated internally from the 81 MHz clock.” AV7110 Preview at 72.</p> <p>“Since there is only an 8-bit bus on the HSDI, the ESC is limited to an 8-bit, single bus architecture so its mode selection inputs should be set to mode 0. The upper data bits can be left floating since they have internal pullups on the ESC. Likewise, the AD-0 inputs of the ESC will not be used for this mode and can be left unconnected. The ESC requires an external clock source from 10 MHz to 40 MHz. Since the CLK40 signal of the 'AV7110 is actually a 40.5 MHz clock it cannot be used directly for this controller without violating its specification. Table 2 shows the signals needed for the EDMA interface.” AV7110 Preview at 66; <i>see id.</i> tbl. 32 (listing DMA interface signals).</p> <p>“high speed data interface (HSDI) The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device. Logic for these three interfaces share signal pins and hence only one can be active at any given time. Table 28 shows the pin definitions for the HSDI in its various configurations. Switching from one interface to another will require a predefined sequence of API calls. Two signal pins (HSDI_ STATUS[1:0) indicate which of the three interfaces is active. They can be used to control external logic for interface arbitration. The definition of these signals is shown at the bottom of Table 28.” AV7110 Preview at 60.</p>



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	<p>On power-up the IEEE 1394 interface is enabled on the HSDI. An API call can be used to configure the HSDI for another mode or to return to the 1394 interface if necessary. To complete the 1394 implementation, the 'AV7110 requires an external packetizer and link layer controller, and a physical layer device. Figure 26 shows the connection between the 'AV7110 and these devices.” AV7110 Preview at 62; see id. at fig. 26.</p> <p>“IEEE 1284 interface The IEEE 1284 interface on the 'AV7110 has the following characteristics:</p> <ul style="list-style-type: none"> <li>• Supports transfer of up to 10 Mbits/sec</li> <li>• Supports the compatibility, nibble and byte mode</li> <li>• Supports the ECP mode except for run length coding compression</li> <li>• Does not support the EPP mode</li> <li>• Peripheral mode only</li> </ul> <p>The IEEE 1284 interface is used to connect the 'AV7110 to an external host. The 'AV7110 side of the protocol can be handled by an IEEE 1284 peripheral interface controller on the chip such as the SN54ACT1284/SN? 4ACT1284. Since the signals on the HSDI are 5-V-tolerant, they can be connected directly to this external 1284 driver.” AV7110 Preview at 69; see id. fig.33; see also id. at 69-70.</p> <p>AV7110 Preview at 62; <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) C packets to and from the internal data RAM. This data can then be processed by the user software as needed.”); <i>see also id.</i> at 63 (listing signals associated with the 1394 interface).</p> <p>“external DMA interface (EDMA) When configured for EDMA operation (HSDI_ STATUS[1 LO] = 01), the HSDI is capable of a glue less connection to an external enhanced SCSI controller (ESC) device such as the NCR 53CF94-1 /53CF96-1. Figure 30 shows the connections for this example configuration.” AV7110 Preview at 66.</p>

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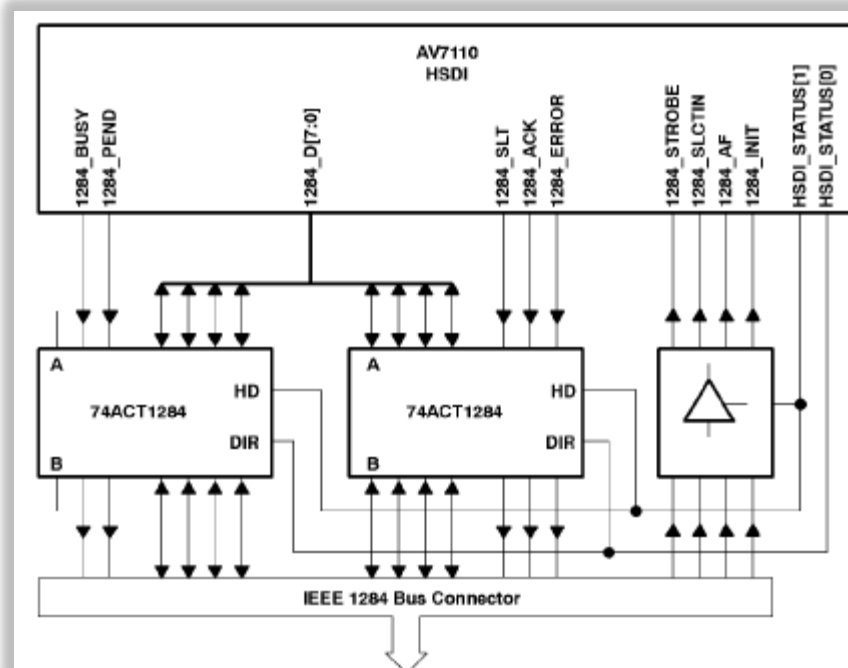


AV7110 Preview at 71 fig. 34; *see id.* (“In this example, the logic is grouped into a single programmable logic device. For simplicity, some of the HSDI signal names have been shorted (i.e., ST1 and ST0 to represent HSDI\_STATUS[1 :0], etc.). Note that the 1284 interface block is completely disabled (tri-stated) when it is not selected and so can be directly connected to the HSDI bus.”).

*See* AV7110 Preview at 1 (stating that the AV7110 includes a “[c]onfigurable High Speed Data Interface to Connect to Either an IEEE 1394 Link Device, an IEEE 1284 Interface, or an External DMA Device Like SCSI that Supports Up to 16 Mbps Data Rate”).

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AV7110 Preview at 69; *see also id.* at 70 tbl. 34 (listing signals associated with IEEE 1284 interface).

“The application software interfaces with the peripheral interface controller via RTSL API calls. To send data to the host the application software will issue an API call to transfer the data from memory to the peripheral interface via a DMA. To receive data from the host, the application software will issue an API to transfer a predetermined number of bytes from the peripheral interface to internal data memory via the HSDI DMA unit. The user application software must have a way to determine the number of bytes of data that is expected from the host.” AV7110 Preview at 70.

“combining the 1394, 1284 and external controller interfaces

With additional external logic it is possible to combine the three HSDI interfaces within a single design. Note that performing the API call to switch between interfaces will involve resetting the HSDI and so transfers between interfaces are not practical (i.e., 1394 to 1284). Switching between HSDI modes should be detected by external logic and proper care should be taken to prevent contention between the external devices and the HSDI

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	<p>interface. Figure 34 shows the block diagram of an example of this configuration based on the devices used previously.” AV7110 Preview at 70.</p> <p>“conditional access and descrambling processing The 'AV7110 contains a full implementation of the ECD hardware. The descrambling of the incoming data is performed automatically with minimum intervention by the CPU. The TPP module detects which transport packets are scrambled, at either the program elementary stream (PES) or the transport stream level, and routes the data through the ECD as necessary. The ECD stores the descrambler keys locally and automatically selects the correct key of a specific PID. Up to 16 sets of keys are stored in the key table for use by the ECD. It is possible for more than one PID to use the same key. The descrambler keys are derived by the conditional access software using the command packet from the bit-stream.” AV7110 Preview at 23.</p> <p>AV7110 Preview at 62; see id. (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) C packets to and from the internal data RAM. This data can then be processed by the user software as needed.”); see also id. at 63 (listing signals associated with the 1394 interface).</p>
[1e] storing said video and audio components on a storage device;	<p>AV7110 Preview discloses or at least renders obvious “storing said video and audio components on a storage device” based on at least the following exemplary disclosures:</p> <p>“After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards. The chip decodes MPEG-1 and MPEG-2 main profile at main level for video and Layer I and II MPEG-1 and MPEG-2 stereo for audio. Both video and audio decoders synchronize their presentation of reconstructed data using the transmitted presentation time stamps (PTS) and their local system clock. The local system clock is continuously updated by the ARM.” AV7110 Preview at 13.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport</p>

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	<p>packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PID table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.</p> <p>The only difference between the two scenarios is that in the case where there is no TPP traffic, the TPP buffer pool can be used. In the case where there is active TPP data, a general purpose buffer needs to be used. Additionally, when TPP data traffic is active, the end of packet (EOP) interrupt generation will require an indication data type configured in the header, which describes where the data to be processed is to be found.” AV7110 Preview at 21.</p> <p>“trick mode</p> <p>When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error <ul style="list-style-type: none"> <li>• Continuously displays the decoded I frame.”</li> </ul> </li> </ul> <p>AV7110 Preview at 26; <i>see id.</i> tbl. 6 (showing video decoder commands enabling trick mode functionality).</p> <p>“The HSDI supports the following concurrent data transfers.</p> <ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/program to 1394 (using dedicated I/F - see NOTE XXXX of Table 29)</li> <li>• TPP/program to decoder; 1394/DMA to/from memory</li> <li>• TPP/program to decoder; memory/DMA to/from HSDI</li> </ul>



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	<ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/DMA to HSDI</li> <li>• TPP/program to decoder; TPP/program to 1394; memory/DMA to/from 1394</li> <li>• TPP/program to decoder; 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; TPP/DMA to 1394” AV7110 Preview at 61.</li> </ul> <div> <p style="text-align: center;"><b>Figure 25. Functional Block Diagram of High Speed Data Interface</b></p> </div> <p>AV7110 Preview at 61 (showing the functional blocks of the HSDI); <i>see also id.</i> at 62-65 (showing describing AV7110’s reading and writing of data from/to the 1394 interface).</p> <p>“AV7110 internal data path for 1394</p> <p>In recording mode, the 'AV7110 sends either encrypted or clean packets to the 1394 interface. The packet will be transferred as soon as it arrives. When recording encrypted data, the ECD module is bypassed. In the case of recording decrypted byte, the TPP sends the encrypted part of the payload to the ECD module, and then forwards each byte to the 1394 interface. No CPU processing is done to the packet during recording. The TPP automatically modifies the header if the packet is decrypted.</p> <p>Note that the same bit stream cannot be sent to the 1394 interface twice (such as, once after decryption, and twice as part of a full transport stream with the by-pass capability). Both Timon and the 'AV7110 support only one MPEG-2 transport stream channel on the bulky data interface.</p> <p>During playback mode, MPEG-2 transport packets coming from the 1394 interface go directly to the TPP module.</p> <p>Figure 29 shows the functional block diagram of the data flow between the TPP, ECD, and 1394 interface. Note</p>

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	<p>that the major portion of the 1394 interface function is implemented in the HSDI module. Dedicated data lines are used for the 1394 interface that allows the 'AV7110 to work in different modes.</p> <ul style="list-style-type: none"> <li>• Decode/decrypt/display one channel and record it</li> <li>• Decode/decrypt/display one channel and record it encrypted (pay-per-view)</li> <li>• Decode/display one channel while recording all or part of 32 PIDs from a transponder, with each selected PIDs either encrypted or decrypted. In addition non selected PIDs can also be recorded in their original format (decryption is not possible for non selected PIDs).</li> <li>• While the TPP is receiving MPEG-2 data from the 1394 port, the 'AV7110 can also record part of the bit stream it is receiving to the 1394 port</li> <li>• Send the whole transport stream from the FEC to the 1394 port without any filtering or decryption and, at the same time, decode/decrypt/display a program from either the same transport stream or from another transport stream received through the 1394 port..” AV7110 Preview at 65.</li> </ul> <div> <p style="text-align: center;"><b>Figure 25. 1394 Data Flow Block Diagram</b></p> </div> <p>AV7110 Preview at 69 fig. 25 (showing functional block diagram of data flow between TPP, ECD, and 1394 interface).</p> <p>“Since there is only an 8-bit bus on the HSDI, the ESC is limited to an 8-bit, single bus architecture so its mode selection inputs should be set to mode 0. The upper data bits can be left floating since they have internal pullups on the ESC. Likewise, the AD<sup>7</sup>-0 inputs of the ESC will not be used for this mode and can be left unconnected. The ESC requires an external clock source from 10 MHz to 40 MHz. Since the CLK40 signal of the 'AV7110 is</p>

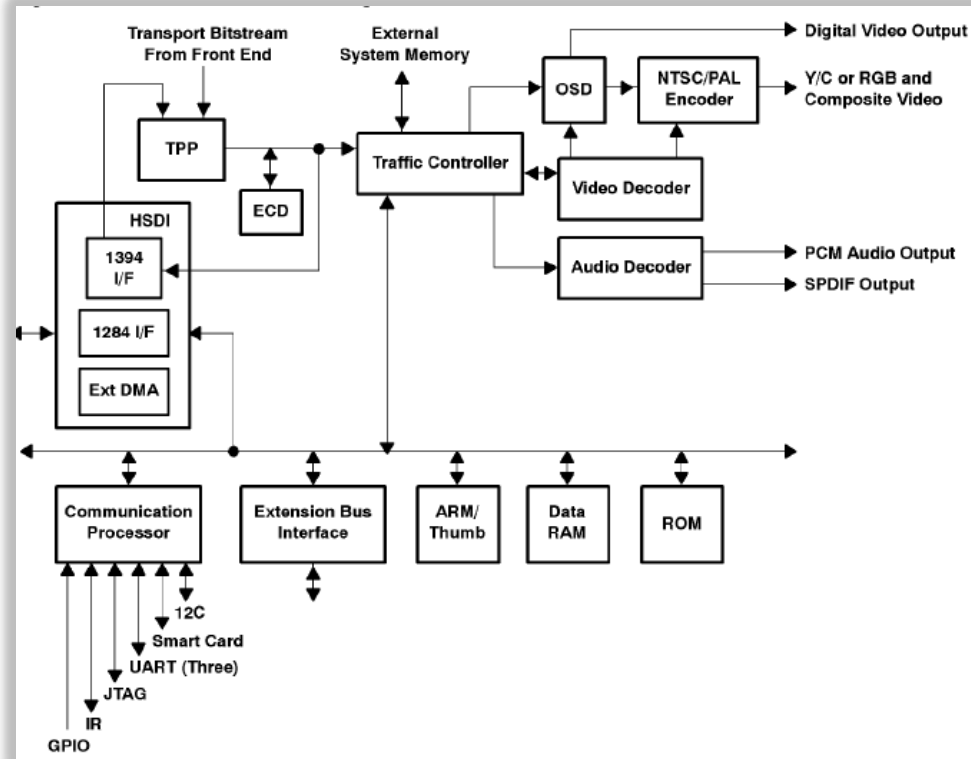
'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>actually a 40.5 MHz clock it cannot be used directly for this controller without violating its specification. Table 32 shows the signals needed for the EDMA interface.” AV7110 Preview at 66; <i>see id.</i> tbl. 32 (listing EDMA interface signals).</p> <p>“When configured for EDMA operation (HSDI_ STATUS[1 LO] = 01), the HSDI is capable of a glue less connection to an external enhanced SCSI controller (ESC) device such as the NCR 53CF94-1 /53CF96-1. Figure 30 shows the connections for this example configuration.</p> <p>....</p> <p>All data transfers (using the HSDI DMA unit) as well as external controller communications (using the A[3:0] output signals), are controlled by the firmware. Firmware will handle MPEG-2 program stream and MPEG-1 system stream input. This firmware will not be available with the initial samples of the 'AV7110. The other input data formats will be handled by user application software. This includes specific interfaces such as the ESC. Table 33 details the EDMA register which allows the user to configure the wait states and other factors of the EDMA port.” AV7110 Preview at 66, 67.</p> <div> <p>The diagram, labeled 'Figure 26. 1394 Interface', shows the internal architecture of the AV7100. At the top is a horizontal bar representing the AV7100 chip. Below it, an 'External Bus' is connected to a vertical stack of three components: a 'DVCR Packetizer', a 'LINK Interface', and a 'PHY Interface'. To the right of the 'LINK Interface' is a box labeled 'TIMON (TSB12LV41)'. A 'Data BD Port' is connected to the 'DVCR Packetizer'. At the bottom, the 'PHY Interface' is connected to three separate lines labeled '1394 Port 1', '1394 Port 2', and '1394 Port 3'.</p> </div> <p>AV7110 Preview at 62; <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) C packets to and from the internal data RAM. This data can</p>

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	<p>then be processed by the user software as needed.”); <i>see also id.</i> at 63 (listing signals associated with the 1394 interface).</p> <p>“The application software interfaces with the peripheral interface controller via RTSL API calls. To send data to the host the application software will issue an API call to transfer the data from memory to the peripheral interface via a DMA. To receive data from the host, the application software will issue an API to transfer a predetermined number of bytes from the peripheral interface to internal data memory via the HSDI DMA unit. The user application software must have a way to determine the number of bytes of data that is expected from the host.” AV7110 Preview at 70.</p> <p>“Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM, and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.</p> <p>....</p> <p>After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards. The chip decodes MPEG-1 and MPEG-2 main profile at main level for video and Layer I and II MPEG-1 and MPEG-2 stereo for audio. Both video and audio decoders synchronize their presentation of reconstructed data using the transmitted presentation time stamps (PTS) and their local system clock. The local system clock is continuously updated by the ARM.” AV7110 Preview at 13.</p> <p>“The SDRAM must be 16-bits wide. The 'AV7110 provides control signals for up to two SDRAMs. Any combination of 4 or 16 Mbit SDRAMs may be used, provided they total at least 16 Mbits. The SDRAM must operate at an 81 MHz clock frequency and have the same timing parameters as the TI TMS626162, a 16 Mbit SDRAM. Other supported sizes and configurations are:</p> <p>16 Mbit → one 16 Mbit SDRAM  20 Mbit → one 16 Mbit and one 4 Mbit SDRAM  32 Mbit → two 16 Mbit SDRAM</p>

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	<p>The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 2D macroblock. The interface also supports decrement mode for bitBLT block transfers.</p> <p>....</p> <p>During DVB decoding, the 'AV7110 allocates the 16 Mbit SDRAM for PAL mode according to the default layout shown in Table 2. All the address pointers of the SDRAM partitioning are user programmable and hence the actual layout can be customized according to needs.” AV7110 Preview at 19.</p> <p>“memory usage reduction</p> <p>In the minimum memory configuration, the 'AV7110 is designed to work with two memory devices: a single 16 Mbit SDRAM device for system data storage (audio, video data, etc.) and a 4 Mbit DRAM for local data storage (private data, SI information, etc.). Table 11 shows what the two memories are used for, in bytes. The amount of memory available for OSD applications depends upon the mode of operation of the 'AV7110. For example, if the letterbox display format is used, more memory is required to store B frames and hence less OSD space will be available.” AV7110 Preview at 30.</p> <p>“Figure 27 shows the functionality of the interface signals when the 'AV7110 reads data from Timon. The maximum input rate of MPEG-2 data coming from Timon and routed through the transport stream hardware demultiplexer block (TPP) is approximately 64.8 Mbits/second. The maximum input bit rate over one transport packet is 60 Mbits/second.</p> <p>....</p> <p>When the 'AV7110 writes data to Timon (record mode), it drives BDIF, BDIEN, and BDIRW for one clock (system) period. BDIEN is driven low for only one byte and must be driven high between two byte transmissions. This is shown in Figure 28.” AV7110 Preview at 64; <i>see also id.</i> figs. 27-28.</p>
[1f] providing at least one Output Section, wherein said Output Section extracts said video and audio components from said storage device;	AV7110 Preview discloses or at least renders obvious “providing at least one Output Section, wherein said Output Section extracts said video and audio components from said storage device” based on at least the following exemplary disclosures:

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AV7110 Preview at 12 fig. 1.

“The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.” AV7110 Preview at 13.

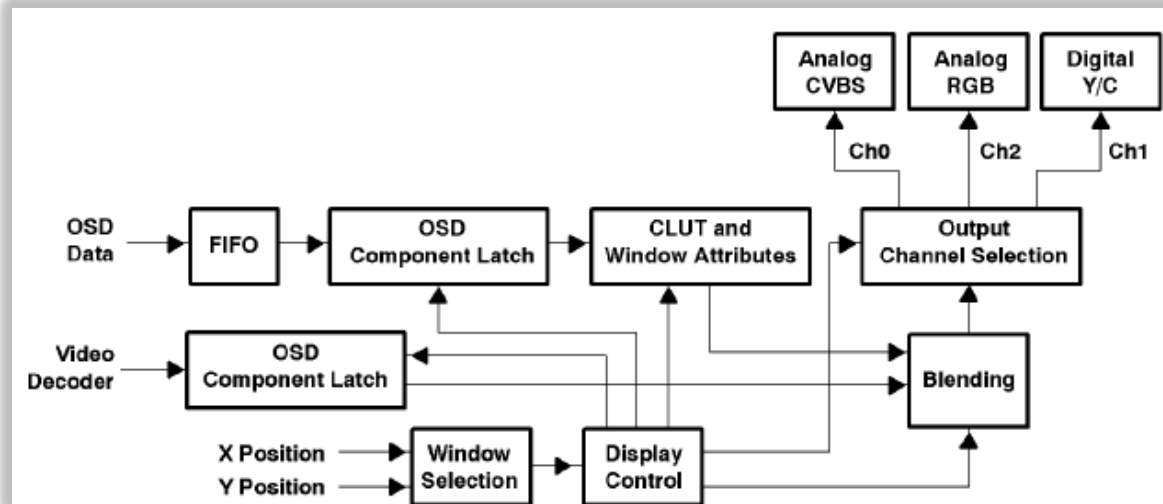
'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The TPP hardware is capable of detecting packets lost from the transport stream. With error concealment by the audio and the video decoders the ‘AV7110 minimizes the effect of lost data.” AV7110 Preview at 13.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PID table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.” AV7110 Preview at 21.</p> <p>“MPEG transport decoder (TPP) TPP module features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps Maximum input bit rate through the 1394 interface ..... 64.8 Mbps Maximum video bit rate ..... 15 Mbps</p>

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	<p>Maximum audio bit rate ..... 1.13 Mbps</p> <p>Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec</p> <p>Maximum number of PIDs that can be filtered ..... 32</p> <p>Maximum number of PIDs that can be descrambled ..... 32</p> <p>Maximum number of pairs of keys for the descrambler ..... 16</p> <p>Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SDRAM, and produces three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs. After being configured and activated by the ARM CPU, the OSD module reads OSD data and mixes it with the video output. The CPU is responsible for turning on and off OSD operations. The bitBLT hardware which is attached to the OSD module provides acceleration for memory block moves and graphics operations.” AV7110 Preview at 33.</p>

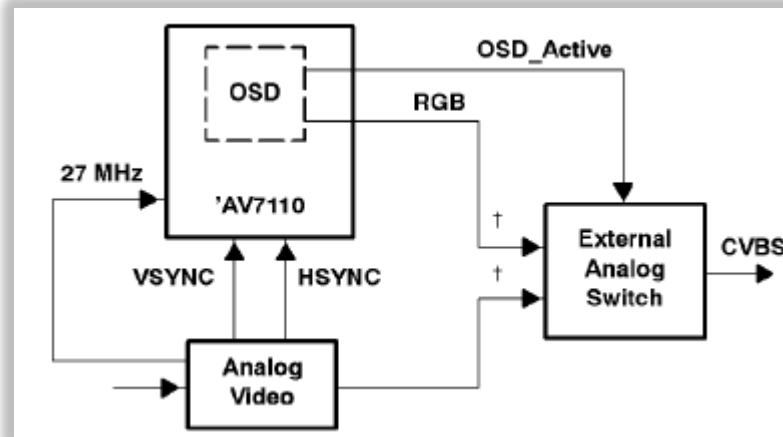


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AV7110 Preview at 33 fig. 8 (showing block diagram of the OSD module).



AV7110 Preview at 36 fig. 9.

“video output interfaces

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	<p>analog video output - NTSC/PAL encoder module</p> <ul style="list-style-type: none"> <li>• Supports NTSC and PAL B, D, G/H, and I display formats</li> <li>• Outputs Y/C or RGB, and composite video with 9-bit DACs</li> <li>• Generates 100/75 format color bar for PAL mode testing</li> <li>• Complies to the RS170A standard</li> <li>• Composite and RGB signals comply with ITU-R BT.470-3 and ITUR BT.471-1</li> <li>• Supports Macro Vision anti-taping function on composite video</li> <li>• Provides sync signals with option to accept external sync signals</li> </ul> <p>The composite video output can be either PAL or NTSC format. The default output format is PAL at powerup. Changing between NTSC and PAL mode can be done via an API which selects the output mode of the NTSC/PAL encoder. Note that the video decoder microcode ROM is specific to NTSC or PAL and required for proper operation.</p> <p>The sync signal pins Vsync and Hsync on the 'AV7110 are defaulted to 3-state mode at powerup, where internally generated sync signals will be used by the NTSC/PAL encoder. The user can then select the source of video sync signals via an API. If internal source is selected then the Vsync and Hsync pins will be configured as output pins.</p> <p>In addition to composite video, the 'AV7110 also provides either an analog S-video (Y - luminance , C - chrominance) signal or an analog RGB output with 720 pixel resolution. All outputs conform to the RS170A standard. Selection of RGB or S-video output is done via API software. Macro Vision version 7 is enabled via an API; the default state is off. A version of the 'AV7110 where the MacroVision anti-taping circuitry is permanently disabled is also available.” AV7110 Preview at 39.</p> <p>“digital video output (not supported when 32-bit EBI is used)</p> <p>PAL mode digital video output</p> <p>The digital output is in 4:2:2 component format. The content of the video could be either pure video or the blended combination of video and OSD. The pin assignments for the digital video output signals are:</p> <p style="padding-left: 40px;">YCOUT(8) 8-bit Cb/Y/Cr/Y data output</p> <p style="padding-left: 40px;">YCCLK(1) 27 MHz clock output</p> <p>The timing of 4:2:2 digital video output is shown in Figure 12.</p> <p>...</p> <p>NTSC mode digital video output</p> <p>The digital output includes video in either 4:4:4 or 4:2:2 component format, plus the aspect ratio VARIS code at the beginning of each video frame. The video output format is programmable by the user but defaults to 4:2:2.</p>

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	<p>The content of the video could be either pure video or the blended combination of video and OSD. The pin assignments for the digital video output signals are:</p> <p style="padding-left: 40px;">YCOOUT(8) 8-bit Cb/Y/Cr/Y and VARIS multiplexed data output</p> <p style="padding-left: 40px;">YCCLK(1) 27 MHz clock output</p> <p style="padding-left: 40px;">YCCTRL(2) 2-bit control signals to distinguish between Y/Cb/Cr components and VARIS code</p> <p>The interpretation of YCCTRL is defined in Table 20. . . .” AV7110 Preview at 41.</p> <p>“PCM audio output</p> <p>The PCM audio output from the 'AV7110 is a serial PCM data line, with associated bit clock (ASCLK) and left/right clock (LRCLK). PCM data is output serially on PCM OUT using the serial clock ASCLK as shown in Figure 15. The data output of PCM OUT alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7110 Preview at 46; <i>see generally id.</i> at 46-47 (describing additional aspects of PCM audio output).</p> <p>“elementary stream playback</p> <p>In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.</p> <p>SPDIF audio output</p> <p>The SPDIF output conforms to the consumer format of the AES3 standard for serial transmission of digital audio data. When using an external PLL (PCMSRC=1), SPDIF is supported only if Bx over-sampled PCMCLK is supplied (that is, PCMSEL[0]=1).” AV7110 Preview at 48.</p> <p><i>See generally</i> AV7110 Preview at 32-38 (describing OSD and graphics acceleration); <i>id.</i> at 41-43 (describing different aspects of digital video output).</p> <p>“After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards. The chip decodes MPEG-1 and MPEG-2 main profile at main level for video</p>

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	<p>and Layer I and II MPEG-1 and MPEG-2 stereo for audio. Both video and audio decoders synchronize their presentation of reconstructed data using the transmitted presentation time stamps (PTS) and their local system clock. The local system clock is continuously updated by the ARM.” AV7110 Preview at 13.</p> <p>“video decoder features</p> <ul style="list-style-type: none"> <li>• Real-time decoding of MPEG-2 Main Profile@Main level and MPEG-1 video bit-streams</li> <li>• Error detection and concealment</li> <li>• Internal 90 kHz/27 MHz system time clock</li> <li>• Sustained input rate of 15 Mbps</li> <li>• Supports trick mode with full size trick mode picture</li> <li>• Provides 1/4 and 1/16 decimated size picture</li> <li>• Extracts closed caption and other picture user data from the bit-stream</li> <li>• 3:2 pulldown in NTSC mode</li> <li>• Provides read access to video input buffer's read/write pointers</li> <li>• Pan-and-scan for 16:9 and 20:9 source material according to MPEG syntax</li> <li>• Letterbox support</li> <li>• High level command interface</li> <li>• Synchronization using presentation time stamps (PTS); also supports VBV delay based and free run (no synchronization) video playback</li> <li>• Supports the following display format with polyphase horizontal resampling and vertical chrominance filtering.” AV7110 at 25.</li> </ul> <p>“The video decoder module receives a video bit-stream from the SDRAM. It also uses the SDRAM as its working memory to store tables, buffers, and reconstructed images. The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.</p> <p>The 'AV7110 synchronizes the presentation of video with the audio using the transmitted PTS which are extracted by the ARM from the PES packets. it compares the PTS with the local system time clock (STC) and performs synchronization recovery if the difference is outside of a user programmable threshold range given as follows:</p> $STC - \text{threshold} < PTS < STC + \text{threshold}$

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	<p>If synchronization recovery is needed, the video decoder will either redisplay or skip a frame, depending on the PTS value. If the PTS lags, that is, the time for displaying the current picture has already passed, the video decoder discards the following B pictures without decoding them until the PTS catches up with the STC. If the PTS leads, that is, the time for displaying the current picture has not arrived yet, the video decoder pauses the decoding and continuously displays the last picture (see Synchronization for more details).” AV7110 Product Preview at 25-26.</p> <p>“trick mode</p> <p>When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error</li> <li>• Continuously displays the decoded I frame.” AV7110 Preview at 26; <i>see id.</i> tbl. 6 (showing video decoder commands enabling trick mode functionality).</li> </ul> <p>“The video decoder contains a polyphase filter and a vertical interpolation filter for performing horizontal resampling and luma/chroma vertical interpolation to support decimation and scaling of pictures. In operation, the firmware first loads picture data from the video storage space in the SDRAM to the internal buffer of the video decoder.” AV7110 Preview at 27; <i>see id.</i> (describing additional aspects).</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers I and II</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Outputs in both PCM and SPDIF formats</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information</li> <li>• Supports half-frequency modes</li> </ul>

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	<ul style="list-style-type: none"> <li>• Supports playback of 16-bit PCM data (PCM bypass), audio elementary stream, and audio PES</li> <li>• Provides read/write accesses to audio input buffers read/write pointers</li> </ul> <p>The audio module receives MPEG compressed audio data from the TC, decodes it, and outputs audio samples in PCM format. APIs are provided for the ARM CPU to initialize/control the audio decoder via a control register and to read status information from the decoder's status register.</p> <p>Audio frame data and PTS information are stored in the SDRAM in packet form. The audio module decodes the packets to extract the PTS and audio data. The audio decoder uses this PTS value to perform playback synchronization (see Synchronization for more details). It is application software's responsibility to determine and enable the PID of the MPEG-1 compliant bit-stream in a MPEG-2 audio program which contains both the MPEG-1 compliant bit-stream and the MPEG-2 extension bit-stream.</p> <p>The ARM can control the operation of the audio module via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and over-sampling ratio, and choose the output format for dual channel mode. The ARM will also be able to read status information from the audio module. One 32-bit register provides the MPEG header information and sync, CRC, and PCM status.” AV7110 Preview at 44; <i>see also id.</i> at 45-46 (listing registers used by the audio module).</p> <p>“The 'AV7110 uses the STC and PTS to determine the play back time of the decoded audio and video data. The relationship between STC and PTS is determined at the time of the generation of the generation of the respective elementary streams (ES). Upon reception, the demultiplexing software in the 'AV7110 extracts the video PTS and inserts it in an array of PTS and byte-count information maintained for the video decoder. For the audio the PTS information is extracted by the audio decoder front end from the PES. The video decoder contains an STC counter that is clocked by the system clock (27 MHz) and normalized to a 90 kHz reference. The audio decoder does not contain a counter. Instead, it gets updated from the system time reference counter every 1 .4 ms.” AV7110 Preview at 48.</p> <p>“extension bus interface (EBI)</p> <p>The extension bus interface is a 32-bit or 16-bit bidirectional data bus with a 25-bit address. It also provides 3 external interrupts and a wait line. All the external memories or I/O devices are mapped to the 32-bit address space of the ARM. There are six internally generated chips selects (CSx) for devices such as EEPROM memory, modem, front panel, front panel, front end control, parallel output port, and 1394 link device. Each CS has its own defined memory space and a programmable wait register which has a default of maximum allowable values as defined in Table 27. The number of wait states depends on the content of the register, with a minimum of one</p>

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wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. These are all programmable by user application software using APIs.” AV7110 Preview at 50.

“CS1 is intended for ARM application code, but writes will not be prevented. CS2, CS3, CS4, and CS5 all have the same characteristics. The ARM performs reads and writes to these devices through the extension bus. CS6 is read and write accessible by the ARM. It is also accessed by the TC for TPP DMAs, and it is write only. User C application software selects the PID of the packets to be sent through this port, the TPP will then send the data Q via DMAs. The parallel port is one byte wide and it is accessed via the least significant byte.” AV7110 Preview at 51.

**Table 27. An Example of Extension Bus Chip Select Assignment**

CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE
CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)
N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)
N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)
CS2	3000 0000 – 31FF FFFF	1 – 7	Modem
CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel
CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port

AV7110 Preview at 51 tbl. 27.

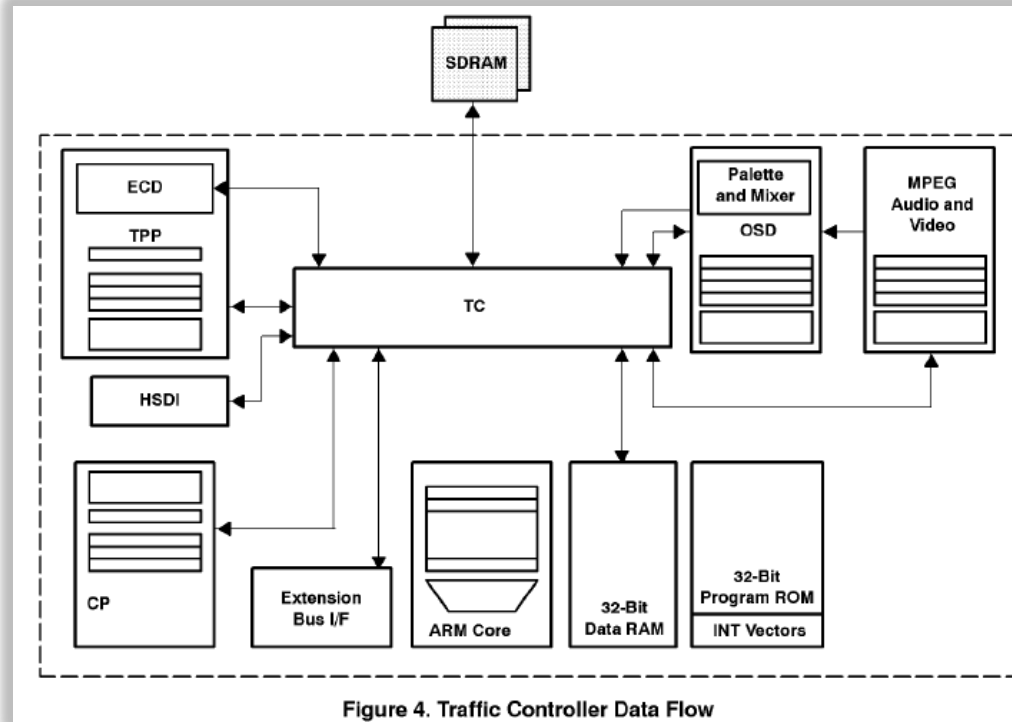
“The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it has to become active before the programmable wait cycle expires. If the combined total wait states exceeds its maximum, the decoder is not guaranteed to function properly. The EXTWAIT signal is synchronized internally with the on-chip 81 MHz clock. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT signal should be at least 24.7 ns. Since the EXTWAIT signal has the potential to stall the whole decoding process, the ARM will cap its wait to 500 ns. Afterwards, the ARM assumes the device that generated the EXTWAIT has failed and will ignore EXTWAIT from then on. Only a software or hardware reset can activate

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	<p>the EXTWAIT signal again. The timing diagram shown in Figure 19 is an example of a read using the EXTWAIT signal.” AV7110 Preview at 53.</p> <p>“The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 32-bit or 16-bit data and 25-bit address. It also supports DMA transfers to/from the extension bus. DMA transfers within the extension bus are not supported directly. They may be accomplished from user application software by using one DMA to the internal data RAM, followed by a second DMA to transfer back to the EBI. Extension bus single read and write cycle timings are shown in Figure 17 and Figure 18 respectively.” AV7110 Preview at 51; <i>see also id.</i> at 52 figs. 17 and 18.</p> <p>“traffic controller (TC) features</p> <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>• Authorizes and manages DMA transfers</li> <li>• Provides SDRAM interface</li> <li>• Manages extension bus</li> <li>• Provides memory access protection</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> <li>- Audio/video decoder to/from SDRAM</li> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> </ul> </li> <li>• Generates chip selects (CS) for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus</li> <li>• Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.</li> </ul>



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AV7110 Preview at 18 fig. 4.

See AV7110 Preview at 7 (stating that the TMS320AV7110 includes “an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory.”).

“The ARM can control the operation of the audio module via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and over-sampling ratio, and choose the output format for dual channel mode. The ARM will also be able to read status information from the audio module. One 32-bit register provides the MPEG header information and sync, CRC, and PCM status.” AV7110 Preview at 44.

See [1e].

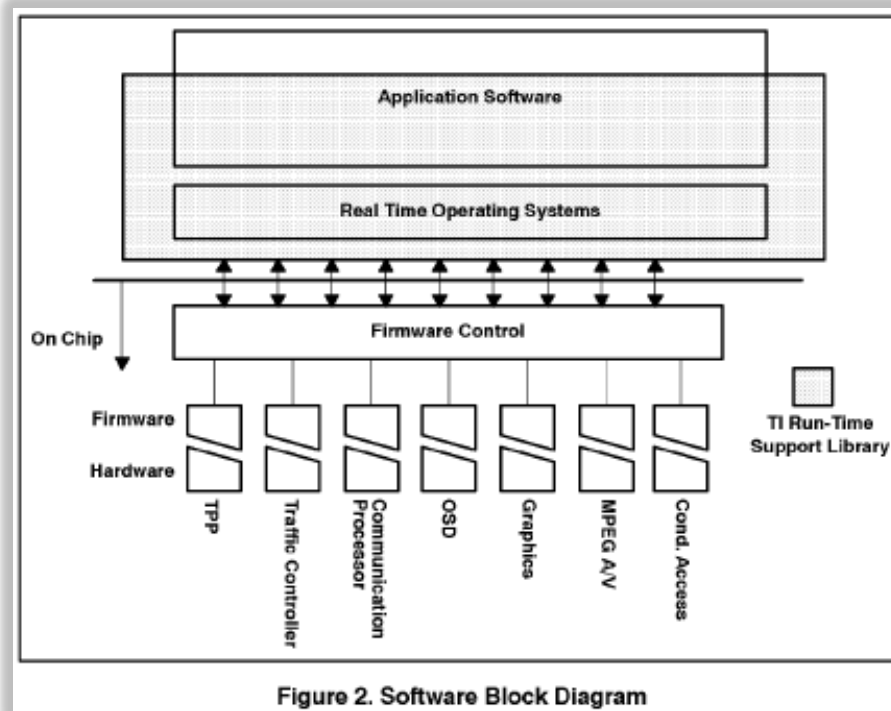
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[1g] wherein said Output Section assembles said video and audio components into an MPEG stream;	AV7110 Preview discloses or at least renders obvious “wherein said Output Section assembles said video and audio components into an MPEG stream” based on at least the following exemplary disclosures:  <i>See [1e], [1d], and [1f].</i>
[1h] wherein said Output Section sends said MPEG stream to a decoder;	AV7110 Preview discloses or at least renders obvious said “wherein said Output Section sends said MPEG stream to a decoder” based on at least the following exemplary disclosures:  <i>See [1f] and [1g].</i>
[1i] wherein said decoder converts said MPEG stream into TV output signals;	AV7110 Preview discloses or at least renders obvious “wherein said decoder converts said MPEG stream into TV output signals” based on at least the following exemplary disclosures:  <i>See [1f].</i>
[1j] wherein said decoder delivers said TV output signals to a TV receiver; and	AV7110 Preview discloses or at least renders “wherein said decoder delivers said TV output signals to a TV receiver” based on at least the following exemplary disclosures:  <i>See [1f].</i>
[1k] accepting control commands from a user, wherein said control commands are sent through the system and affect the flow of said MPEG stream.	AV7110 Preview discloses or at least renders obvious “accepting control commands from a user, wherein said control commands are sent through the system and affect the flow of said MPEG stream” based on at least the following exemplary disclosures:  “Command communication from the 'AV7110 to the ESC is done using the 4-bit EDMA A bus which is mapped into the ARM addressing space of the 'AV7110 when the EDMA port is selected. This will allow user software to write directly to the registers of the ESC. For details of these registers, refer to the appropriate external controller documentation. The 'AV7110 does not processing of this data and thus places no restriction on its function. An access to this memory space while the EDMA is selected will automatically generate a read or write cycle on the HSDI using the EDMA_RO and EDMA_WR signals and the EDMA_CS signal. Timing for these access is shown in Figure 31.” AV7110 Preview at 67.

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	<p>“communication processor features</p> <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> <li>• Provides 3 general purpose UARTs - two at up to 115.2 Kbps and one at up to 9.6 Kbps</li> <li>• Accepts IR input signals</li> <li>• Generates IR output signals</li> <li>• Provides up to nine general purpose I/Os</li> <li>• Manages 12C and JTAG interfaces</li> </ul> <p>This module contains a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR, and 12C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM CPU. Interrupts are used to communicate between these interface modules and the ARM CPU.”</p> <p>AV7110 Preview at 72; <i>see generally id.</i> at 72-78 (describing different functions and functional blocks of the communication processor).</p> <p>“IR input port</p> <p>Hardware is provided to capture and deliver IR data bits to user software for command decoding. Sample IR command decoding driver software for several commonly used IR formats are provided with the 'AV7110. API software is provided to configure the hardware to recognize IR format with different parameter settings:</p> <ul style="list-style-type: none"> <li>• data frame length (up to 32 bits)</li> <li>• maximum time between frame (a 13-bit count equals one period of CLK40)</li> <li>• LSB/MSB first</li> <li>• repeat pattern present</li> <li>• stop pattern present</li> <li>• compare enable (ignore repeated frames if this bit is set)</li> </ul> <p>At start up, user application software sets up the parameters above and defines the encoding pattern of the preamble, stop, repeat, data zero, and data one by storing the duration of the high and low levels of each pattern in the IR-input-RAM. The IR hardware will then look for IR input (assumed demodulated) which matches the pattern” AV7110 Preview at 75.</p> <p>“Software on the 'AV7110 is divided into three sections: firmware, API, and user software. Firmware is masked into the internal ROM of the 'AV7110. This software is supplied by Texas Instruments (TI™) and is used for low level control of the hardware and bit-stream demultiplexing in the 'AV7110. The user software is resident in external memory and contains all the software written by the user. The user software communicates with the</p>

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	<p>firmware through application programming interfaces (AP Is). These AP Is are contained in external ROM. APIs are written by TI and provided in the form of run time support library (RTSL).</p> <p>The 'AV7110s firmware is comprised of a collection of interrupt (FIQ) service routines and supervisor mode run-time support programs. This software isolates the application software from any direct interaction with the hardware. Figure 2 shows the high level block diagram of the complete software system.” AV7110 Preview at 13.</p> <p>“At the lowest level, each hardware component has a firmware module associated with it. A module may consist of:</p> <p style="padding-left: 40px;">Initialization code - executed at processor reset</p> <p style="padding-left: 40px;">Interrupt Service Routines - executed from interrupt by the associated hardware module.</p> <p>The run-time support library provides an application programming interface for user software. All run-time modules are written to be invoked from supervisory mode. This prevents software running in user mode from interfering with the built-in firmware.</p> <p>Functionally, the firmware consists of several software processes that are self contained at runtime and operate for the most part, independently and asynchronously. Because of the nature of the processing of a complex input stream, the processes are interrupt driven.</p> <p>The interrupt priorities determine the processing sequence, and the demultiplexed input stream packet information determines the data path through the system. There is only minimal inter-process dependency, which eliminates the need for a software control-flow process. Any inter-process dependencies can be handled by proper structuring of the interrupt process in terms of priorities and multi-level processing.” AV7110 Preview at 13-14.</p>

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AV7110 Preview at 14 fig. 2.

“The ARM CPU is responsible for managing all the hardware and software resources in the 'AV7110. At powerup the ARM verifies the existence and size of external memory. Following that, it initializes all the hardware modules by setting up control registers and tables and then resetting data pointers. It then executes the default firmware from internal ROM and transfers control to the users applications software. A set of run-time library routines provide the access to the firmware and hardware for user application programs. The application programs are stored in external memory attached to the extension bus. During normal operation the ARM constantly responds, based on a programmable priority, to FIQ interrupt requests from any of the hardware modules and devices on the extension bus. The types of interrupt services include transport packet parsing, program clock recovery, traffic controller and OSD service requests, service or

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	<p>data transfer requests from the extension bus and communication processor, and service requests from the audio/video decoder.” AV7110 Preview at 16.</p> <p><i>See</i> [1pre], [1e], [1d], and [1f].</p>
2. The process of claim 1, wherein said Input Section directs said MPEG stream to the destination indicated by said control commands.	<p>AV7110 Preview discloses or at least renders obvious “said Input Section directs said MPEG stream to the destination indicated by said control commands” based on at least the following exemplary disclosures:</p> <p><i>See</i> claim 1 at [1a], [1pre], [1d], [1e], [1f].</p>
3. The process of claim 1, wherein said Output Section extracts said video and audio components from the storage device indicated by said control commands.	<p>AV7110 Preview discloses or at least renders obvious “said Output Section extracts said video and audio components from the storage device indicated by said control commands” based on at least the following exemplary disclosures:</p> <p><i>See</i> claim 1 at [1a], [1pre], [1d], [1e], and [1f].</p>
5. The process of claim 1, wherein the storing and extracting of said video and audio components from said storage device are performed simultaneously.	<p>AV7110 Preview discloses or at least renders obvious “storing and extracting of said video and audio components from said storage device are performed simultaneously” based on at least the following exemplary disclosures:</p> <p><i>See</i> claim 1 at [1e] and [1pre].</p>
6. The process of claim 1, wherein said Media Switch calculates and logically associates a time stamp to said video and audio components.	<p>AV7110 Preview discloses or at least renders obvious “said Media Switch calculates and logically associates a time stamp to said video and audio components” based on at least the following exemplary disclosures:</p> <p><i>See</i> claim [1d].</p>
7. The process of claim 1, wherein said Media Switch extracts time stamp values from a digital TV stream and logically	<p>AV7110 Preview discloses or at least renders obvious “said Media Switch extracts time stamp values from a digital TV stream and logically associates said time stamp values to said video and audio components” based on at least the following exemplary disclosures:</p>

'389 Patent Claim	Exemplary Prior Art Disclosure
associates said time stamp values to said video and audio components.	<i>See</i> claim [1d].
12. The process of claim 1, further comprising the step of: increasing the decoder system clock rate for fast playback or fast reverse playback.	AV7110 Preview discloses or at least renders obvious “increasing the decoder system clock rate for fast playback or fast reverse playback” based on at least the following exemplary disclosures:  <i>See</i> claim 1 at [1pre], [1e], and [1f].
13. The process of claim 1, further comprising the step of: decreasing the decoder system clock rate for slow playback or slow reverse playback.	AV7110 Preview discloses or at least renders obvious “decreasing the decoder system clock rate for slow playback or slow reverse playback” based on at least the following exemplary disclosures:  <i>See</i> claim 1 at [1pre], [1e], and [1f].
18. The process of claim 1, wherein said Media Switch has a data bus connecting it to a CPU and DRAM.	AV7110 Preview discloses or at least renders obvious “said Media Switch has a data bus connecting it to a CPU and DRAM” based on at least the following exemplary disclosures:  <i>See</i> claim [1d].
19. The process of claim 1, wherein said Media Switch shares an address bus with a CPU and DRAM.	AV7110 Preview discloses or at least renders obvious “said Media Switch shares an address bus with a CPU and DRAM” based on at least the following exemplary disclosures:  <i>See</i> claim [1d].
20. The process of claim 1, wherein said Media Switch operates asynchronously and autonomously with a CPU.	AV7110 Preview discloses or at least renders obvious “said Media Switch operates asynchronously and autonomously with a CPU” based on at least the following exemplary disclosures:  <i>See</i> claim [1d].
21. The process of claim 1, wherein said storage device is connected to said Media Switch.	AV7110 Preview discloses or at least renders obvious “said storage device is connected to said Media Switch” based on at least the following exemplary disclosures:

'389 Patent Claim	Exemplary Prior Art Disclosure
	<i>See</i> claim [1d] and [1e].
22. The process of claim 1, wherein said Media Switch allows the CPU to queue up Direct Memory Access (DMA) transfers.	AV7110 Preview discloses or at least renders obvious “said Media Switch allows the CPU to queue up Direct Memory Access (DMA) transfers” based on at least the following exemplary disclosures:  <i>See</i> claim [1d].
23. The process of claim 1, wherein said Media Switch is implemented in hardware.	AV7110 Preview discloses or at least renders obvious “said Media Switch is implemented in hardware” based on at least the following exemplary disclosures:  <i>See</i> claim [1d].
[31pre]. A process for the simultaneous storage and play back of multimedia data, comprising the steps of:	<p>To the extent that the preamble is limiting, AV7110 Preview discloses or at least renders obvious “a process for the simultaneous storage and play back of multimedia data” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO), and MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infra-red (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.” AV7110 Preview at 1.</li> <li>• “Fully Functional Decoder Using a Single 16 Mbit External SDRAM <ul style="list-style-type: none"> <li>• Accepts Transport bit-streams of Up to 72.8 Mbps Burst Rate (60 Mbps Average Over One Transport Packet)</li> <li>• On-Chip European Common Descrambler Hardware</li> <li>• Hardware CRC Accelerator for SI/PSI Information Processing</li> <li>• Video Decoder That Decodes MPEG-1 and MPEG-2 Main Profile at Main Level Bit-Streams</li> </ul> </li> </ul>



'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Audio Decoder That Decodes MPEG-1 Layer I and II and the Basic Stereo Channels from MPEG-2 Multi-Channel Bit-Streams</li> <li>• Audio Output in Both PCM and SPDIF Formats</li> <li>• OSD Processor that Enables Mixture of OSD and Video Data With Transparency</li> <li>• BitBLT hardware that Accelerates Memory Block Move</li> <li>• 32/16 Bit ARM/Thumb Processor that Removes the Need of Another CPU in the Set-Top Box</li> <li>• Firmware That Controls Device Operation and Provides Application Access to Hardware Resources</li> <li>• On-Chip SDRAM Controller for 16, 20, or 32 Mbit SDRAM</li> <li>• General Purpose 16-/32-Bit Extension Bus Interface (EBI)</li> <li>• Configurable High Speed Data Interface to Connect to Either an IEEE 1394 Link Device, an IEEE 1284 Interface, or an External DMA Device Like SCSI that Supports Up to 16 Mbps Data Rate</li> <li>• Two 4-Wire UART Data Ports Supporting Up to 115.2Kbps Rate, and One 2-Wire UART Data Port Supporting Up to 9.6Kbps Rate</li> <li>• ISO 7816-3/NDC Smart Card Interface</li> <li>• I2c Master/Slave Interface</li> <li>• Programmable IR Input Port</li> <li>• Programmable IR Output Port</li> <li>• Four Dedicated General Purpose I/O Pins and Five Multiplexed Pins Which Can Be Configured to Be General Purpose I/O Pins</li> <li>• 3.3-V Device With Selected 5-V-Tolerant Pins for Interfacing to Other 5-V Devices” AV7110 Preview at 1.</li> <li>• “The HSDI supports the following concurrent data transfers. . . . 1394/program to TPP; TPP/DMA to 1394.” AV7110 Preview at 61.</li> <li>• “While the TPP is receiving MPEG-2 data from the 1394 port, the 'AV7110 can also record part of the bit stream it is receiving to the 1394 port. Send the whole transport stream from the FEC to the 1394 port without any filtering or decryption and, at the same time, decode/decrypt/display a program from either the same transport stream or from another transport stream received through the 1394 port.” AV7110 Preview at 65.</li> <li>• “trick mode</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error</li> <li>• Continuously displays the decoded I frame.” AV7110 Preview at 26.</li> </ul>
<p>[31a] providing a physical data source, wherein said physical data source accepts broadcast data from an input device, parses video and audio data from said broadcast data, and temporarily stores said video and audio data;</p>	<p>AV7110 Preview discloses or at least renders obvious “providing a physical data source that accepts broadcast data from an input device, parses video and audio data from said broadcast data, and temporarily stores said video and audio data” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO) . . .” AV7110 Preview at 1.</li> <li>• “• Accepts Transport bit-streams of Up to 72.8 Mbps Burst Rate (60 Mbps Average Over One Transport Packet) <ul style="list-style-type: none"> <li>• On-Chip European Common Descrambler Hardware</li> <li>• Video Decoder That Decodes MPEG-1 and MPEG-2 Main Profile at Main Level Bit-Streams</li> <li>• Audio Decoder That Decodes MPEG-1 Layer I and II and the Basic Stereo Channels from MPEG-2 Multi-Channel Bit-Streams” AV7110 Preview at 1.</li> </ul> </li> <li>• “The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet).” AV7110 Preview at 13.</li> <li>• “The on-chip SRAM (also referred to as internal data RAM in this document) provides the space necessary for the 'AV7110 to properly decode transport bit-streams without losing any packets.” AV7110 Preview at 15.</li> <li>• “TPP module</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p><i>features</i></p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface.” AV7110 Preview at 22.</li> </ul> <ul style="list-style-type: none"> <li>• “The TPP in the 'AV7110 filters the header of each packet according to the PID and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PID at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.” AV7110 Preview at 22.</li> <li>• “The TPP module detects which transport packets are scrambled, at either the program elementary stream (PES) or the transport stream level, and routes the data through the ECD as necessary.” AV7110 Preview at 23.</li> <li>• “transport parser input interface The 'AV7110 accepts DVB transport packet data from a front end such as a forward error correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_ START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB conditional access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23.</li> <li>• “The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device.” AV7110 Preview at 60.</li> <li>• “The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 &lt;::&gt; interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A)</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>packets to and from the internal data RAM. This data can then be processed by the user software as needed.” AV7110 Preview at 62.</p> <ul style="list-style-type: none"><li>• See AV7110 Preview at Fig. 1 (e.g., “Transport Bitstream From Front End,” “TPP”):</li></ul> <div><p>Figure 1 shows a functional block diagram of the TMS320AV7110.</p><p>Figure 1. 'AV7110 Block Diagram</p></div>
<p>[31b] providing a source object, wherein said source object extracts video and audio data from said physical data source;</p>	<p>AV7110 Preview discloses or at least renders obvious “providing a source object that extracts video and audio data from said physical data source” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"><li>• “TPP module features</li><li>• Parses transport bit streams</li><li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li><li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li></ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps Maximum input bit rate through the 1394 interface ..... 64.8 Mbps</p>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>Maximum video bit rate . . . . . 15 Mbps</p> <p>Maximum audio bit rate . . . . . 1.13 Mbps</p> <p>Minimum time between two transport packets (providing input rate is less than average rate) . . . . . 0 Sec</p> <p>Maximum number of PIDs that can be filtered . . . . . 32</p> <p>Maximum number of PIDs that can be descrambled . . . . . 32</p> <p>Maximum number of pairs of keys for the descrambler . . . . . 16</p> <p>Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>• “The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.” AV7110 Preview at 13.</p> <p>• “The TPP in the 'AV7110 filters the header of each packet according to the PID and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PID at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. . . . The data transfer from TPP to the internal data RAM is done via DMA automatically. Transport packets containing only audio or video payloads are automatically transferred to the proper external SD RAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and</p>

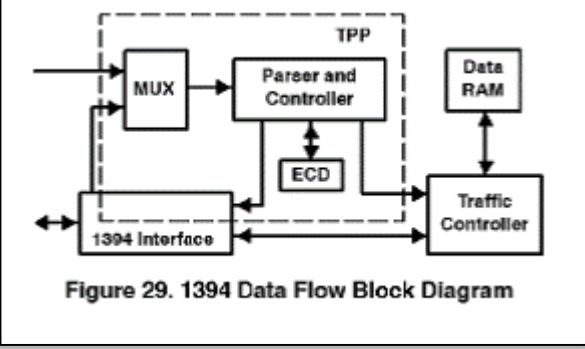
'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>establishes a DMA for transferring payload data from internal data RAM to the appropriate destination.” AV7110 Preview at 22.</p> <ul style="list-style-type: none"> <li>• “The TPP module detects which transport packets are scrambled, at either the program elementary stream (PES) or the transport stream level, and routes the data through the ECD as necessary. The ECD stores the descrambler keys locally and automatically selects the correct key of a specific PID.” AV7110 Preview at 23.</li> <li>• “Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination.” AV7110 Preview at 22.</li> <li>• AV7110 Preview at Fig. 1 (e.g., “TPP,” “Traffic Controller”)</li> <li>• AV7110 Preview at Fig. 4 (e.g., “TPP”)</li> </ul>
[31c] providing a transform object, wherein said transform object stores and retrieves data streams onto a storage device;	<p>AV7110 Preview discloses or at least renders obvious “providing a transform object that stores and retrieves data streams onto a storage device” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “traffic controller (TC) features <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>• Authorizes and manages DMA transfers</li> <li>• Provides SDRAM interface</li> <li>• Manages extension bus</li> <li>• Provides memory access protection</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> </ul> </li> </ul> </li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>- Audio/video decoder to/from SD RAM</li> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> <li>• Generates chip selects (CS) for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus</li> <li>• Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.</li> </ul> <ul style="list-style-type: none"> <li>• “The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM.” AV7110 Preview at 13.</li> <li>• “The ARM CPU is responsible for managing all the hardware and software resources in the 'AV7110. At powerup the ARM verifies the existence and size of external memory. Following that, it initializes all the hardware modules by setting up control registers and tables and then resetting data pointers. It then executes the default firmware from internal ROM and transfers control to the users applications software. A set of run-time library routines provide the access to the firmware and hardware for user application programs. The application programs are stored in external memory attached to the extension bus.” AV7110 Preview at 16.</li> <li>• “The types of interrupt services include transport packet parsing, program clock recovery, traffic controller and OSD service requests, service or data transfer requests from the extension bus and communication processor, and service requests from the audio/video decoder.” AV7110 Preview at 16.</li> <li>• “Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM, and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.” AV7110 Preview at 13.</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• “Configurable High Speed Data Interface to Connect to Either an IEEE 1394 Link Device, an IEEE 1284 Interface, or an External DMA Device Like SCSI that Supports Up to 16 Mbps Data Rate” AV7110 Preview at 1.</li> <li>• “Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM.” AV7110 Preview at 21.</li> <li>• “Recording mode through 1394 interface <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs.” AV7110 Preview at 22.</li> </ul> </li> <li>• “trick mode When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures.” AV7110 Preview at 26.</li> <li>• “The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device.” AV7110 Preview at 60.</li> <li>• “The functional block diagram of HSDI is given in Figure 25. The HSDI supports the following concurrent data transfers. <ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/program to 1394 (using dedicated I/F - see NOTE XXXX of Table 29)</li> <li>• TPP/program to decoder; 1394/DMA to/from memory</li> <li>• TPP/program to decoder; memory/DMA to/from HSDI</li> <li>• TPP/program to decoder; TPP/DMA to HSDI</li> <li>• TPP/program to decoder; TPP/program to 1394; memory/DMA to/from 1394</li> <li>• TPP/program to decoder; 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; TPP/DMA to 1394” AV7110 Preview at 61.</li> </ul> </li> </ul>



'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• “The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) packets to and from the internal data RAM. This data can then be processed by the user software as needed.” AV7110 Preview at 62.</li> <li>• “In recording mode, the 'AV7110 sends either encrypted or clean packets to the 1394 interface. The packet will be transferred as soon as it arrives. When recording encrypted data, the ECO module is bypassed.” AV7110 Preview at 65.</li> <li>• “Note that the major portion of the 1394 interface function is implemented in the HSDI module. Dedicated data lines are used for the 1394 interface that allows the 'AV7110 to work in different modes. <ul style="list-style-type: none"> <li>• Decode/decrypt/display one channel and record it</li> <li>• Decode/decrypt/display one channel and record it encrypted (pay-per-view)</li> <li>• Decode/display one channel while recording all or part of 32 PIDs from a transponder, with each selected PIDs either encrypted or decrypted. In addition non selected PIDs can also be recorded in their original format (decryption is not possible for non selected PIDs).</li> <li>• While the TPP is receiving MPEG-2 data from the 1394 port, the 'AV7110 can also record part of the bitstream it is receiving to the 1394 port</li> <li>• Send the whole transport stream from the FEC to the 1394 port without any filtering or decryption and, at the same time, decode/decrypt/display a program from either the same transport stream or from another transport stream received through the 1394 port.” AV7110 Preview at 65.</li> </ul> </li> <li>• AV7110 Preview at Fig. 1 (e.g., “Traffic Controller” and “HSDI”)</li> <li>• <i>See</i> AV7110 Preview at Fig. 29 (e.g., “Traffic Controller” and “1394 Interface”):</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	 <p>Figure 29. 1394 Data Flow Block Diagram</p> <ul style="list-style-type: none"> <li>• AV7110 Preview at Fig. 4 (e.g., “TC” and “HSDI”)</li> </ul>
<p>[31d] wherein said source object obtains a buffer from said transform object, said source object converts video data into data streams and fills said buffer with said streams;</p>	<p>AV7110 Preview discloses or at least renders obvious “wherein said source object obtains a buffer from said transform object, said source object converts video data into data streams and fills said buffer with said streams” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM.” AV7110 Preview at 13.</li> <li>• “traffic controller (TC) features             <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>• Authorizes and manages DMA transfers</li> <li>• Provides SDRAM interface</li> <li>• Manages extension bus</li> <li>• Provides memory access protection</li> <li>• Manages the data flow between processors and memories                 <ul style="list-style-type: none"> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> </ul> </li> </ul> </li> </ul>

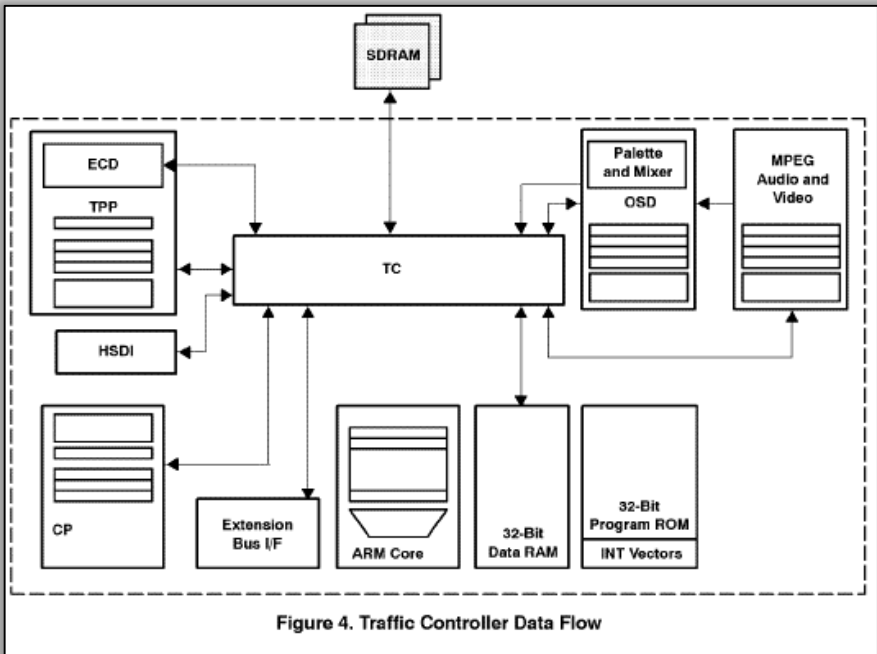
'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>- Audio/video decoder to/from SD RAM</li> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> <li>• Generates chip selects (CS) for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus</li> <li>• Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.</li> <li>• “The SDRAM is used to store system level tables, video and audio bit-streams, reconstructed video images, OSD data, video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware.” AV7110 Preview at 20.</li> <li>• “The TC continuously monitors the fullness of the video and audio input buffers. If overflow or underflow occurs, a maskable FIQ interrupt will be used to alert the firmware so that corrective action can be taken in a timely manner. Alternatively, user software can periodically inspect (read access) the read/write pointers of the circular video and audio input buffers and take preemptive actions if overflow/underflow is deemed imminent. Moreover, the TC also keeps the number of bytes of video data being sent to the video decoder in a wrap-around counter. This byte-count is used by the firmware for accurate video PTS synchronization.” AV7110 Preview at 20.</li> <li>• “Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers on the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PID table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.” AV7110 Preview at 21.</li> <li>• “Interrupt requests are generated from internal modules like the TPP, OSD, A/V decoder, communication processor, and devices on the extension bus. Some of the requests are for data transfers to internal RAM,</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>while others are true interrupts to the ARM CPU. The TC handles data transfers to internal RAM, while others are true interrupts to the ARM CPU. The TC handles data transfers, and the ARM provides services to true interrupts. The interrupts are grouped into FIQs and IRQs. The firmware will use FIQs, while the application software will use IRQs. The priorities for FIQs are managed by the firmware while those of IRQ are managed by the application software.” AV7110 Preview at 19.</p> <ul style="list-style-type: none"> <li>• “The TC manages two types of DMA transfers, but only one of them, the general purpose DMA (GPDMA), is accessible to the user. The user has no knowledge of the other type of DMAs which are initiated by the TPP, the video decoder, the audio decoder, and the OSD module. The GPDMA includes ARM-generated and bitBLT-generated DMAs.” AV7110 Preview at 20.</li> <li>• “The bitBLT hardware provides a faster way to move a block of memory from one space to the other. It reads data from a source location, performs shift/mask/merge/expand operations on the data, and finally write it to a destination location.” AV7110 Preview at 38.</li> <li>• AV7110 Preview at Fig. 4 (e.g., “TPP” and “TC”)</li> </ul>
[31e] wherein said source object is automatically flow controlled by said transform object;	<p>AV7110 Preview discloses or at least renders obvious “wherein said source object is automatically flow controlled by said transform object” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “Firmware That Controls Device Operation and Provides Application Access to Hardware Resources” AV7110 Preview at 1.</li> <li>• “traffic controller (TC) features <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>...</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> <li>- Audio/video decoder to/from SD RAM</li> </ul> </li> </ul> </li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>- SDRAM to/from internal data RAM</p> <p>- High speed data interface to/from internal data RAM</p> <p>...” AV7110 Preview at 17.</p> <ul style="list-style-type: none"> <li> <p>“resource management</p> <p>The ARM CPU is responsible for managing all the hardware and software resources in the 'AV7110. At powerup the ARM verifies the existence and size of external memory. Following that, it initializes all the hardware modules by setting up control registers and tables and then resetting data pointers. It then executes the default firmware from internal ROM and transfers control to the users applications software. A set of run-time library routines provide the access to the firmware and hardware for user application programs. The application programs are stored in external memory attached to the extension bus. During normal operation the ARM constantly responds, based on a programmable priority, to FIQ interrupt requests from any of the hardware modules and devices on the extension bus. The types of interrupt services include transport packet parsing, program clock recovery, traffic controller and OSD service requests, service or data transfer requests from the extension bus and communication processor, and service requests from the audio/video decoder.” AV7110 Preview at 16.</p> </li> <li> <p>“Interrupt requests are generated from internal modules like the TPP, OSD, A/V decoder, communication processor, and devices on the extension bus. Some of the requests are for data transfers to internal RAM, while others are true interrupts to the ARM CPU. The TC handles data transfers to internal RAM, while others are true interrupts to the ARM CPU. The TC handles data transfers, and the ARM provides services to true interrupts. The interrupts are grouped into FIQs and IRQs. The firmware will use FIQs, while the application software will use IRQs. The priorities for FIQs are managed by the firmware while those of IRQ are managed by the application software.” AV7110 Preview at 19.</p> </li> <li> <p>“managing DMA transfer</p> <p>The TC in the 'AV7110 provides DMA capability to facilitate large block transfers between memories and buffers. . . . The TC manages two types of DMA transfers, but only one of them, the general purpose DMA (GPDMA), is accessible to the user. The user has no knowledge of the other type of DMAs which are initiated by the TPP, the video decoder, the audio decoder, and the OSD module. The GPDMA includes ARM-generated and bitBLT-generated DMAs. The TC can accept up to 4 GPDMA at any given time. DMA from the data RAM to the extension bus (and vice versa) is byte aligned.” AV7110 Preview at 20.</p> </li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li> <p>“video/audio buffer monitoring support The TC continuously monitors the fullness of the video and audio input buffers. If overflow or underflow occurs, a maskable FIQ interrupt will be used to alert the firmware so that corrective action can be taken in a timely manner. Alternatively, user software can periodically inspect (read access) the read/write pointers of the circular video and audio input buffers and take preemptive actions if overflow/underflow is deemed imminent. Moreover, the TC also keeps the number of bytes of video data being sent to the video decoder in a wrap-around counter. This byte-count is used by the firmware for accurate video PTS synchronization.” AV7110 Preview at 20.</p> </li> <li> <p>“Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SD RAM without intervention from the ARM, and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SD RAM. The TC repacks the data and gets rid of the voids created by the header removal.” AV7110 Preview at 13.</p> </li> <li> <p>“Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PID table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.” AV7110 Preview at 21.</p> </li> <li> <p>“It is possible to split the video input buffer between DRAM and SDRAM to increase the amount of SDRAM space available for OSD display. When this mode is selected, the DRAM portion is only used as an overflow buffer. When the allocated buffer space in the SD RAM is full, the incoming data is written directly to the DRAM. As soon as memory space is available in the SDRAM, the data is transferred from the DRAM to the SDRAM via DMA automatically. Once the overflow buffer in the DRAM has been</p> </li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>emptied, incoming data is written directly to the SDRAM again. The video decoder always takes data from the SDRAM. The size of the buffers in each area of memory is under API control. At least 107 KBytes of the video input buffer must be located in the SDRAM for the video decoder to operate properly. . . . A dedicated DMA channel is used for the automatic transfer of data from the DRAM to SD RAM to implement this split buffer scheme.” AV7110 Preview at 31.</p> <ul style="list-style-type: none"> <li>• “trick mode When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur. During trick mode decoding, the video decoder repeats the following steps: <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error</li> <li>• Continuously displays the decoded I frame.” AV7110 Preview at 26.</li> </ul> </li> <li>• “The video decoder module receives a video bit-stream from the SDRAM. It also uses the SDRAM as its working memory to store tables, buffers, and reconstructed images. The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.” AV7110 Preview at 25.</li> <li>• “APIs are provided for the ARM CPU to initialize/control the audio decoder via a control register and to read status information from the decoder's status register. . . . The ARM can control the operation of the audio module via a 32-bit control register.” AV7110 Preview at 44.</li> <li>• “In the minimum memory configuration, the 'AV7110 is designed to work with two memory devices: a single 16 Mbit SD RAM device for system data storage (audio, video data, etc.) and a 4 Mbit DRAM for local data storage (private data, SI information, etc.). Table 11 shows what the two memories are used for, in bytes. The amount of memory available for OSD applications depends upon the mode of operation of the 'AV7110. For example, if the letterbox display format is used, more memory is required to store B frames and hence less OSD space will be available. Table 12 shows the size of B frame buffer for different display formats at normal (full) resolution.” AV7110 Preview at 30.</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• See AV7110 Preview at Fig. 4:</li> </ul>  <p style="text-align: center;">Figure 4. Traffic Controller Data Flow</p> <ul style="list-style-type: none"> <li>• See Table 2 (“Default Memory Allocation of 16 Mbit SDRAM (PAL)”)</li> </ul>
[31f] providing a sink object, wherein said sink object obtains data stream buffers from said transform object and outputs said streams to a video and audio decoder;	<p>AV7110 Preview discloses or at least renders obvious “providing a sink object that obtains data stream buffers from said transform object and outputs said streams to a video and audio decoder” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “On-Chip SDRAM Controller for 16, 20, or 32 Mbit SDRAM” AV7110 Preview at 1.</li> <li>• “. . . both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SD RAM and process them according to the ISO standards. The chip decodes</li> </ul>



'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>MPEG-1 and MPEG-2 main profile at main level for video and Layer I and II MPEG-1 and MPEG-2 stereo for audio.” AV7110 Preview at 13.</p> <ul style="list-style-type: none"> <li>• “traffic controller (TC) features <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>...</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> <li>- Audio/video decoder to/from SD RAM</li> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> </ul> </li> </ul> </li> </ul> <p>...” AV7110 Preview at 17.</p> <ul style="list-style-type: none"> <li>• “The TC in the 'AV7110 provides DMA capability to facilitate large block transfers between memories and buffers. . . . The SDRAM is used to store system level tables, video and audio bit-streams, reconstructed video images, OSD data, video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware.” AV7110 Preview at 20.</li> <li>• “The video decoder module receives a video bit-stream from the SDRAM. It also uses the SDRAM as its working memory to store tables, buffers, and reconstructed images. The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.” AV7110 Preview at 25.</li> <li>• “In operation, the firmware first loads picture data from the video storage space in the SD RAM to the internal buffer of the video decoder. Vertical and horizontal filters are then applied to the video data to produce the 4:2:2 image.” AV7110 Preview at 27.</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• “In the minimum memory configuration, the 'AV7110 is designed to work with two memory devices: a single 16 Mbit SD RAM device for system data storage (audio, video data, etc.) and a 4 Mbit DRAM for local data storage (private data, SI information, etc.).” AV7110 Preview at 30.</li> <li>• “It is possible to split the video input buffer between DRAM and SDRAM to increase the amount of SDRAM space available for OSD display. When this mode is selected, the DRAM portion is only used as an overflow buffer. When the allocated buffer space in the SD RAM is full, the incoming data is written directly to the DRAM. As soon as memory space is available in the SDRAM, the data is transferred from the DRAM to the SDRAM via DMA automatically. Once the overflow buffer in the DRAM has been emptied, incoming data is written directly to the SDRAM again. The video decoder always takes data from the SDRAM. The size of the buffers in each area of memory is under API control. At least 107 KBytes of the video input buffer must be located in the SDRAM for the video decoder to operate properly. . . . A dedicated DMA channel is used for the automatic transfer of data from the DRAM to SD RAM to implement this split buffer scheme.” AV7110 Preview at 31.</li> <li>• “The audio module receives MPEG compressed audio data from the TC, decodes it, and outputs audio samples in PCM format. APIs are provided for the ARM CPU to initialize/control the audio decoder via a control register and to read status information from the decoder's status register.” AV7110 Preview at 44.</li> <li>• “In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.” AV7110 Preview at 48.</li> </ul>
[31g] wherein said decoder converts said streams into display signals and sends said signals to a display;	<p>AV7110 Preview discloses or at least renders obvious “wherein said decoder converts said streams into display signals and sends said signals to a display” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “• Video Decoder That Decodes MPEG-1 and MPEG-2 Main Profile at Main Level Bit-Streams • Audio Decoder That Decodes MPEG-1 Layer I and II and the Basic Stereo Channels from MPEG-2 Multi-Channel Bit-Streams” AV7110 Preview at 1.</li> <li>• “video decoder</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>features</p> <ul style="list-style-type: none"> <li>• Real-time decoding of MPEG-2 Main Profile@Main level and MPEG-1 video bit-streams</li> <li>• Error detection and concealment</li> <li>• Internal 90 kHz/27 MHz system time clock</li> <li>• Sustained input rate of 15 Mbps</li> <li>• Supports trick mode with full size trick mode picture</li> <li>• Provides 1/4 and 1/16 decimated size picture</li> <li>• Extracts closed caption and other picture user data from the bit-stream</li> <li>• 3:2 pulldown in NTSC mode</li> <li>• Provides read access to video input buffer's read/write pointers</li> <li>• Pan-and-scan for 16:9 and 20:9 source material according to MPEG syntax</li> <li>• Letterbox support</li> <li>• High level command interface</li> <li>• Synchronization using presentation time stamps (PTS); also supports VBV delay based and free run (no synchronization) video playback</li> <li>• Supports the following display format with polyphase horizontal resampling and vertical chrominance filtering” AV7110 Preview at 25.</li> </ul> <ul style="list-style-type: none"> <li>• “The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SD RAM, and produces</li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<p>three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs.” AV7110 Preview at 33.</p> <ul style="list-style-type: none"> <li>• “audio decoder features <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers I and II</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Outputs in both PCM and SPDIF formats</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information</li> <li>• Supports half-frequency modes</li> <li>• Supports playback of 16-bit PCM data (PCM bypass), audio elementary stream, and audio PES</li> <li>• Provides read/write accesses to audio input buffers read/write pointers” AV7110 Preview at 44.</li> </ul> </li> <li>• “The audio module receives MPEG compressed audio data from the TC, decodes it, and outputs audio samples in PCM format. APIs are provided for the ARM CPU to initialize/control the audio decoder via a control register and to read status information from the decoder's status register.” AV7110 Preview at 44.</li> </ul>

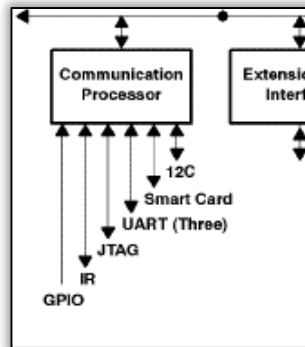
'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• “high level commands The video decoder accepts the high level commands detailed in Table 6. Video Decoder Commands” AV7110 Preview at 26.</li> <li>• AV7110 Preview at Fig. 1 (e.g., “Video Decoder” and “Audio Decoder”)</li> </ul>
[31h] wherein said sink object is automatically flow controlled by said transform object;	<p>AV7110 Preview discloses or at least renders obvious “wherein said sink object is automatically flow controlled by said transform object” based on at least the following exemplary disclosures:</p> <p><i>See [31e].</i></p>
[31i] providing a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system; and	<p>AV7110 Preview discloses or at least renders obvious “providing a control object that receives commands from a user, said commands control the flow of the broadcast data through the system” based on at least the following exemplary disclosures:</p> <ul style="list-style-type: none"> <li>• “• Programmable IR Input Port • Programmable IR Output Port” AV7110 Preview at 1.</li> <li>• “IR input port Hardware is provided to capture and deliver IR data bits to user software for command decoding. Sample IR command decoding driver software for several commonly used IR formats are provided with the 'AV7110.” AV7110 Preview at 75.</li> <li>• “communication processor features <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> <li>• Provides 3 general purpose UARTs - two at up to 115.2 Kbps and one at up to 9.6 Kbps</li> <li>• Accepts IR input signals</li> <li>• Generates IR output signals</li> </ul> </li> </ul>

'389 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Provides up to nine general purpose I/Os</li> <li>• Manages I2C and JTAG interfaces</li> </ul> <p>This module contains a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR, and I2C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM CPU. Interrupts are used to communicate between these interface modules and the ARM CPU.” AV7110 Preview at 72.</p> <ul style="list-style-type: none"> <li>• “trick mode When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur. During trick mode decoding, the video decoder repeats the following steps: <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error</li> <li>• Continuously displays the decoded I frame.” AV7110 Preview at 26.</li> </ul> </li> <li>• “high level commands The video decoder accepts the high level commands detailed in Table 6. Video Decoder Commands” AV7110 Preview at 26.</li> <li>• “The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.” AV7110 Preview at 25.</li> <li>• “APIs are provided for the ARM CPU to initialize/control the audio decoder via a control register and to read status information from the decoder's status register. . . . The ARM can control the operation of the audio module via a 32-bit control register.” AV7110 Preview at 44.</li> <li>• <i>See</i> AV7110 Preview at Table 6 (e.g., “FastForward” and “Freeze”):</li> </ul>

**'389 Patent Claim****Exemplary Prior Art Disclosure****Table 6. Video Decoder Commands**

NAME	DESCRIPTION
Play	Normal decoding
Freeze	Normal decoding but continue to display the last picture.
Stop	Stops the decoding process. The display continue with the last picture.
Scan	Searches for the first I picture, decodes it, continuously displays it, and flushes the buffer.
FastForward	Decode and display only the I and P pictures. Applicable only when user has control of the input bit-stream.
SingleStep	Decode and display the next picture, then stop. Applicable only when user has control of the input bit-stream.
SlowMotion (N)	Decode pictures and display each picture N-frame times. Applicable only when user has control of the input bit-stream.
NewChannel	For channel change, the video decoder first finishes the current display picture. Then, based on settings provided through an API in user software, selects what to display: a pre-setup OSD window or blank background. This command should be preceded by a stop command.
Reset	Halts execution of the current command. The bit-stream buffer is flushed and the video decoder performs an internal reset
Decimate 1/2	Continue normal decoding and displaying of a $1/2 \times 1/2$ decimated picture (used by OSD API).
Decimate 1/4	Continue normal decoding and displaying of a $1/4 \times 1/4$ decimated picture (used by OSD API).
Half-res on	Turn on half-resolution B frame storage (see Half Resolution B Picture Storage)
Half-res off	Turn off half-resolution B frame storage (see Half Resolution B Picture Storage)

- See AV7110 Preview at Fig. 1 (e.g., “Communication Processor”):



[31j] wherein said control object sends flow command events to said source, transform, and sink objects.

AV7110 Preview discloses or at least renders obvious “wherein said control object sends flow command events to said source, transform, and sink objects” based on at least the following exemplary disclosures:

See [31i].

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[32pre]. An apparatus for the simultaneous storage and play back of multimedia data, comprising:	To the extent that the preamble is limiting, AV7110 Preview discloses or at least renders obvious “an apparatus for the simultaneous storage and play back of multimedia data” based on at least the following exemplary disclosures:  <i>See claim [1pre].</i>
[32a] a module for accepting television (TV) broadcast signals, wherein said TV signals are based on a multitude of standards, including, but not limited to, National Television Standards Committee (NTSC) broadcast, PAL broadcast, satellite transmission, DSS, DBS, or ATSC;	AV7110 Preview discloses or at least renders obvious “a module for accepting television (TV) broadcast signals, wherein said TV signals are based on a multitude of standards, including, but not limited to, National Television Standards Committee (NTSC) broadcast, PAL broadcast, satellite transmission, DSS, DBS, or ATSC” based on at least the following exemplary disclosures:  <i>See claim [1a].</i>
[32b] a module for tuning said TV signals to a specific program;	AV7110 Preview discloses or at least renders obvious “a module for tuning said TV signals to a specific program” based on at least the following exemplary disclosures:  <i>See claim [1b].</i>
[32c] at least one Input Section, wherein said Input Section converts said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation;	AV7110 Preview discloses or at least renders obvious “at least one Input Section, wherein said Input Section converts said specific program to an Moving Pictures Experts Group (MPEG) formatted stream for internal transfer and manipulation” based on at least the following exemplary disclosures:  <i>See claim [1c].</i>
[32d] a Media Switch, wherein said Media Switch parses said MPEG stream, said MPEG stream is separated into its video and audio components;	AV7110 Preview discloses or at least renders obvious “a Media Switch, wherein said Media Switch parses said MPEG stream, said MPEG stream is separated into its video and audio components” based on at least the following exemplary disclosures:  <i>See claim [1d].</i>



'389 Patent Claim	Exemplary Prior Art Disclosure
[32e] a module for storing said video and audio components on a storage device;	AV7110 Preview discloses or at least renders obvious “a module for storing said video and audio components on a storage device” based on at least the following exemplary disclosures:  <i>See claim [1e].</i>
[32f] at least one Output Section, wherein said Output Section extracts said video and audio components from said storage device;	AV7110 Preview discloses or at least renders obvious “at least one Output Section, wherein said Output Section extracts said video and audio components from said storage device” based on at least the following exemplary disclosures:  <i>See claim [1f].</i>
[32g] wherein said Output Section assembles said video and audio components into an MPEG stream;	AV7110 Preview discloses or at least renders obvious “wherein said Output Section assembles said video and audio components into an MPEG stream” based on at least the following exemplary disclosures:  <i>See claim [1g].</i>
[32h] wherein said Output Section sends said MPEG stream to a decoder;	AV7110 Preview discloses or at least renders obvious “wherein said Output Section sends said MPEG stream to a decoder” based on at least the following exemplary disclosures:  <i>See claim [1h].</i>
[32i] wherein said decoder converts said MPEG stream into TV output signals;	AV7110 Preview discloses or at least renders obvious “wherein said decoder converts said MPEG stream into TV output signals” based on at least the following exemplary disclosures:  <i>See claim [1i].</i>
[32j] wherein said decoder delivers said TV output signals to a TV receiver; and	AV7110 Preview discloses or at least renders obvious “wherein said decoder delivers said TV output signals to a TV receiver” based on at least the following exemplary disclosures:  <i>See claim [1j].</i>
[32k] accepting control commands from a user, wherein said control commands are sent through the system and affect the flow of said MPEG stream.	AV7110 Preview discloses or at least renders obvious “accepting control commands from a user, wherein said control commands are sent through the system and affect the flow of said MPEG stream” based on at least the following exemplary disclosures:  <i>See claim [1k].</i>

'389 Patent Claim	Exemplary Prior Art Disclosure
33. The apparatus of claim 32, wherein said Input Section directs said MPEG stream to the destination indicated by said control commands.	AV7110 Preview discloses or at least renders obvious “said Input Section directs said MPEG stream to the destination indicated by said control commands” based on at least the following exemplary disclosures:  <i>See claim 2.</i>
34. The apparatus of claim 32, wherein said Output Section extracts said video and audio components from the storage device indicated by said control commands.	AV7110 Preview discloses or at least renders obvious “said Output Section extracts said video and audio components from the storage device indicated by said control commands” based on at least the following exemplary disclosures:  <i>See claim 3.</i>
36. The apparatus of claim 32, wherein the storing and extracting of said video and audio components from said storage device are performed simultaneously.	AV7110 Preview discloses or at least renders obvious “storing and extracting of said video and audio components from said storage device are performed simultaneously” based on at least the following exemplary disclosures:  <i>See claim 5.</i>
37. The apparatus of claim 32, wherein said Media Switch calculates and logically associates a time stamp to said video and audio components.	AV7110 Preview discloses or at least renders obvious “said Media Switch calculates and logically associates a time stamp to said video and audio components” based on at least the following exemplary disclosures:  <i>See claim 6.</i>
38. The apparatus of claim 32, wherein said Media Switch extracts time stamp values from a digital TV stream and logically associates said time stamp values to said video and audio components.	AV7110 Preview discloses or at least renders obvious “said Media Switch extracts time stamp values from a digital TV stream and logically associates said time stamp values to said video and audio components” based on at least the following exemplary disclosures:  <i>See claim 7.</i>
43. The apparatus of claim 32, further comprising:	AV7110 Preview discloses or at least renders obvious “a module for increasing the decoder system clock rate for fast playback or fast reverse playback” based on at least the following exemplary disclosures:

'389 Patent Claim	Exemplary Prior Art Disclosure
a module for increasing the decoder system clock rate for fast playback or fast reverse playback	<i>See</i> claim 12.
44. The apparatus of claim 32, further comprising: a module for decreasing the decoder system clock rate for slow playback or slow reverse playback.	AV7110 Preview discloses or at least renders obvious “a module for decreasing the decoder system clock rate for fast playback or fast reverse playback” based on at least the following exemplary disclosures:  <i>See</i> claim 13.
49. The apparatus of claim 32, wherein said Media Switch has a data bus connecting it to a CPU and DRAM.	AV7110 Preview discloses or at least renders obvious “said Media Switch has a data bus connecting it to a CPU and DRAM” based on at least the following exemplary disclosures:  <i>See</i> claim 18.
50. The apparatus of claim 32, wherein said Media Switch shares an address bus with a CPU and DRAM.	AV7110 Preview discloses or at least renders obvious “said Media Switch shares an address bus with a CPU and DRAM” based on at least the following exemplary disclosures:  <i>See</i> claim 19.
51. The apparatus of claim 32, wherein said Media Switch operates asynchronously and autonomously with a CPU.	AV7110 Preview discloses or at least renders obvious “said Media Switch operates asynchronously and autonomously with a CPU” based on at least the following exemplary disclosures:  <i>See</i> claim 20.
52. The apparatus of claim 32, wherein said storage device is connected to said Media Switch.	AV7110 Preview discloses or at least renders obvious “said storage device is connected to said Media Switch” based on at least the following exemplary disclosures:  <i>See</i> claim 21.

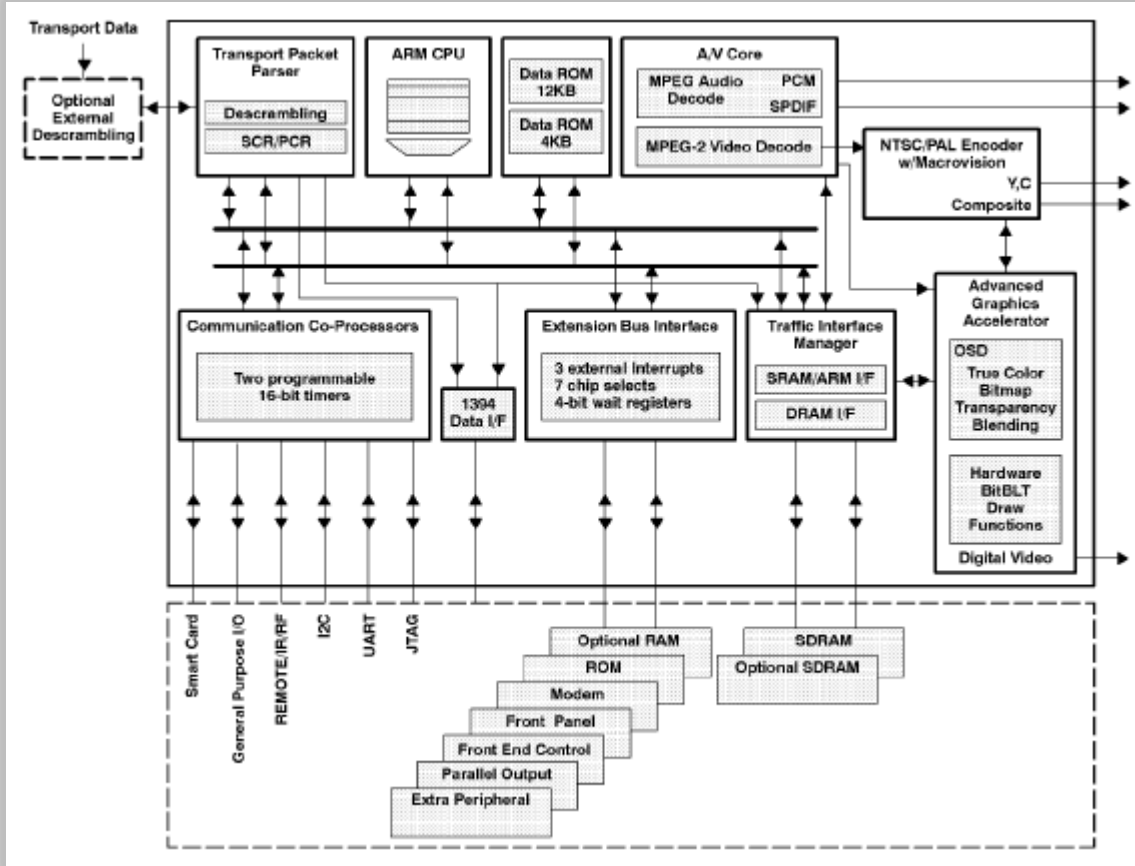
'389 Patent Claim	Exemplary Prior Art Disclosure
53. The apparatus of claim 32, wherein said Media Switch allows the CPU to queue up Direct Memory Access (DMA) transfers.	AV7110 Preview discloses or at least renders obvious “said Media Switch allows the CPU to queue up Direct Memory Access (DMA) transfers” based on at least the following exemplary disclosures:  <i>See claim 22.</i>
[61pre]. An apparatus for the simultaneous storage and play back of multimedia data, comprising:	To the extent that the preamble is limiting, AV7110 Preview discloses or at least renders obvious “an apparatus for the simultaneous storage and play back of multimedia data” based on at least the following exemplary disclosures:  <i>See claim [31pre].</i>
[61a] a physical data source, wherein said physical data source accepts broadcast data from an input device, parses video and audio data from said broadcast data, and temporarily stores said video and audio data;	AV7110 Preview discloses or at least renders obvious “a physical data source, wherein said physical data source accepts broadcast data from an input device, parses video and audio data from said broadcast data, and temporarily stores said video and audio data” based on at least the following exemplary disclosures:  <i>See claim [31a].</i>
[61b] a source object, wherein said source object extracts video and audio data from said physical data source;	AV7110 Preview discloses or at least renders obvious “a source object, wherein said source object extracts video and audio data from said physical data source” based on at least the following exemplary disclosures:  <i>See claim [31b].</i>
[61c] a transform object, wherein said transform object stores and retrieves data streams onto a storage device;	AV7110 Preview discloses or at least renders obvious “a transform object, wherein said transform object stores and retrieves data streams onto a storage device” based on at least the following exemplary disclosures:  <i>See claim [31c].</i>
[61d] wherein said source object obtains a buffer from said transform object, said source object converts video data into data streams and fills said buffer with said streams;	AV7110 Preview discloses or at least renders obvious “wherein said source object obtains a buffer from said transform object, said source object converts video data into data streams and fills said buffer with said streams” based on at least the following exemplary disclosures:  <i>See claim [31d].</i>

<b>'389 Patent Claim</b>	<b>Exemplary Prior Art Disclosure</b>
[61e] wherein said source object is automatically flow controlled by said transform object;	AV7110 Preview discloses or at least renders obvious “wherein said source object is automatically flow controlled by said transform object” based on at least the following exemplary disclosures:  <i>See claim [31e].</i>
[61f] a sink object, wherein said sink object obtains data stream buffers from said transform object and outputs said streams to a video and audio decoder;	AV7110 Preview discloses or at least renders obvious “a sink object, wherein said sink object obtains data stream buffers from said transform object and outputs said streams to a video and audio decoder” based on at least the following exemplary disclosures:  <i>See claim [31f].</i>
[61g] wherein said decoder converts said streams into display signals and sends said signals to a display;	AV7110 Preview discloses or at least renders obvious “wherein said decoder converts said streams into display signals and sends said signals to a display” based on at least the following exemplary disclosures:  <i>See claim [31g].</i>
[61h] wherein said sink object is automatically flow controlled by said transform object;	AV7110 Preview discloses or at least renders obvious “wherein said sink object is automatically flow controlled by said transform object” based on at least the following exemplary disclosures:  <i>See claim [31h].</i>
[61i] a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system; and	AV7110 Preview discloses or at least renders obvious “a control object, wherein said control object receives commands from a user, said commands control the flow of the broadcast data through the system” based on at least the following exemplary disclosures:  <i>See claim [31i].</i>
[61j] wherein said control object sends flow command events to said source, transform, and sink objects.	AV7110 Preview discloses or at least renders obvious “wherein said control object sends flow command events to said source, transform, and sink objects” based on at least the following exemplary disclosures:  <i>See claim [31j].</i>

**Invalidity Contentions for U.S. Patent No. 7,558,472****Based on “Product Preview: TMS320AV7100 Integrated Set-Top Digital Signal Processor” (“AV7100 Preview”)**

Based upon TiVo’s Complaint, Infringement Contentions, and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered, the reference charted below anticipates or at least renders obvious the asserted claims. These invalidity contentions are not an admission by Samsung that the accused products are covered by, or infringe the asserted claims, particularly when these claims are properly construed and applied. These invalidity contentions are not an admission that Samsung concedes or acquiesces to any claim construction implied or suggested by TiVo’s Complaint or Infringement Contentions. Nor is Samsung asserting any claim construction positions through these charts, including whether the preamble is a limitation. The portions of the prior art reference cited below are not exhaustive but are exemplary in nature.

<b>’472 Patent Claim</b>	<b>Exemplary Prior Art Disclosure</b>
<b>Claim 1</b>	
[1p] A system for the simultaneous storage and playback of multimedia data, comprising:	<p>To the extent that the preamble is limiting, the AV7100 Preview discloses or at least renders obvious a system for the simultaneous storage and playback of multimedia data. For example:</p> <p>“The TMS320AV7100 Integrated Digital Satellite System (DSS) Set-Top Digital Signal Processor (‘AV7100) is designed to be the core of a digital set-top box. It incorporates an Advanced RISC Machines (ARM) central processor, a transport bit stream decoder, an MPEG video and audio decoder, an NTSC/PAL (National Television Standards Committee/Phase Alternating Line) video encoder, an on-screen display controller to mix graphics and video, a 1394 interface to an external 1394 device, two universal asynchronous receiver transmitter (UART) serial data interfaces, infra red (IR) and radio frequency (RF) remote control inputs, REMOTE input and output, a smart card interface, and an extension bus to connect peripherals, such as additional RS232 ports, display and control panels, and additional read-only memory (ROM) and dynamic RAM (DRAM). External program and data memory expansion allows the ‘AV7100 to support a range of set-top boxes from low- to high-end.” AV7100 Preview at 1.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	 <p>The diagram illustrates the AV7100 system architecture. It begins with 'Transport Data' entering a dashed box containing 'Optional External Descrambling'. This leads to a 'Transport Packet Parser' which includes 'Descrambling' and 'SCR/PCR' blocks. The data then flows to an 'ARM CPU' and 'Data ROM' (12KB and 4KB). The 'A/V Core' contains 'MPEG Audio Decode', 'PCM', 'SPDIF', and 'MPEG-2 Video Decode' blocks. The output of the A/V Core goes to an 'NTSC/PAL Encoder w/Macrovision' which produces 'Y,C' and 'Composite' signals. The system also includes 'Communication Co-Processors' with 'Two programmable 16-bit timers', an 'Extension Bus Interface' with '3 external interrupts', '7 chip selects', and '4-bit wait registers', and a 'Traffic Interface Manager' with 'SRAM/ARM I/F' and 'DRAM I/F'. These components are connected to a central bus. The bus also connects to 'Optional RAM', 'ROM', 'Modem', 'Front Panel', 'Front End Control', 'Parallel Output', and 'Extra Peripheral'. The 'Advanced Graphics Accelerator' includes 'OSD', 'True Color', 'Bitmap', 'Transparency', and 'Blending' blocks, and 'Hardware BitBLT Draw Functions'. The final output is 'Digital Video'.</p> <p>AV7100 Preview at 9 fig. 1.</p> <p>“trick mode decoding</p> <p>When decoding a picture from a digital recorder, the ‘AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li> </ul> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p> <div> <pre> graph LR     In(( )) --&gt; I1394[1394 Interface]     I1394 --&gt; MUX[MUX]     MUX --&gt; TPP[TPP]     MUX --&gt; DES[DES]     TPP &lt;--&gt; DES     TPP --&gt; I1394     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM[RAM]   </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p>



'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“extension bus read and write timing The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p> <p><i>See claim 1 at 1a-1j, infra.</i></p>
[1a] an input section for acquiring an input signal;	<p>AV7100 Preview discloses or at least renders obvious an input section for acquiring an input signal. For example:</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention.” AV7100 Preview at 15.</p> <p>“input interface The transport packet data from the FEC device is input to the ‘AV7100 eight bits at a time, using the byte clock, DCLK. A high on PACCLK signals valid packet data. During satellite sourced decode, a DERROR signal is received from the FEC device to indicate that a packet has data errors. The DERROR pin is valid on the first byte or one data byte cycle before the first data byte. It does not change until the following packet.” AV7100 Preview at 16; <i>see also id.</i> at 17 fig. 5 (illustrating input interface timing).</p> <p><i>See</i> AV7100 Preview at 1 (stating that the AV7100 “[a]ccepts Transport Bit Stream Up to 40-MBits per Second”).</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p>“During recording, it is assumed that input data originates from the FEC device. An FEC error signal sets the DERROR pin at or before the first byte of input data. This DERROR value is sent to the PERROR output on the 1394 interface coincident with the first valid PDATA. The PERROR value remains active as long as the FEC device keeps DERROR active. Typically, the FEC device retains DERROR until the beginning of the following packet. In this case, the 1394 link device may check for record errors at the first data byte of the packet.” AV7100 Preview at 54.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
<p>[1b] an output section, wherein said input signal is passed to said output section as a transport stream; said output section including:</p>	<p>AV7100 Preview discloses or at least renders obvious an output section, wherein said input signal is passed to said output section as a transport stream. For example:</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“During recording, it is assumed that input data originates from the FEC device. An FEC error signal sets the DERROR pin at or before the first byte of input data. This DERROR value is sent to the PERROR output on the 1394 interface coincident with the first valid PDATA. The PERROR value remains active as long as the FEC device keeps DERROR active. Typically, the FEC device retains DERROR until the beginning of the following packet. In this case, the 1394 link device may check for record errors at the first data byte of the packet.” AV7100 Preview at 54.</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p><i>See</i> AV7100 Preview at 1 (stating that the AV7100 “[a]ccepts Transport Bit Stream Up to 40-MBits per Second”).</p> <p>“Video Decoder Decodes MPEG-1 (Moving Pictures Experts Group) and MPEG-2 Main Profile and Main Level Bit Stream</p> <ul style="list-style-type: none"> <li>• Audio Decoder Decodes MPEG-1 Layer I and II Bit Stream” AV7100 Preview at 1.</li> </ul> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Supports output data in both PCM and SPDIF formats</li> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for sychronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF</p>

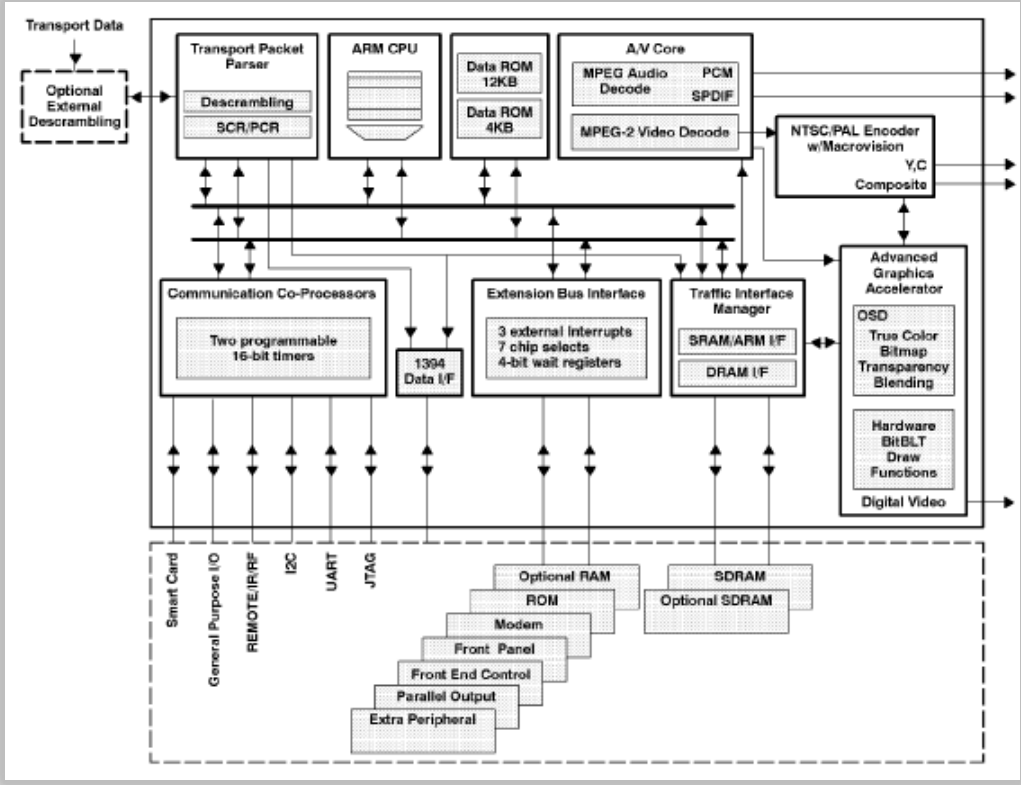
'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p>“The video decoder is capable of producing decimated pictures using <math>\frac{1}{2}</math> or <math>\frac{1}{4}</math> decimation per dimension, which results in reduced areas of <math>\frac{1}{4}</math> or <math>\frac{1}{16}</math>, respectively. The decimated picture can be viewed in real time. Decimation is achieved by using field data out of a frame, skipping lines, and performing vertical filtering to smooth the decimated image.” AV7100 Preview at 19.</p> <p><i>See</i> AV7100 Preview at 19 (describing (1) display formats supported by AV7100, (2) aspect ratio conversion supported by the AV7100).</p> <p>“Audio Output in Both Pulse Code Modulation (PCM) and SPDIF Formats On-Screen Display (OSD) Processor Enables Mixture of OSD and Video Data With Transparency” AV7100 Preview at 1.</p> <p>“On-Chip NTSC/PAL Encoder Incorporates Closed Caption and Video Aspect Ratio Identification Signal Encoding and the Macrovision® Logic for Anti-Taping Protection Analog Y, C, and Composite Video Outputs With 9-Bit Precision Internally or Externally Generated Video Synchronization Signals Digital Video Component Output That Also Contains Aspect Ratio Identification Code” AV7100 Preview at 1.</p> <p>“Both the video and audio decoders synchronize their presentation using the transmitted PTS. For DSS the PTS is transmitted as picture user data in the video bit stream and as an MPEG-1 system packet bit stream for audio. Dedicated hardware decodes the PTS if it is in the MPEG-1 system packet and forwards it to the audio decoder. The video decoder decodes PTS from picture user data. Both the video and audio decoders compare PTS to the local system clock in order to synchronize presentation of reconstructed data. The local system clock is continuously updated by the ARM. When the PTS and local system clock do not match within tolerance, the video decoder either redisplay or skips a frame. At that time, the CC/EDS is handled as follows:</p> <ul style="list-style-type: none"> <li>• When the video decoder redisplay a frame, the second display does not contain CC/EDS.</li> <li>• When the video decoder skips a frame, the corresponding CC/EDS is also skipped.” AV7100 Preview at 20.</li> </ul>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The OSD module is responsible for managing OSD data from different OSD windows and blending them with the video. The OSD module accepts video from the video decoder, reads OSD data from SDRAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces. OSD defaults to standby mode and simply routes video from the video decoder to both outputs. The ARM is responsible for turning on/off OSD operations and for setting specific window attributes of the OSD windows. Dedicated bitBLT hardware attached to the OSD module provides acceleration to memory block moves and graphics operations. OSD data may originate from the user data in the bit stream or may be generated by applications executed on the ARM. Regardless of the source, the OSD data is stored in the SDRAM and managed by the ARM. Memory space in the single 16 Mbits SDRAM is limited to approximately 241 kbytes for OSD, with capability to increase this to approximately 391 kbytes using the half resolution display mode. The OSD data may be represented in one of the following forms: bitmap, graphics 4:4:4 component, 4:2:2 component, or simply background color.” AV7100 Preview at 22; <i>see also id.</i> at 21, 22-24 (describing additional aspects of the OSD module).</p> <p>“The ‘AV7100 provides video output signals encoded for display on a video monitor. The encoded data may include video data or blended video and OSD data. The encoder supports the NTSC format and PAL B, D, G/H and I display formats. The NTSC/PAL pin selects between NTSC and PAL output. Changing between NTSC and PAL requires a hardware reset of the device.</p> <p>The encoder uses 9-bit D/A converters (DACs) to produce an analog S-video signal on separate luminance M and chrominance © channels. An analog composite (Comp) signal is also output. Output signals conform to the RS 170A standard. Application circuits for external connections to the DAG outputs are illustrated in Figure 24. With a single-ended 75 Q load, the output current for peak white is 20 mA.” AV7100 Preview at 26.</p> <p>“The ‘AV7100 also supports various features for video display and control. Closed caption (CC) and Extended Data Services (EDS) information which has been extracted by the video decoder is passed to the ‘AV7100 encoder. The encoder then presents CC data at video line 21 and EDS at video line 284. The video decoder also extracts aspect ratio data from the bit stream and sends it to the ARM, which in turn prepares data according to the video aspect ratio identification signal (VARIS) standard, EIAJ CPX-1204. The ARM forwards VARIS codes to the ‘AV7100 NTSC/PAL module where the codes are inserted onto the 20<sup>th</sup> video line for NTSC and 23<sup>rd</sup> line for PAL.” AV7100 Preview at 26.</p> <p>“The ‘AV7100 provides a digital output interface for pure video or blended video and OSD. The digital output includes video in either 4:4:4 or 4:2:2 YCrCb format. VARIS coding for aspect ratio is also provided at the</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>beginning of each video frame. The video output format is programmable by the user, but defaults to 4:2:2. The pin assignments for the digital video output signals are:  8-bit Cb/Y/Cr/Y and VARIS multiplexed data output  27-MHz or 40.5-MHz clock output  YCOOUT(8)  YCCLK(1)  YCCTRL(2) 2-bit control signals to distinguish between YCrCb components and VARIS code” AV7100 Preview at 26; <i>see also id.</i> at 26-29 (describing additional aspects of the digital video output interface).</p> <p>“PCM audio output  The 2s complement PCM data is output serially on the PCM OUT pin using the serial clock ASCLK. ASCLK is derived from the PCM clock, PCMCLK, according to the PCMSEL 1 :O bits in the control register. The PCM clock  must be the proper multiple of the sampling frequency of the bit stream. The PCMCLK may be input to the device or internally derived from an 36.864-MHz clock. The data on the PCMOUT pin alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7100 Preview at 31; <i>see id.</i> fig. 9 (showing timing for the PCM data).</p> <p>“SPDIF audio output  The SPDIF output conforms to a subset of the AES3 standard for serial transmission of digital audio data. The SPDIF format is a subset of the minimum implementation of AES3.” AV7100 Preview at 31.</p> <p><i>See claim 1 at 1c-1j, infra.</i></p>
[1c] a processor;	<p>AV7100 Preview discloses or at least renders obvious a processor. For example:</p> <p>“ARM CPU features</p> <ul style="list-style-type: none"> <li>• Operates at 40.5 MHz</li> <li>• Supports byte (8-bit), half-word (16-bit), and word (32-bit) data types</li> <li>• Reads instructions from on-chip ROM or from the ‘AV7100 extension bus</li> <li>• Switchable between ARM (32-bit) or THUMB (16-bit) instruction modes</li> <li>• 32-bit data and 32-bit address lines</li> </ul>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Seven processing modes</li> <li>• Two interrupts, fast interrupt request (FIQ) and interrupt request (IRQ)” AV7100 Preview at 11.</li> </ul> <p>“The ARM7TDM I/THUMB is the integrated CPU of the ‘AV7100. The ARM is a 32-bit RISC processor which is capable of executing instructions in 16- or 32-bit format at a clock frequency of 40.5 MHz. The standard ARM instructions are exactly one word (32 bits) in length, and the data operations are performed on word quantities only. However, LOAD and STORE instructions can transfer either byte, half-word, or word quantities. The ARM THUMB mode uses the same 32-bit architecture with a 16-bit instruction set. This mode retains the 32-bit performance, but reduces the code size with 16-bit instructions. With 16-bit instructions, THUMB still gives 70 - 80% of the performance of the ARM as when running ARM instructions from 32-bit memory. In this data sheet, ARM and THUMB are used interchangeably.” AV7100 Preview at 11.</p> <p>“The ARM uses a LOAD and STORE architecture such that all operations are on the registers. The ARM has seven different processing modes, with sixteen 32-bit registers visible in user mode. In the THUMB configuration there are only eight registers available in user mode. However, the high registers may be accessed through special instructions. The instruction pipeline is three stage, fetch - decode - execute, and most instructions take only one cycle to execute.” AV7100 Preview at 11.</p>
[1d] a decoder subsystem that decodes said transport stream, said decoder subsystem connected to said processor by a first data bus; and	AV7100 Preview discloses or at least renders obvious a decoder subsystem that decodes said transport stream, said decoder subsystem connected to said processor by a first data bus. For example:



'472 Patent Claim	Exemplary Prior Art Disclosure
	 <p>The diagram illustrates the AV7100 system architecture. It features a central processing core with several key components: a Transport Packet Parser (including Descrambling and SCR/PCR), an ARM CPU, Data ROM (12KB and 4KB), and an A/V Core (including MPEG Audio Decode, PCM SPDIF, and MPEG-2 Video Decode). This core is connected to a Communication Co-Processors block (with two programmable 16-bit timers), an Extension Bus Interface (with 3 external interrupts, 7 chip selects, and 4-bit wait registers), and a Traffic Interface Manager (with SRAM/ARM I/F and DRAM I/F). The system also includes an NTSC/PAL Encoder w/Macrovision, an Advanced Graphics Accelerator (with OSD, True Color, Bitmap, Transparency, and Blending), and Hardware BitBLT Draw Functions. External peripherals are connected via Smart Card, General Purpose I/O, REMOTE/IR/F, I2C, UART, JTAG, and a 1394 Data I/F. Other components include Optional RAM, ROM, Modem, Front Panel, Front End Control, Parallel Output, Extra Peripheral, and SDRAM. The system outputs NTSC/PAL Composite, Y/C, and Digital Video signals.</p> <p>AV7100 Preview at 9 fig. 1.</p> <p>“Video Decoder Decodes MPEG-1 (Moving Pictures Experts Group) and MPEG-2 Main Profile and Main Level Bit Stream  • Audio Decoder Decodes MPEG-1 Layer I and II Bit Stream” AV7100 Preview at 1.</p> <p>“transport packet parser features  • Parses transport bit streams  • Accepts bit stream from either the front end device or the 1394 interface  • Performs system clock reference recovery</p>

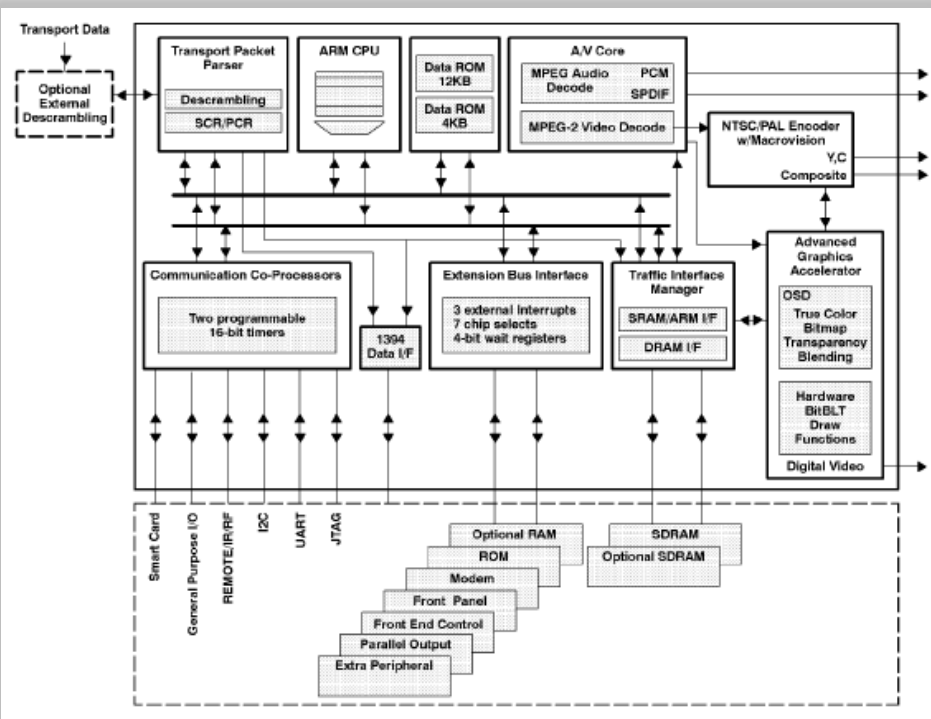
'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p>“transport bit stream processing</p> <p>The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.</p> <p>The TPP also activates or deactivates the decryption engine based upon the content of the individual packet. The conditional access keys are stored in RAM and managed by firmware running on the ARM. The TPP will also detect packets lost from the transport stream. Using error concealment by the audio/video decoder and redundant header information from the DSS bit stream, the ‘AV7100 minimizes the effects of lost data.” AV7100 Preview at 15.</p> <p>“video decoder features</p> <ul style="list-style-type: none"> <li>• Real-time video decoding of MPEG-2 Main Profile and Main Level Bit Stream and MPEG-1</li> <li>• Error detection and concealment</li> <li>• Internal 90 kHz/27-MHz system time clock</li> <li>• Sustained input rate of 15 Mbps</li> <li>• Supports trick mode with full trick mode picture</li> <li>• Provides ¼ and 1/16 decimated picture size</li> <li>• Extracts closed caption and other picture user data from the bit stream</li> <li>• 3:2 pulldown in NTSC mode</li> </ul>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Supports various display formats with polyphase horizontal resampling and vertical chrominance filtering</li> <li>• Pan-and-scan for 16:9 source material according to both DSS and MPEG syntax</li> <li>• High-level command interface</li> <li>• Synchronization using presentation time stamps (PTS)</li> <li>• Half resolution display mode allows additional OSD space in the SDRAM” AV7100 Preview at 18.</li> </ul> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p> <p>“trick mode decoding</p> <p>When decoding a picture from a digital recorder, the ‘AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li> </ul> <p>“The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder AP ls. Consult the TMS320AV7100 Software Guide for details.” AV7100 Preview at 20; <i>see id.</i> tbl. 8 (showing video decoder commands).</p> <p>“audio decoder features</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Supports output data in both PCM and SPDIF formats</li> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p><i>See</i> AV7100 Preview at 31-32 (listing and describing audio decoder control and status registers).</p> <p>“extension bus interface  The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus. Each CS has its own defined memory space and a programmable wait register. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. . . .  The extension bus supports the connection of seven devices using the predefined chip selects. Additional devices may be used by externally decoding the address bus. Table 21 shows the name of the device, its chip select, address range, and programmable wait state. Table 22 and Table 23 show extension bus wait state and configuration registers. Each device on the extension bus is required to have data outputs in high-impedance state within one clock cycle following the removal of chip-select.” AV7100 Preview at 37.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure																																
	<div><p><b>Table 21. Extension Bus Chip Selects</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 MBytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 32 MBytes)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7100 Preview at 37 tbl. 21.</p> <p>“extension bus read and write timing</p> <p>The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p> <p>“EXTWAIT signal</p> <p>The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it must become active before the programmable wait cycle expires. The total number of wait states should not exceed the maximum allowed from Table 21. If the combined total wait states exceed the maximum, the decoder is not guaranteed to function properly. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT should be at least 24.7 ns. Because the EXTWAIT signal has the potential to stall the decoding process, the ARM will cap its wait at 500 ns. After this time, the ARM assumes the device that generated the EXTWAIT has failed and ignores EXTWAIT from that point forward. Only a software or hardware reset can activate the EXTWAIT signal again. . . .</p> <p>If an 8-bit device is connected to the extension bus, the EBI automatically converts the single ARM word access to four consecutive byte accesses, and the maximum wait time applies to the total of the four byte accesses. In the consecutive read access where the CS remains active during the reading of four bytes, each byte access has to</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)	N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE																														
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CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device																														
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port																														

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	<p>complete within 125 ns. For a device that requires longer access delay, for example 250 ns, then the access from the ARM has to be limited only to half words. In a write access, where the CS toggles for each byte write, each write can take 500 ns.” AV7100 Preview at 42.</p> <p>“The extension bus supports access to 60 or 70 ns DRAM. The DRAM must have an 8-bit, 9-bit, or 10-bit column address and must have a data width of 8 or 16 bits. Byte access is allowed even when the DRAM has a 16-bit data width. The byte access is specified by the signal DCAS for EXTDATA[15:8] and CCAS for EXTDATA[7:0]. The system default DRAM configuration is 70 ns, 9-bit column address, and 16-bit data width. The firmware verifies the DRAM configuration during startup.” AV7100 Preview at 43; <i>see id.</i> at 43-50 (describing additional aspects of extension bus DRAM).</p> <p>“traffic controller features</p> <ul style="list-style-type: none"> <li>• Authorizes and manages direct memory access (DMA) transfers</li> <li>• Provides SDRAM interface</li> <li>• Provides memory access protection</li> <li>• Manages interrupt requests</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>TTP/DES to/from internal data RAM</li> <li>Data RAM to/from extension bus SDRAM to OSD</li> <li>Audio and video decoders to/from SDRAM</li> <li>SDRAM to/from data RAM</li> </ul> </li> <li>• Manages extension bus</li> <li>• Generates chip selects for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus” AV7100 Preview at 12.</li> </ul> <p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>See claim 1 at 1b, <i>supra</i>.</p>
<p>[1e] a media switch connected to said decoder subsystem by a second data bus, said media switch operative to interface a plurality of system components and operates asynchronously from said processor, wherein said media switch comprises a media manager, said media manager including:</p>	<p>AV7100 Preview discloses or at least renders obvious a media switch connected to said decoder subsystem by a second data bus, said media switch operative to interface a plurality of system components and operates asynchronously from said processor, wherein said media switch comprises a media manager. For example:</p>  <p>AV7100 Preview at 9 fig. 1.</p> <p>“traffic controller features</p> <ul style="list-style-type: none"> <li>• Authorizes and manages direct memory access (DMA) transfers</li> <li>• Provides SDRAM interface</li> </ul>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Provides memory access protection</li> <li>• Manages interrupt requests</li> <li>• Manages the data flow between processors and memories               <ul style="list-style-type: none"> <li>TTP/DES to/from internal data RAM</li> <li>Data RAM to/from extension bus SDRAM to OSD</li> <li>Audio and video decoders to/from SDRAM</li> <li>SDRAM to/from data RAM</li> </ul> </li> <li>• Manages extension bus</li> <li>• Generates chip selects for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus” AV7100 Preview at 12.</li> </ul> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware” AV7100 Preview at 15.</li> </ul> <p>“transport bit stream processing</p> <p>The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.</p>



'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>The TPP also activates or deactivates the decryption engine based upon the content of the individual packet. The conditional access keys are stored in RAM and managed by firmware running on the ARM. The TPP will also detect packets lost from the transport stream. Using error concealment by the audio/video decoder and redundant header information from the DSS bit stream, the 'AV7100 minimizes the effects of lost data." AV7100 Preview at 15.</p> <p>"ARM CPU features</p> <ul style="list-style-type: none"> <li>• Operates at 40.5 MHz</li> <li>• Supports byte (8-bit), half-word (16-bit), and word (32-bit) data types</li> <li>• Reads instructions from on-chip ROM or from the 'AV7100 extension bus</li> <li>• Switchable between ARM (32-bit) or THUMB (16-bit) instruction modes</li> <li>• 32-bit data and 32-bit address lines</li> <li>• Seven processing modes</li> <li>• Two interrupts, fast interrupt request (FIQ) and interrupt request (IRQ)" AV7100 Preview at 11.</li> </ul> <p>"The SDRAM interface supports 16-bit data width SDRAM operating at minimum 81 MHz. The SDRAM selected for use with the 'AV7100 should meet or exceed the timing requirements in Table 3 for proper operation. The TI TMS626162-12 is one example of a compatible 16 Mbit SDRAM." AV7100 Preview at 13.</p> <p>"system clock reference recovery</p> <p>Combined with the ARM, the TPP also handles system clock reference (SCR) recovery with an external VCXO. The TPP latches and transfers its internal system clock to the ARM upon the arrival of any packet which contains system clock information. After further processing of the packet and identification of the system clock, the ARM calculates the difference between the system clock from the bit stream and the internal system clock at the time the packet arrives. The ARM filters this difference and routes it through a Sigma-Delta digital-to-analog converter to control an external VCXO. Output from the 'AV7100 VCXO CTRL pin is a digital pulse train with 8-bit resolution for control. During startup, when there is no incoming SCR, the ARM drives the VCXO to its center frequency. Figure 4 provides an example circuit for the external VCXO." AV7100 Preview at 15; <i>see id.</i> tbl. 4.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>The diagram shows an external clock generator circuit. A VCXO_CTRL signal is connected to the control pin of a VCXO (Variable Crystal Oscillator) through a 22 kΩ resistor. The VCXO output is connected to CLK27 through a 100 pF capacitor. The VCXO is powered by +5V through a 2.2 kΩ resistor. The output of the VCXO is also connected to a 100 kΩ resistor, which is connected to the non-inverting input of a buffer. The buffer's output is connected to the CLK27 pin through a 100 Ω resistor. The buffer is powered by +5V through a 100 kΩ resistor. Two HVU359TRF Vari-Cap capacitors are connected between the +5V supply and ground, each controlled by a 100 kΩ resistor. A 27 MHz crystal is connected between the two Vari-Cap capacitors. A 1 MΩ resistor is connected between the two Vari-Cap capacitors. A 100 pF capacitor is connected between the two Vari-Cap capacitors. A 100 Ω resistor is connected between the two Vari-Cap capacitors. A 0.1 μF capacitor is connected between the two Vari-Cap capacitors.</p> <p>AV7100 Preview at 16 fig. 4.</p> <p>“Both the video and audio decoders synchronize their presentation using the transmitted PTS. For DSS the PTS is transmitted as picture user data in the video bit stream and as an MPEG-1 system packet bit stream for audio. Dedicated hardware decodes the PTS if it is in the MPEG-1 system packet and forwards it to the audio decoder. The video decoder decodes PTS from picture user data. Both the video and audio decoders compare PTS to the local system clock in order to synchronize presentation of reconstructed data. The local system clock is continuously updated by the ARM.</p> <p>When the PTS and local system clock do not match within tolerance, the video decoder either redisplay or skips a frame. At that time, the CC/EDS is handled as follows:</p> <ul style="list-style-type: none"> <li>• When the video decoder redisplay a frame, the second display does not contain CC/EDS.</li> <li>• When the video decoder skips a frame, the corresponding CC/EDS is also skipped.” AV7100 Preview at 20.</li> </ul> <p>“When the PCM_SRC pin is low, the ‘AV7100 audio PLL is used to generate the necessary output clocks for the audio data, phase locked to the input bit stream. The clock generator requires an 36.864-MHz external VCXO. The AUD PLLO pin outputs a control voltage that can be applied to the external loop filter and VCXO to produce the required input at the AUD PLLI pin. The clock generator derives the correct output clocks, based on the contents of the audio control register bits PCMSSEL1-0, shown in Table 17. An example of the external clock</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>circuit configuration is illustrated in Figure 23.” AV7100 Preview at 30; <i>see also id.</i> tbl. 17 (showing audio clock frequencies).</p> <p>“All firmware is stored in on-chip ROM, except the OSD graphics and some generic run-time support. The run-time support library (RTSL) and all user application software are stored outside the 'AV7100 in external memory attached to the extension bus. Details of the firmware, RTSL, and application program interface (API) are provided in the companion software document, TMS320AV7100 Software Guide.” AV7110 Product Preview at 11.</p> <p>“communication coprocessor features</p> <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> <li>• Provides three UARTs - one for smart card and two for general use</li> <li>• Accepts IR, REMOTE, and RF signals</li> <li>• Provides a REMOTE output</li> <li>• Provides two general purpose I/Os</li> <li>• Manages I2C and JTAG interfaces” AV7100 Preview at 33.</li> </ul> <p>“The communication coprocessor consists of a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR/RF, I2C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM. Interrupts are used to communicate between these interface modules and the ARM.” AV7100 Preview at 33.</p> <p>“The ‘AV7100 includes an interface to the smart card access control system. The interface consists of a high-speed UART and logic to comply with the News Datacom specification (Document #HU-T052, Release E, dated November 1994, and Release F, dated January 1996) “DirecTV Project: Decoder-Smart Card Interface Requirements.” Applicable software drivers that control the interface are also included, and detailed in the companion software document for the ‘AV7100.” AV7100 Preview at 33.</p> <p>“conditional access and DES processing</p> <p>The conditional access is triggered by the arrival of a control word packet (CWP). The ARM firmware recognizes that a CWP has been received and passes it to the verifier, which is the user-implemented News Datacom application software running on the ARM. The verifier reads the CWP and communicates with the external smart</p>

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	<p>card through a UART I/O interface. After verification, it passes the pointer to an 8-byte key back to the firmware, which then loads the key for the DES to decrypt succeeding packets.” AV7100 Preview at 33; <i>see id.</i> at 16 (describing additional aspects of processing transport data).</p> <p>“UART interfaces The ‘AV7100 includes two general purpose 2-wire UARTs that are memory mapped and fully accessible by application programs. The UARTs operate in asynchronous mode only and support baud rates of 1200, 2400, 4800, 9600, 14400, 19200, 28800, and 57600 kbps. The UARTs are full duplex. The transmitter is double buffered, and the receive interface is buffered with eight bytes of FIFO memory in addition to its internal register. The UARTs transmit/receive 1 start bit, 7 or 8 data bits, optional parity, and 1 or 2 stop bits. The outputs of the UARTs are digital and require external level shifters for RS232 compliance.” AV7100 Preview at 33; <i>see id.</i> at 33-34 (describing additional aspects of the UART interface).</p> <p>“The IR/RF remote control interface is a means of transmitting user commands to the set-top box. This interface consists of a custom hardware receiver implementing a bit frame-based communication protocol. A single bit frame represents a user command. The IR, RF, and REMOTEIN ports require a square wave input with no false transitions; therefore, the signal must reach its threshold prior to being applied to the pins. The interface accepts an IR, RF, or REMOTEIN data stream up to a frequency of 1.3 kHz. Since more than one data stream may be active at any given time, the ‘AV7100 hardware determines priority so that only one IR, RF, or REMOTE input is decoded.” AV7100 Preview at 35; <i>see id.</i> at 35-36 (describing additional aspects of the IR/RF remote control interface).</p> <p>“general purpose I/Os The ‘AV7100 includes two user-configurable I/O pins, 101 and 102. 101 and 102 are supported by dedicated 32-bit control/status registers, named IOSCR1 and IOSCR2, respectively.” AV7100 Preview at 36; <i>see id.</i> tbl. 20 (providing register descriptions for the control/status registers); <i>id.</i> at 37 (describing additional aspects of general purpose I/O).</p> <p>“I2C interface The ‘AV7100 includes an I2C serial bus interface that can act as either a master or slave. (Master mode is the default). In master mode, the ‘AV7100 initiates and terminates transfers and generates clock signals. Only the standard mode (100 kbit/s) I2C-bus system is implemented; fast mode is not supported. Multi-master mode is also not supported.</p>

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	<p>To put the device in slave mode the application program must set the slave mode select and a 7-bit address for the 'AV7100. The application must also send a software reset to the 12C to complete the transition to slave mode.</p> <p>In slave mode, when the programmable address bits match the applied address, the 'AV7100 responds accordingly. The 'AV7100 also responds to general call commands issued to address 0 (the general call address) that change the programmable part of the slave address. These commands are Ox04 and Ox06. No other general call commands are acknowledged, and no action is taken.” AV7100 Preview at 37.</p> <p>“Note that there is no direct DMA transfer to/from extension bus memories from/to the SDRAM. However, the user can employ the bitBLT hardware (which uses data RAM) as an intermediate step to execute such a transfer. The only constraints for this type of transfer are that the block being transferred must consist of 32-bit multiples, and it must begin at a 32-bit word boundary.” AV7100 Preview at 12.</p> <p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“extension bus interface  The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus. Each CS has its own defined memory space and a programmable wait register. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. . . .  The extension bus supports the connection of seven devices using the predefined chip selects. Additional devices may be used by externally decoding the address bus. . . . Table 22 and Table 23 show extension bus wait state and</p>

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	<p>configuration registers. Each device on the extension bus is required to have data outputs in high-impedance state within one clock cycle following the removal of chip-select.” AV7100 Preview at 37.</p> <div><p><b>Table 21. Extension Bus Chip Selects</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 MBytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 32 MBytes)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7100 Preview at 37 tbl. 21 (showing name of device, its chip select, address range, and programmable wait state).</p> <p>“CS1 is intended for ARM application code, but writes are not prevented. DRAM is read/write accessible by the ARM. It is also accessed by the traffic controller for TPP and bitBLT DMA transfers.</p> <p>CS2, CS3, CS4, and CS5 all have the same characteristics. The ARM performs reads and writes to these devices through the extension bus.</p> <p>CS6 is read and write accessible by the ARM. It is also accessed by the traffic controller for TPP DMAs, and it is write only. The parallel port is one byte wide and accessed via the most significant byte.” AV7100 Preview at 38.</p> <p>“extension bus read and write timing</p> <p>The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p> <p>“EXTWAIT signal</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)	N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE																														
CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)																														
N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)																														
CS2	3000 0000 – 31FF FFFF	1 – 7	Modem																														
CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel																														
CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device																														
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device																														
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port																														

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it must become active before the programmable wait cycle expires. The total number of wait states should not exceed the maximum allowed from Table 21. If the combined total wait states exceed the maximum, the decoder is not guaranteed to function properly. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT should be at least 24.7 ns. Because the EXTWAIT signal has the potential to stall the decoding process, the ARM will cap its wait at 500 ns. After this time, the ARM assumes the device that generated the EXTWAIT has failed and ignores EXTWAIT from that point forward. Only a software or hardware reset can activate the EXTWAIT signal again. . . .</p> <p>If an 8-bit device is connected to the extension bus, the EBI automatically converts the single ARM word access to four consecutive byte accesses, and the maximum wait time applies to the total of the four byte accesses. In the consecutive read access where the CS remains active during the reading of four bytes, each byte access has to complete within 125 ns. For a device that requires longer access delay, for example 250 ns, then the access from the ARM has to be limited only to half words. In a write access, where the CS toggles for each byte write, each write can take 500 ns.” AV7100 Preview at 42.</p> <p>“The extension bus supports access to 60 or 70 ns DRAM. The DRAM must have an 8-bit, 9-bit, or 10-bit column address and must have a data width of 8 or 16 bits. Byte access is allowed even when the DRAM has a 16-bit data width. The byte access is specified by the signal DCAS for EXTDATA[15:8] and CCAS for EXTDATA[7:0]. The system default DRAM configuration is 70 ns, 9-bit column address, and 16-bit data width. The firmware verifies the DRAM configuration during startup.” AV7100 Preview at 43; <i>see id.</i> at 43-50 (describing additional aspects of extension bus DRAM).</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24..” AV7100 Preview at 51-52.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p style="text-align: center;">Figure 19. 1394 Interface</p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p>



'472 Patent Claim	Exemplary Prior Art Disclosure
	<div> <pre> graph LR     In(( )) --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM     1394[1394 Interface] --&gt; MUX     </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24.” AV7100 Preview at 52; <i>see id.</i> tbl. 24 (listing 1394 interface signals).</p> <p><i>See</i> AV7100 Preview at 3 (listing 1394 bus in pin descriptions table).</p> <p><i>See</i> AV7100 Preview at 3-8, table 1 (e.g., “SMCLK,” “SMCLK2”)</p> <p><i>See</i> claim 1 at 1f-1i, <i>infra</i>.</p>
[1f] a host controller;	<p>AV7100 Preview discloses or at least renders obvious a host controller. For example:</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24..” AV7100 Preview at 51-52.</p> <div> <p style="text-align: center;">Figure 19. 1394 Interface</p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP,</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p> <div> <pre> graph LR     In(( )) --&gt; MUX     In --&gt; I1394[1394 Interface]     I1394 --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP &lt;--&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM   </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p><i>See claim 1 at 1j, infra.</i></p>
<p>[1g] a DMA controller;</p>	<p>AV7100 Preview discloses or at least renders obvious a DMA controller. For example:</p> <p>“traffic controller features</p> <ul style="list-style-type: none"> <li>• Authorizes and manages direct memory access (DMA) transfers</li> <li>• Provides SDRAM interface</li> <li>• Provides memory access protection</li> <li>• Manages interrupt requests</li> <li>• Manages the data flow between processors and memories</li> </ul> <p>TTP/DES to/from internal data RAM  Data RAM to/from extension bus SDRAM to OSD  Audio and video decoders to/from SDRAM  SDRAM to/from data RAM</p> <ul style="list-style-type: none"> <li>• Manages extension bus</li> <li>• Generates chip selects for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus” AV7100 Preview at 12. <p>“DMA transfer</p> <p>The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“extension bus read and write timing</p> <p>The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the</p> </li></ul>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p> <p>“The bit BLT hardware provides a fast way to move a block of memory from one space to another. The hardware reads data from a source location, performs shift/mask/merge/expand operations on the data, and finally writes it to a destination location. This hardware enables the following graphics functions:</p> <ul style="list-style-type: none"> <li>• Set/get pixel</li> <li>• Horizontal/vertical line drawing</li> <li>• Block fill</li> <li>• Bit BLT for fonts</li> <li>• Bitmap/graphic bit BLT</li> <li>• Transparency” AV7100 Preview at 25; <i>see id.</i> at 25-26 (describing additional aspects of the bit BLT hardware, including allowable source and destination memories for this module).</li> </ul> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24..” AV7100 Preview at 51-52.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p style="text-align: center;">Figure 19. 1394 Interface</p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p>

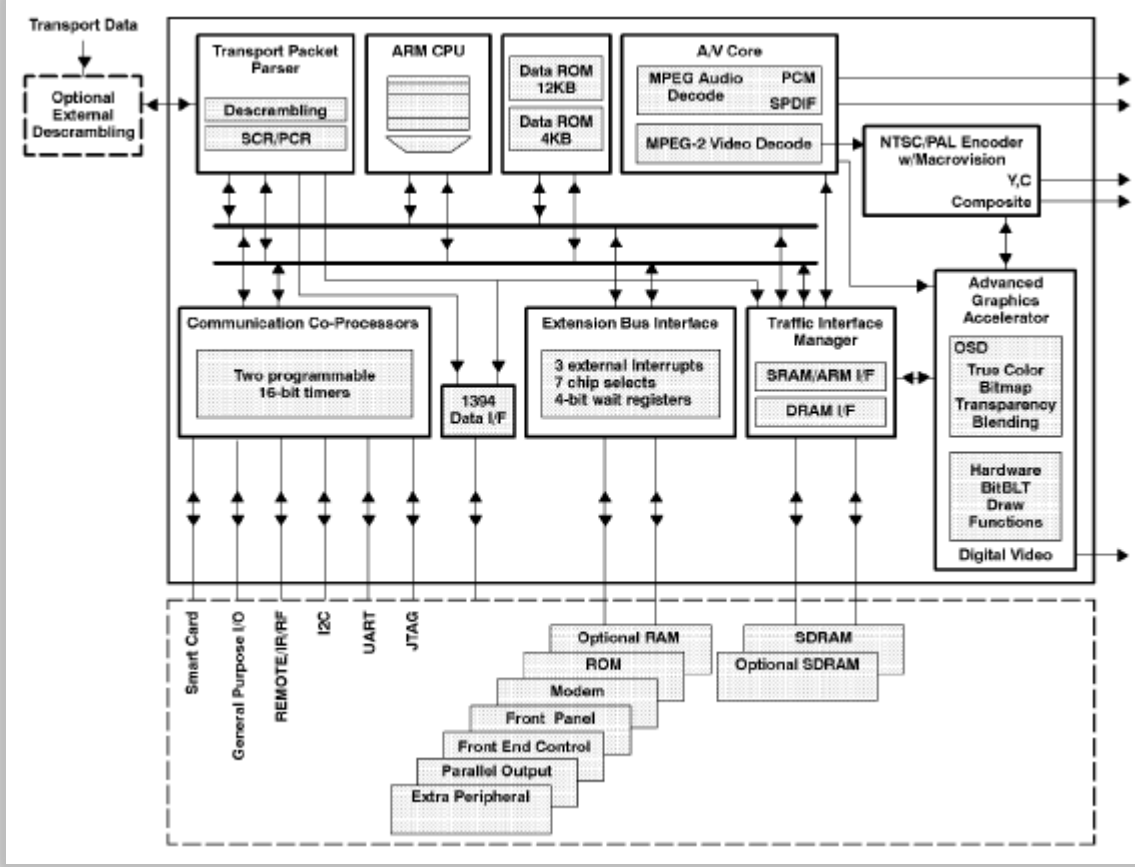
'472 Patent Claim	Exemplary Prior Art Disclosure
	<div> <pre> graph LR     In(( )) --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM     TPP --&gt; I1394[1394 Interface]     I1394 --&gt; MUX </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; see also id. at 53-54 (showing read and write timing relationships on the 1394 interface).</p>

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[1h] a bus arbiter; and	<p>AV7100 Preview discloses or at least renders obvious a bus arbiter. For example:</p> <p>“interrupts There are three externally accessible interrupt lines and three corresponding interrupt acknowledges on the 'AV7100. These three interrupts, along with interrupts generated internally to the 'AV7100, are handled by a centralized interrupt handler. Interrupt mask and priority are managed by the firmware. The three extension bus interrupts are connected to three different interrupt request lines which are visible to the user via the EXTINT2:0 pins. When the interrupt handler on the ARM begins servicing one of these interrupts, the ARM should first issue an interrupt acknowledge, which activates the corresponding EXTACK2:0 output. At the completion of the interrupt servicing, the ARM should reset the interrupt acknowledge, which returns EXTACK2:0 to the inactive state.” AV7100 Preview at 42.</p> <p>“Based on programmable priority, the ARM responds to interrupt requests generated by internal modules and external devices on the extension bus. Some of the requests are for data transfers to internal RAM, whereas others are true interrupts to the ARM. The 'AV7100s traffic controller handles data transfers, and the ARM provides services to true interrupts. Interrupts are grouped into FIQ and IRQ categories. The system software uses FIQ; the application software uses IRQ. The priorities for FIQs and IRQs are managed by the firmware.” AV7100 Preview at 11.</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24.” AV7100 Preview at 51-52; <i>see id.</i> at 51 fig. 19.</p> <p>“extension bus read and write timing The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100</p>



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	<p>requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24..” AV7100 Preview at 51-52.</p> <div> <pre> graph TD     AV7100[AV7100] --- ExternalBus[External Bus]     subgraph TPP [ ]         direction TB         DVCR[DVCR Packetizer]         LINK[LINK Interface]         DVCR --- LINK     end     ExternalBus --- LINK     LINK --- PHY[PHY Interface]     DVCR --- Data[Data]   </pre> <p style="text-align: center;"><b>Figure 19. 1394 Interface</b></p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP,</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p> <div> <pre> graph LR     In(( )) --&gt; I1394[1394 Interface]     I1394 --&gt; MUX[MUX]     MUX --&gt; TPP[TPP]     TPP &lt;--&gt; DES[DES]     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM[RAM]     TPP --&gt; I1394   </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
[1i] a multimedia data stream processor; and	<p>AV7100 Preview discloses or at least renders obvious a multimedia data stream processor. For example:</p>  <p>AV7100 Preview at 9 fig. 1.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p>“transport bit stream processing</p> <p>The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.</p> <p>The TPP also activates or deactivates the decryption engine based upon the content of the individual packet. The conditional access keys are stored in RAM and managed by firmware running on the ARM. The TPP will also detect packets lost from the transport stream. Using error concealment by the audio/video decoder and redundant header information from the DSS bit stream, the ‘AV7100 minimizes the effects of lost data.” AV7100 Preview at 15.</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending them with the video. The OSD module accepts video from the video decoder, reads OSD data from SDRAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces. OSD defaults to standby mode and simply routes video from the video decoder to both outputs. The ARM is responsible for turning on/off OSD operations and for setting specific window attributes of the OSD windows. Dedicated bitBLT</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>hardware attached to the OSD module provides acceleration to memory block moves and graphics operations. OSD data may originate from the user data in the bit stream or may be generated by applications executed on the ARM. Regardless of the source, the OSD data is stored in the SDRAM and managed by the ARM. Memory space in the single 16 Mbits SDRAM is limited to approximately 241 kbytes for OSD, with capability to increase this to approximately 391 kbytes using the half resolution display mode. The OSD data may be represented in one of the following forms: bitmap, graphics 4:4:4 component, 4:2:2 component, or simply background color.” AV7100 Preview at 22; see also id. at 21, 22-24 (describing additional aspects of the OSD module).</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. Figure 19 depicts the connection.” AV7100 Preview at 51.</p> <div> <pre> graph TD     AV7100[AV7100] --- BusLine     BusLine --- ExternalBus[External Bus]     BusLine --- DataLine[Data]     DataLine --- DVCR[DVCR Packetizer]     DVCR --- LINK[LINK Interface]     LINK --- PHY[PHY Interface]     ExternalBus --- LINK   </pre> <p>Figure 19. 1394 Interface</p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“communication coprocessor features</p> <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> </ul>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Provides three UARTs - one for smart card and two for general use</li> <li>• Accepts IR, REMOTE, and RF signals</li> <li>• Provides a REMOTE output</li> <li>• Provides two general purpose I/Os</li> <li>• Manages 12C and JTAG interfaces” AV7100 Preview at 33.</li> </ul> <p>“The communication coprocessor consists of a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR/RF, 12C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM. Interrupts are used to communicate between these interface modules and the ARM.” AV7100 Preview at 33.</p> <p>“The ‘AV7100 includes an interface to the smart card access control system. The interface consists of a high-speed UART and logic to comply with the News Datacom specification (Document #HU-T052, Release E, dated November 1994, and Release F, dated January 1996) “DirecTV Project: Decoder-Smart Card Interface Requirements.” Applicable software drivers that control the interface are also included, and detailed in the companion software document for the ‘AV7100.” AV7100 Preview at 33.</p> <p>“conditional access and DES processing The conditional access is triggered by the arrival of a control word packet (CWP). The ARM firmware recognizes that a CWP has been received and passes it to the verifier, which is the user-implemented News Datacom application software running on the ARM. The verifier reads the CWP and communicates with the external smart card through a UART I/O interface. After verification, it passes the pointer to an 8-byte key back to the firmware, which then loads the key for the DES to decrypt succeeding packets.” AV7100 Preview at 33.</p> <p>“UART interfaces The ‘AV7100 includes two general purpose 2-wire UARTs that are memory mapped and fully accessible by application programs. The UARTs operate in asynchronous mode only and support baud rates of 1200, 2400, 4800, 9600, 14400, 19200, 28800, and 57600 kbps. The UARTs are full duplex. The transmitter is double buffered, and the receive interface is buffered with eight bytes of FIFO memory in addition to its internal register. The UARTs transmit/receive 1 start bit, 7 or 8 data bits, optional parity, and 1 or 2 stop bits. The outputs of the UARTs are digital and require external level shifters for RS232 compliance.” AV7100 Preview at 33; see id. at 33-34 (describing additional aspects of the UART interface).</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The IR/RF remote control interface is a means of transmitting user commands to the set-top box. This interface consists of a custom hardware receiver implementing a bit frame-based communication protocol. A single bit frame represents a user command. The IR, RF, and REMOTEIN ports require a square wave input with no false transitions; therefore, the signal must reach its threshold prior to being applied to the pins. The interface accepts an IR, RF, or REMOTEIN data stream up to a frequency of 1.3 kHz. Since more than one data stream may be active at any given time, the ‘AV7100 hardware determines priority so that only one IR, RF, or REMOTE input is decoded.” AV7100 Preview at 35; see id. at 35-36 (describing additional aspects of the IR/RF remote control interface).</p>
<p>[1j] a storage subsystem connected to said media switch, wherein multimedia data are stored on said storage subsystem and retrieved from said storage subsystem essentially simultaneously.</p>	<p>AV7100 Preview discloses or at least renders obvious a storage subsystem connected to said media switch, wherein multimedia data are stored on said storage subsystem and retrieved from said storage subsystem essentially simultaneously. For example:</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24..” AV7100 Preview at 51-52.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<div> <pre> graph TD     AV7100[AV7100] --- ExternalBus[External Bus]     subgraph AV7100_Internal [AV7100]         DVCRPacketizer[DVCR Packetizer]         LINKInterface[LINK Interface]         PHYInterface[PHY Interface]         ExternalBus --- DVCRPacketizer         ExternalBus --- LINKInterface         LINKInterface --- PHYInterface     end     DVCRPacketizer --- Data[Data] </pre> <p>Figure 19. 1394 Interface</p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“During decoding, the ‘AV7100 allocates the first 16-Mbit SDRAM for NTSC mode, as shown in Figure 3.” AV7100 Preview at 14; see id. fig. 3 (showing memory allocation of 16-Mbit SDRAM).</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> </ul>



'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p>“trick mode decoding</p> <p>When decoding a picture from a digital recorder, the ‘AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame”</li> </ul> <p>AV7100 Preview at 18.</p> <p>“The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder AP Is. Consult the TMS320AV7100 Software Guide for details.” AV7100 Preview at 20; see id. tbl. 8 (showing video decoder commands).</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible</p>

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	<p>services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p> <div> <pre> graph LR     In(( )) --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM     TC --&gt; I1394[1394 Interface]     I1394 --&gt; MUX   </pre> <p>The diagram illustrates the data flow between several components. An input signal enters a MUX (Multiplexer) block. The output of the MUX goes to the TPP (Transponder Processing Port) block. The TPP block is connected to the DES (Data Encryption Standard) block via a bidirectional arrow. The TPP block also has a bidirectional connection to the Traffic Controller block. The Traffic Controller block is connected to the RAM (Random Access Memory) block via a bidirectional arrow. The Traffic Controller block has a bidirectional connection to the 1394 Interface block. The 1394 Interface block has a bidirectional connection to the MUX block.</p> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“During recording, it is assumed that input data originates from the FEC device. An FEC error signal sets the DERROR pin at or before the first byte of input data. This DERROR value is sent to the PERROR output on the 1394 interface coincident with the first valid PDATA. The PERROR value remains active as long as the FEC device keeps DERROR active. Typically, the FEC device retains DERROR until the beginning of the following packet. In this case, the 1394 link device may check for record errors at the first data byte of the packet.</p> <p>During playback mode, an error signal can cause an interrupt only once per packet. For the case of an error between packets, the 1394 link device must ensure that the PERROR of the 'AV7100 is held active until the first byte at PDATA is entered. If an error occurs within a packet, the PERROR pin must complete the transition to</p>

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	<p>high before the last byte of the packet is clocked. PERROR must then be returned low before the first byte of the following good packet.” AV7100 Preview at 54.</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“Fully Functional Decoder Using a Single 16-MBit External Synchronous Dynamic Random-Access Memory (SDRAM)” AV7100 Preview at 1.</p> <p>“The ‘AV7100 provides chip select signals for up to two SDRAMs. The minimum SDRAM size required by the decoder is 16 Mbit. Other supported sizes and configurations are:  16 Mbit --7 one 16 Mbit SDRAM  20 Mbit --7 one 16 Mbit and one 4 Mbit SDRAM  32 Mbit --7 two 16 Mbit SDRAM  The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 20 macroblock. The interface also supports decrement mode for bitBLT block transfer.  The two chip selects correspond to the following address ranges:  SCS1 --7 0xCC00 0000 - 0xCC1 F FFFF  SCS2 --7 0xCC20 0000 - 0xCDFF FFFF” AV7100 Preview at 13.</p> <p>“During decoding, the ‘AV7100 allocates the first 16-Mbit SDRAM for NTSC mode, as shown in Figure 3.” AV7100 Preview at 14; see id. fig. 3 (showing memory allocation of 16-Mbit SDRAM).</p> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for</p>

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	<p>initialization and control of the video decoder. The output video is sent to the 'AV7100 on-screen display (OSD) module for further blending with OSD data." AV7100 Preview at 18.</p> <p>"The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The 'AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization." AV7100 Preview at 30.</p> <p>"extension bus read and write timing The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state." AV7100 Preview at 39.</p> <p><i>See also claim 1 at 1f, supra.</i></p>
Claim 12	
<p>12. The system of claim 1, said output section further comprising a transport interface, wherein said transport interface receives said transport stream from said input section.</p>	<p>AV7100 Preview discloses or at least renders obvious "said output section further comprising a transport interface, wherein said transport interface receives said transport stream from said input section." For example:</p> <p>"Accepts Transport Bit Stream Up to 40-MBits per Second" AV7100 Preview at 1.</p> <p>"The 'AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the 'AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal." AV7100 Preview at 15.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p>“input interface</p> <p>The transport packet data from the FEC device is input to the ‘AV7100 eight bits at a time, using the byte clock, DCLK. A high on PACCLK signals valid packet data. During satellite sourced decode, a DERROR signal is received from the FEC device to indicate that a packet has data errors. The DERROR pin is valid on the first byte or one data byte cycle before the first data byte. It does not change until the following packet.” AV7100 Preview at 16; see also id. at 17 fig. 5 (illustrating input interface timing).</p> <p>“Video Decoder Decodes MPEG-1 (Moving Pictures Experts Group) and MPEG-2 Main Profile and Main Level Bit Stream</p> <ul style="list-style-type: none"> <li>• Audio Decoder Decodes MPEG-1 Layer I and II Bit Stream” AV7100 Preview at 1.</li> </ul> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used</p>

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	<p>for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Supports output data in both PCM and SPDIF formats</li> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p><i>See also</i> claim 1 at 1b, 1d, and 1j, <i>supra</i>.</p>
<b>Claim 13</b>	
13. The system of claim 12, said decoder further comprising a transport stream decoder/graphics subsystem.	<p>AV7100 Preview discloses or at least renders obvious “said decoder further comprising a transport stream decoder/graphics subsystem.” For example:</p> <p><i>See</i> claim 1 at 1b and 1d, <i>supra</i>, and claim 14, <i>infra</i>.</p>
<b>Claim 14</b>	

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<p>14. The system of claim 13, wherein said transport stream decoder/graphics subsystem includes any combination of: a host bridge; a memory controller; an MPEG-2 transport demultiplexer; an MPEG-2 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller.</p>	<p>AV7100 Preview discloses or at least renders obvious “said transport stream decoder/graphics subsystem includes any combination of: a host bridge; a memory controller; an MPEG-2 transport demultiplexer; an MPEG-2 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller.” For example:</p> <p>“On-Chip SDRAM Controller for 16, 20, or 32-MBit SDRAM” AV7100 Preview at 1.</p> <p>“The SDRAM interface supports 16-bit data width SDRAM operating at minimum 81 MHz. The SDRAM selected for use with the ‘AV7100 should meet or exceed the timing requirements in Table 3 for proper operation. The TI TMS626162-12 is one example of a compatible 16 Mbit SDRAM.” AV7100 Preview at 13.</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending them with the video. The OSD module accepts video from the video decoder, reads OSD data from SDRAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces. OSD defaults to standby mode and simply routes video from the video decoder to both outputs. The ARM is responsible for turning on/off OSD operations and for setting specific window attributes of the OSD windows. Dedicated bitBLT hardware attached to the OSD module provides acceleration to memory block moves and graphics operations. OSD data may originate from the user data in the bit stream or may be generated by applications executed on the ARM. Regardless of the source, the OSD data is stored in the SDRAM and managed by the ARM. Memory space in the single 16 Mbits SDRAM is limited to approximately 241 kbytes for OSD, with capability to increase this to approximately 391 kbytes using the half resolution display mode. The OSD data may be represented in one of the following forms: bitmap, graphics 4:4:4 component, 4:2:2 component, or simply background color.” AV7100 Preview at 22; see also id. at 21, 22-24 (describing additional aspects of the OSD module).</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> </ul>

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	<ul style="list-style-type: none"> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware” AV7100 Preview at 15.</li> </ul> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“Video Decoder Decodes MPEG-1 (Moving Pictures Experts Group) and MPEG-2 Main Profile and Main Level Bit Stream</p> <ul style="list-style-type: none"> <li>• Audio Decoder Decodes MPEG-1 Layer I and II Bit Stream” AV7100 Preview at 1.</li> </ul> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> </ul>



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	<ul style="list-style-type: none"> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Supports output data in both PCM and SPDIF formats</li> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p>“extension bus interface The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus. Each CS has its own defined memory space and a programmable wait register. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. . . . The extension bus supports the connection of seven devices using the predefined chip selects. Additional devices may be used by externally decoding the address bus. Table 21 shows the name of the device, its chip select, address range, and programmable wait state. Table 22 and Table 23 show extension bus wait state and configuration registers. Each device on the extension bus is required to have data outputs in high-impedance state within one clock cycle following the removal of chip-select.” AV7100 Preview at 37.</p> <p><i>See claim 1 at 1b and 1d, supra.</i></p>
<b>Claim 15</b>	

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15. The system of claim 14, said transport stream decoder/graphics subsystem further comprising at least one transport stream interface, wherein said transport stream interface receives said transport stream from said input section.	<p>AV7100 Preview discloses or at least renders obvious said transport stream decoder/graphics subsystem further comprising at least one transport stream interface, wherein said transport stream interface receives said transport stream from said input section. For example:</p> <p><i>See claim 1 at 1b and 1d, and claims 12 and 14, supra.</i></p>
Claim 16	
16. The system of claim 14, wherein said transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet streams are stored and played back though [sic] an output side of said transport stream decoder/graphics subsystem.	<p>AV7100 Preview discloses or at least renders obvious “said transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet streams are stored and played back though [sic] an output side of said transport stream decoder/graphics subsystem.” For example:</p> <p>“input interface The transport packet data from the FEC device is input to the ‘AV7100 eight bits at a time, using the byte clock, DCLK. A high on PACCLK signals valid packet data. During satellite sourced decode, a DERROR signal is received from the FEC device to indicate that a packet has data errors. The DERROR pin is valid on the first byte or one data byte cycle before the first data byte. It does not change until the following packet.” AV7100 Preview at 16; <i>see also id.</i> at 17 fig. 5 (illustrating input interface timing); <i>id.</i> at 54.</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> </ul>

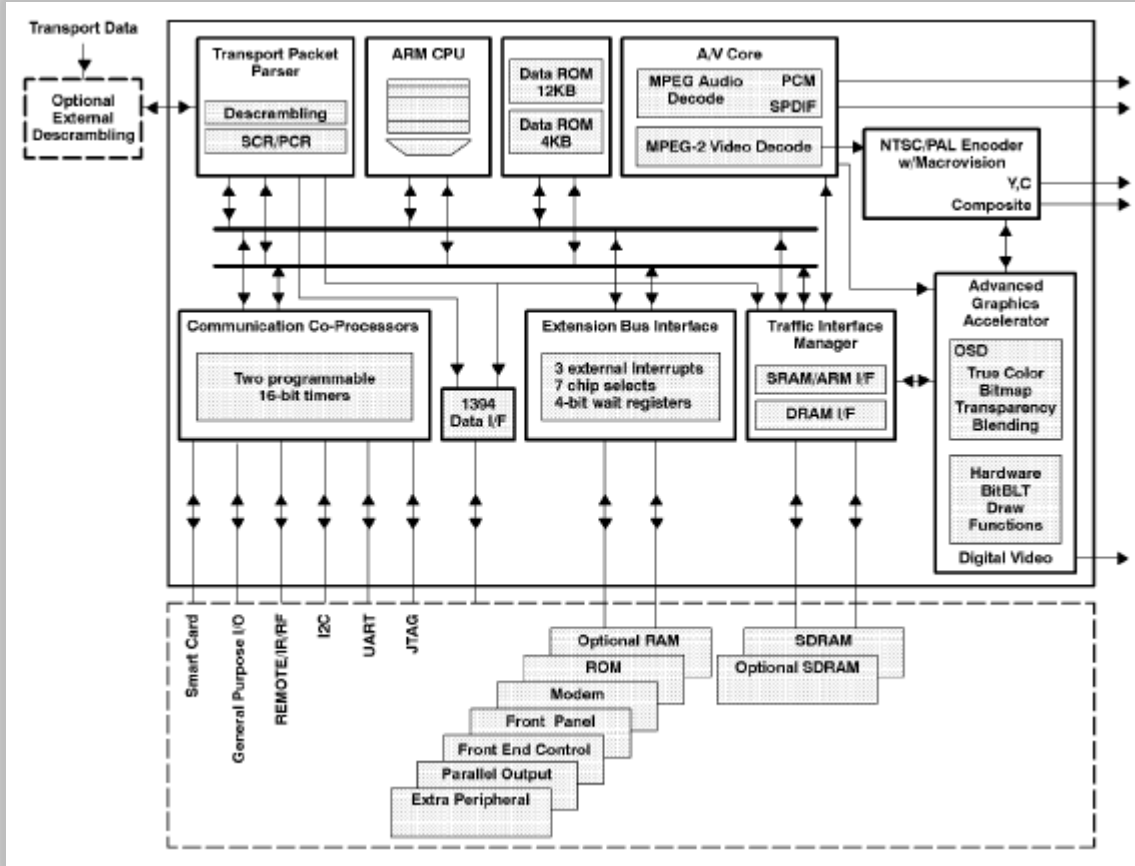
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	<ul style="list-style-type: none"> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware” AV7100 Preview at 15.</li> </ul> <p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF</p>

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	<p>formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p>“Both the video and audio decoders synchronize their presentation using the transmitted PTS. For DSS the PTS is transmitted as picture user data in the video bit stream and as an MPEG-1 system packet bit stream for audio. Dedicated hardware decodes the PTS if it is in the MPEG-1 system packet and forwards it to the audio decoder. The video decoder decodes PTS from picture user data. Both the video and audio decoders compare PTS to the local system clock in order to synchronize presentation of reconstructed data. The local system clock is continuously updated by the ARM.</p> <p>When the PTS and local system clock do not match within tolerance, the video decoder either redisplay or skips a frame. At that time, the CC/EDS is handled as follows:</p> <ul style="list-style-type: none"> <li>• When the video decoder redisplay a frame, the second display does not contain CC/EDS.</li> <li>• When the video decoder skips a frame, the corresponding CC/EDS is also skipped.” AV7100 Preview at 20.</li> </ul> <p>“The video decoder is capable of producing decimated pictures using <math>\frac{1}{2}</math> or <math>\frac{1}{4}</math> decimation per dimension, which results in reduced areas of <math>\frac{1}{4}</math> or <math>\frac{1}{16}</math>, respectively. The decimated picture can be viewed in real time. Decimation is achieved by using field data out of a frame, skipping lines, and performing vertical filtering to smooth the decimated image.” AV7100 Preview at 19.</p> <p><i>See</i> AV7100 Preview at 19 (describing (1) display formats supported by AV7100, (2) aspect ratio conversion supported by the AV7100).</p> <p>“Audio Output in Both Pulse Code Modulation (PCM) and SPDIF Formats On-Screen Display (OSD) Processor Enables Mixture of OSD and Video Data With Transparency” AV7100 Preview at 1.</p> <p>“On-Chip NTSC/PAL Encoder Incorporates Closed Caption and Video Aspect Ratio Identification Signal Encoding and the Macrovision® Logic for Anti-Taping Protection Analog Y, C, and Composite Video Outputs With 9-Bit Precision Internally or Externally Generated Video Synchronization Signals Digital Video Component Output That Also Contains Aspect Ratio Identification Code” AV7100 Preview at 1.</p>

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	<p>“The OSD module is responsible for managing OSD data from different OSD windows and blending them with the video. The OSD module accepts video from the video decoder, reads OSD data from SDRAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces. OSD defaults to standby mode and simply routes video from the video decoder to both outputs. The ARM is responsible for turning on/off OSD operations and for setting specific window attributes of the OSD windows. Dedicated bitBLT hardware attached to the OSD module provides acceleration to memory block moves and graphics operations. OSD data may originate from the user data in the bit stream or may be generated by applications executed on the ARM. Regardless of the source, the OSD data is stored in the SDRAM and managed by the ARM. Memory space in the single 16 Mbits SDRAM is limited to approximately 241 kbytes for OSD, with capability to increase this to approximately 391 kbytes using the half resolution display mode. The OSD data may be represented in one of the following forms: bitmap, graphics 4:4:4 component, 4:2:2 component, or simply background color.” AV7100 Preview at 22; see also id. at 21, 22-24 (describing additional aspects of the OSD module).</p> <p>“The ‘AV7100 provides video output signals encoded for display on a video monitor. The encoded data may include video data or blended video and OSD data. The encoder supports the NTSC format and PAL B, D, G/H and I display formats. The NTSC/PAL pin selects between NTSC and PAL output. Changing between NTSC and PAL requires a hardware reset of the device.</p> <p>The encoder uses 9-bit D/A converters (DACs) to produce an analog S-video signal on separate luminance M and chrominance © channels. An analog composite (Comp) signal is also output. Output signals conform to the RS 170A standard. Application circuits for external connections to the DAG outputs are illustrated in Figure 24. With a single-ended 75 Q load, the output current for peak white is 20 mA.” AV7100 Preview at 26.</p> <p>“The ‘AV7100 also supports various features for video display and control. Closed caption (CC) and Extended Data Services (EDS) information which has been extracted by the video decoder is passed to the ‘AV7100 encoder. The encoder then presents CC data at video line 21 and EDS at video line 284. The video decoder also extracts aspect ratio data from the bit stream and sends it to the ARM, which in turn prepares data according to the video aspect ratio identification signal (VARIS) standard, EIAJ CPX-1204. The ARM forwards VARIS codes to the ‘AV7100 NTSC/PAL module where the codes are inserted onto the 20th video line for NTSC and 23rd line for PAL.” AV7100 Preview at 26.</p> <p>“The ‘AV7100 provides a digital output interface for pure video or blended video and OSD. The digital output includes video in either 4:4:4 or 4:2:2 YCrCb format. VARIS coding for aspect ratio is also provided at the</p>

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	<p>beginning of each video frame. The video output format is programmable by the user, but defaults to 4:2:2. The pin assignments for the digital video output signals are:  8-bit Cb/Y/Cr/Y and VARIS multiplexed data output  27-MHz or 40.5-MHz clock output  YCOUT(8)  YCCLK(1)  YCCTRL(2) 2-bit control signals to distinguish between YCrCb components and VARIS code” AV7100 Preview at 26; see also id. at 26-29 (describing additional aspects of the digital video output interface).</p> <p>“PCM audio output  The 2s complement PCM data is output serially on the PCM OUT pin using the serial clock ASCLK. ASCLK is derived from the PCM clock, PCMCLK, according to the PCMSEL 1 :O bits in the control register. The PCM clock must be the proper multiple of the sampling frequency of the bit stream. The PCMCLK may be input to the device or internally derived from an 36.864-MHz clock. The data on the PCMOUT pin alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7100 Preview at 31; see id. fig. 9 (showing timing for the PCM data).</p> <p>“SPDIF audio output  The SPDIF output conforms to a subset of the AES3 standard for serial transmission of digital audio data. The SPDIF format is a subset of the minimum implementation of AES3.” AV7100 Preview at 31.</p> <p><i>See claim 1 at 1a, 1b, 1d-1j, and claims 12 and 14, supra.</i></p>
Claim 20	
<p>20. The system of claim 14, further comprising a SDRAM connected to said transport stream decoder/graphics subsystem.</p>	<p>AV7100 Preview discloses or at least renders obvious a SDRAM connected to said transport stream decoder/graphics subsystem. For example:</p> <p>“Fully Functional Decoder Using a Single 16-MBit External Synchronous Dynamic Random-Access Memory (SDRAM)” AV7100 Preview at 1.</p>

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	<p>“The ‘AV7100 provides chip select signals for up to two SDRAMs. The minimum SDRAM size required by the decoder is 16 Mbit. Other supported sizes and configurations are:  16 Mbit --7 one 16 Mbit SDRAM  20 Mbit --7 one 16 Mbit and one 4 Mbit SDRAM  32 Mbit --7 two 16 Mbit SDRAM  The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 20 macroblock. The interface also supports decrement mode for bitBLT block transfer.  The two chip selects correspond to the following address ranges:  SCS1 --7 0xCC00 0000 - 0xCC1 F FFFF  SCS2 --7 0xCC20 0000 - 0xCDFF FFFF” AV7100 Preview at 13.</p> <p>“During decoding, the ‘AV7100 allocates the first 16-Mbit SDRAM for NTSC mode, as shown in Figure 3.” AV7100 Preview at 14; <i>see id.</i> fig. 3 (showing memory allocation of 16-Mbit SDRAM).</p> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.” AV7100 Preview at 18.</p> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p>

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	 <p>The diagram illustrates the AV7100 system architecture. It features a central processing core with several key components: a Transport Packet Parser (including Descrambling and SCR/PCR), an ARM CPU, Data ROM (12KB and 4KB), and an A/V Core (including MPEG Audio Decode, PCM, SPDIF, and MPEG-2 Video Decode). This core is connected to a Communication Co-Processors block (with two programmable 16-bit timers), an Extension Bus Interface (with 3 external interrupts, 7 chip selects, and 4-bit wait registers), and a Traffic Interface Manager (with SRAM/ARM I/F and DRAM I/F). The system also includes an NTSC/PAL Encoder w/Macrovision (outputting Y,C and Composite signals) and an Advanced Graphics Accelerator (with OSD, True Color, Bitmap, Transparency, and Blending functions, as well as Hardware BitBLT Draw Functions and Digital Video output). External components are connected via various interfaces: Smart Card, General Purpose I/O, REMOTE I/R/RF, I2C, UART, JTAG, Optional RAM, ROM, Modem, Front Panel, Front End Control, Parallel Output, Extra Peripheral, Optional SDRAM, and SDRAM. The entire system is enclosed in a dashed box representing the main unit.</p> <p>AV7100 Preview at 9 fig. 1.</p> <p>See claim 1 at 1d and 1j, and claim 14, <i>supra</i>.</p>
Claim 22	
22. The system of claim 1, wherein said processor is	AV7100 Preview discloses or at least renders obvious “said processor is operative to run system software, middleware, and application software.” For example:



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operative to run system software, middleware, and application software.	<p>“The ARM is responsible for managing all hardware and software resources in the ‘AV7100. At powerup the ARM verifies the size of external memory. It then initializes all ‘AV7100 hardware modules by setting up control registers and tables and by resetting data pointers. The ARM then executes the default firmware. All firmware is stored in on-chip ROM, except the OSD graphics and some generic run-time support. The run-time support library (RTSL) and all user application software are stored outside the ‘AV7100 in external memory attached to the extension bus. Details of the firmware, RTSL, and application program interface (API) are provided in the companion software document, TMS320AV7100 Software Guide.</p> <p>Based on programmable priority, the ARM responds to interrupt requests generated by internal modules and external devices on the extension bus. Some of the requests are for data transfers to internal RAM, whereas others are true interrupts to the ARM. The 'AV7100s traffic controller handles data transfers, and the ARM provides services to true interrupts. Interrupts are grouped into FIQ and IRQ categories. The system software uses FIQ; the application software uses IRQ. The priorities for FIQs and IRQs are managed by the firmware.” AV7100 Preview at 11.</p> <p>“The ARM initializes and controls the audio decoder via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and oversampling ratio, and choose the output format for dual channel mode. The ARM also reads status information from the audio decoder via a 32-bit status register which provides the MPEG header information and sync, CRC, and PCM status.” AV7100 Preview at 30.</p> <p><i>See</i> AV7100 Preview at 20 tbl. 8 (listing use of OSD API).</p> <p>“The audio module has two registers: a read/write control register and a read-only status register. Both registers are read or written to through user software and 'AV7100 API routines.” AV7100 Preview at 31.</p> <p>“The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder APIs. . . .” AV7100 Preview at 20.</p> <p>“The 'AV7100 includes an interface to the smart card access control system. The interface consists of a high-speed UART and logic to comply with the News Datacom specification (Document #HU-T052, Release E, dated November 1994, and Release F, dated January 1996) ‘DirecTV Project: Decoder-Smart Card Interface Requirements.’ Applicable software drivers that control the interface are also included, and detailed in the companion software document for the 'AV7100.” AV7100 Preview at 33.</p>

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	<p>“The conditional access is triggered by the arrival of a control word packet (CWP). The ARM firmware recognizes that a CWP has been received and passes it to the verifier, which is the user-implemented News Datacom application software running on the ARM. The verifier reads the CWP and communicates with the external smart card through a UART I/O interface. After verification, it passes the pointer to an 8-byte key back to the firmware, which then loads the key for the DES to decrypt succeeding packets.” AV7100 Preview at 33.</p> <p>“To put the device in slave mode the application program must set the slave mode select and a 7-bit address for the 'AV7100. The application must also send a software reset to the 12C to complete the transition to slave mode.” AV7100 Preview at 37.</p> <p>“The initialization software should specify the data size of the device connected to the CS2 to CS6. CS1 and DRAM are always size 16, but CS2 to CS6 (including the parallel data port) can be programmed as a size 8 or size 16 interface. The extension bus interface does the routing between the internal 32-bit data and the 8-bit or 16-bit data on the extension bus. For example, the user program can write a word to an 8-bit device on the extension bus, and the extension bus interface performs four consecutive byte writes.” AV7100 Preview at 43.</p> <p>“device control interfaces reset The 'AV7100 requires a hardware reset on powerup. Reset of the device is initiated by pulling the RESET pin low for at least 100 ns while the clock is running. The following actions will then occur:</p> <ul style="list-style-type: none"> <li>• Input data on all ports is ignored.</li> <li>• External memory is sized.</li> <li>• Data pointers are reset.</li> <li>• All modules are initialized and set to a default state.</li> </ul> <p>TPP tables are initialized. Audio decoder is set for 16 bit output with 256 x oversampling. OSD background color is set to blue and video data is selected for the analog and digital outputs. Macrovision is disabled. The 12C port is set to master mode. When the reset sequence completes, the device will begin to accept data. All data input prior to the end of the reset sequence is ignored.” AV7100 Preview at 55.</p>

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	<p>“Firmware Controls Device Operation and Provides Application Access to Hardware Resources” AV7100 Preview at 1.</p> <p><i>See claim 1 at 1c, supra.</i></p>
Claim 23	
<p>23. The system of claim 22, wherein said system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components.</p>	<p>AV7100 Preview discloses or at least renders obvious said system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components. For example:</p> <p>“The ARM is responsible for managing all hardware and software resources in the ‘AV7100. At powerup the ARM verifies the size of external memory. It then initializes all ‘AV7100 hardware modules by setting up control registers and tables and by resetting data pointers. The ARM then executes the default firmware. All firmware is stored in on-chip ROM, except the OSD graphics and some generic run-time support. The run-time support library (RTSL) and all user application software are stored outside the ‘AV7100 in external memory attached to the extension bus. Details of the firmware, RTSL, and application program interface (API) are provided in the companion software document, TMS320AV7100 Software Guide. Based on programmable priority, the ARM responds to interrupt requests generated by internal modules and external devices on the extension bus. Some of the requests are for data transfers to internal RAM, whereas others are true interrupts to the ARM. The 'AV7100s traffic controller handles data transfers, and the ARM provides services to true interrupts. Interrupts are grouped into FIQ and I RQ categories. The system software uses FIQ; the application software uses IRQ. The priorities for FIQs and IRQs are managed by the firmware.” AV7100 Preview at 11.</p> <p>“The ARM initializes and controls the audio decoder via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and oversampling ratio, and choose the output format for dual channel mode. The ARM also reads status information from the audio decoder via a 32-bit status register which provides the MPEG header information and sync, CRC, and PCM status.” AV7100 Preview at 30.</p> <p><i>See AV7100 Preview at 20 tbl. 8 (listing use of OSD API).</i></p>

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	<p>“The audio module has two registers: a read/write control register and a read-only status register. Both registers are read or written to through user software and 'AV7100 API routines.” AV7100 Preview at 31.</p> <p>“The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder APIs. . . .</p> <p>The half resolution display mode stores and displays only one field of B frame. The same field is displayed twice for the interlaced frame. The same field is repeatedly displayed during the 3:2 pulldown case. The user controls this mode via software using the video decoder commands HalfResOn and HalfResOff.” AV7100 Preview at 20.</p> <p>“The 'AV7100 includes an interface to the smart card access control system. The interface consists of a high-speed UART and logic to comply with the News Datacom specification (Document #HU-T052, Release E, dated November 1994, and Release F, dated January 1996) ‘DirecTV Project: Decoder-Smart Card Interface Requirements.’ Applicable software drivers that control the interface are also included, and detailed in the companion software document for the 'AV7100.” AV7100 Preview at 33.</p> <p>“The conditional access is triggered by the arrival of a control word packet (CWP). The ARM firmware recognizes that a CWP has been received and passes it to the verifier, which is the user-implemented News Datacom application software running on the ARM. The verifier reads the CWP and communicates with the external smart card through a UART 1/0 interface. After verification, it passes the pointer to an 8-byte key back to the firmware, which then loads the key for the DES to decrypt succeeding packets.” AV7100 Preview at 33.</p> <p>“To put the device in slave mode the application program must set the slave mode select and a 7-bit address for the 'AV7100. The application must also send a software reset to the 12C to complete the transition to slave mode.” AV7100 Preview at 37.</p> <p>“The initialization software should specify the data size of the device connected to the CS2 to CS6. CS1 and DRAM are always size 16, but CS2 to CS6 (including the parallel data port) can be programmed as a size 8 or size 16 interface. The extension bus interface does the routing between the internal 32-bit data and the 8-bit or 16-bit data on the extension bus. For example, the user program can write a word to an 8-bit device on the extension bus, and the extension bus interface performs four consecutive byte writes.” AV7100 Preview at 43.</p> <p>“device control interfaces reset</p>

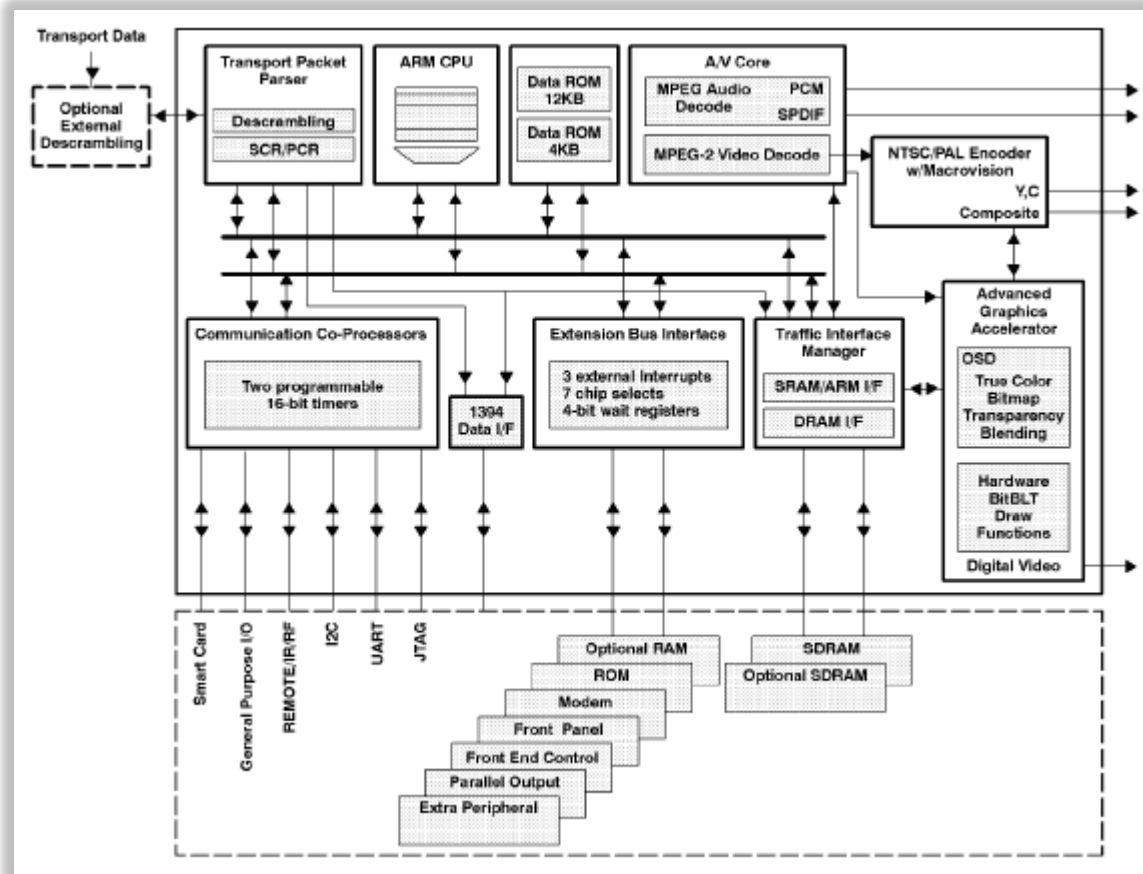
'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>The 'AV7100 requires a hardware reset on powerup. Reset of the device is initiated by pulling the RESET pin low for at least 100 ns while the clock is running. The following actions will then occur:</p> <ul style="list-style-type: none"> <li>• Input data on all ports is ignored.</li> <li>• External memory is sized.</li> <li>• Data pointers are reset.</li> <li>• All modules are initialized and set to a default state.</li> </ul> <p>TPP tables are initialized.  Audio decoder is set for 16 bit output with 256 x oversampling.  OSD background color is set to blue and video data is selected for the analog and digital outputs.  Macrovision is disabled.  The 12C port is set to master mode.  When the reset sequence completes, the device will begin to accept data. All data input prior to the end of the reset sequence is ignored.” AV7100 Preview at 55.</p> <p><i>See claim 1 at 1c and claim 22, supra.</i></p>
Claim 30	
<p>30. The system of claim 1, further comprising a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in said media manager.</p>	<p>AV7100 Preview discloses or at least renders obvious a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in said media manager. For example:</p> <p>“extension bus interface  The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus. Each CS has its own defined memory space and a programmable wait register. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space.” AV7100 Preview at 37.</p>

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	<div><p><b>Table 21. Extension Bus Chip Selects</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 MBytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 32 MBytes)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7100 Preview at 37 tbl. 21.</p> <p><i>See also claim 1 at 1e, supra.</i></p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)	N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
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CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device																														
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device																														
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port																														
Claim 32																																	
32. The system of claim 1, wherein said second bus element comprises a system bus.	<p>AV7100 Preview discloses or at least renders obvious said second bus element comprises a system bus. For example:</p> <p>“extension bus interface</p> <p>The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus. Each CS has its own defined memory space and a programmable wait register. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. . . .</p> <p>The extension bus supports the connection of seven devices using the predefined chip selects. Additional devices may be used by externally decoding the address bus. Table 21 shows the name of the device, its chip select, address range, and programmable wait state. Table 22 and Table 23 show extension bus wait state and</p>																																

'472 Patent Claim	Exemplary Prior Art Disclosure																																
	<p>configuration registers. Each device on the extension bus is required to have data outputs in high-impedance state within one clock cycle following the removal of chip-select.” AV7100 Preview at 37.</p> <div><p><b>Table 21. Extension Bus Chip Selects</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 MBytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 32 MBytes)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7100 Preview at 37 tbl. 21.</p> <p>“extension bus read and write timing</p> <p>The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. The number of wait states can be calculated by the following formula:</p> <p style="padding-left: 40px;">Number of wait states= round_up[(((Device_cycle_time + 8 ns)/24.68 ns)]</p> <p>For example, a 100 ns EEPROM requires five wait states.</p> <p>Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)	N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
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## '472 Patent Claim

## Exemplary Prior Art Disclosure



AV7100 Preview at 9 fig. 1.

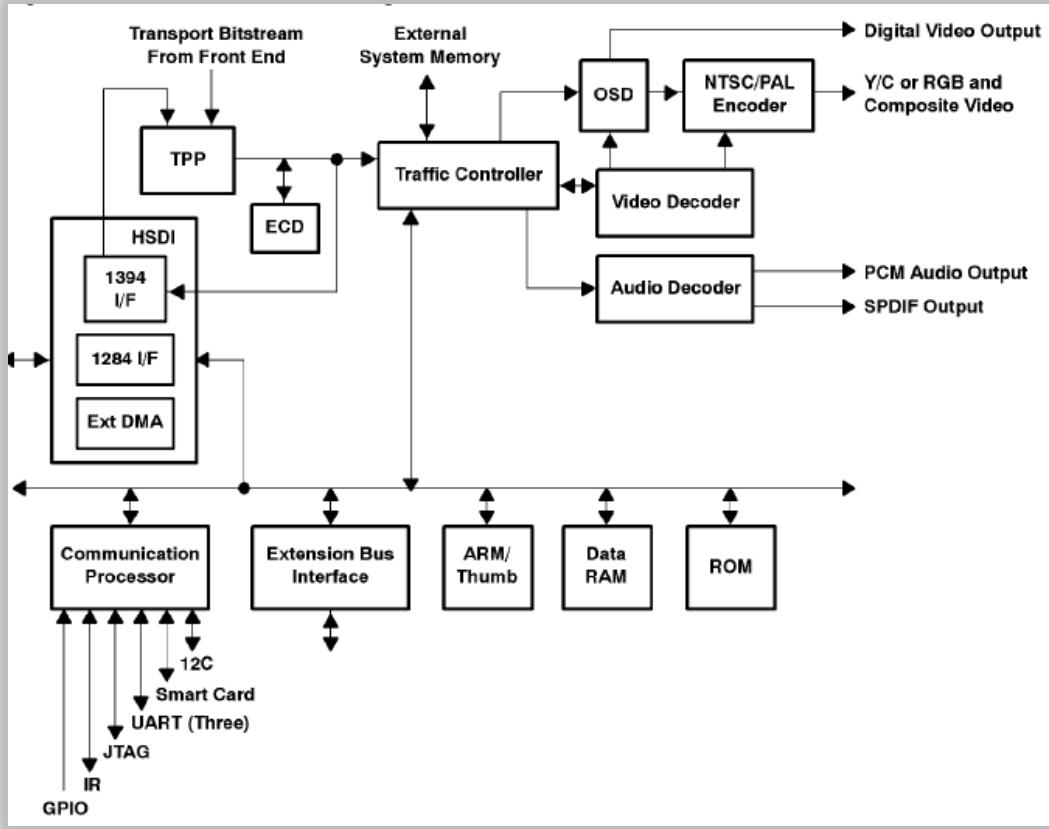
See claim 1 at 1d, 1e, and 1f, *supra*.



**Invalidity Contentions for U.S. Patent No. 7,558,472****Based on “Product Preview: TMS320AV7110 Integrated Digital Set-top Box Decoder” (“AV7110 Preview”)**

Based upon TiVo’s Complaint, Infringement Contentions, and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered, the reference charted below anticipates or at least renders obvious the asserted claims. These invalidity contentions are not an admission by Samsung that the accused products are covered by, or infringe the asserted claims, particularly when these claims are properly construed and applied. These invalidity contentions are not an admission that Samsung concedes or acquiesces to any claim construction implied or suggested by TiVo’s Complaint or Infringement Contentions. Nor is Samsung asserting any claim construction positions through these charts, including whether the preamble is a limitation. The portions of the prior art reference cited below are not exhaustive but are exemplary in nature.

<b>’472 Patent Claim</b>	<b>Exemplary Prior Art Disclosure</b>
<b>Claim 1</b>	
[1p] A system for the simultaneous storage and playback of multimedia data, comprising:	<p>To the extent that the preamble is limiting, the AV7110 Preview discloses or at least renders obvious a system for the simultaneous storage and playback of multimedia data. For example:</p> <p>“The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO), and MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infra-red (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.” AV7110 Preview at 1.</p>

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	 <p>The diagram illustrates the AV7110 system architecture. A 'Transport Bitstream From Front End' enters a 'TPP' (Transport Processing Processor) block. The TPP is connected to an 'HSDI' (High-Speed Data Interface) block, which contains '1394 I/F', '1284 I/F', and 'Ext DMA' components. The HSDI is connected to a 'Traffic Controller' block. The Traffic Controller is also connected to 'External System Memory' and an 'OSD' (On-Screen Display) block. The Traffic Controller outputs to a 'Video Decoder' and an 'Audio Decoder'. The Video Decoder outputs to the OSD, which then feeds into an 'NTSC/PAL Encoder'. The NTSC/PAL Encoder produces 'Digital Video Output' and 'Y/C or RGB and Composite Video'. The Audio Decoder produces 'PCM Audio Output' and 'SPDIF Output'. The system also includes a 'Communication Processor' connected to various interfaces: 'GPIO', 'IR', 'JTAG', 'UART (Three)', 'Smart Card', and '12C'. The Communication Processor is connected to an 'Extension Bus Interface', which in turn connects to 'ARM/Thumb', 'Data RAM', and 'ROM' blocks. Bidirectional arrows indicate data flow between the Traffic Controller, External System Memory, Video Decoder, Audio Decoder, and the bus components.</p> <p>AV7110 Preview at 12 fig. 1.</p> <p>“After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards.” AV7110 Preview at 13.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible</p>

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	<p>to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PIO table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.</p> <p>The only difference between the two scenarios is that in the case where there is no TPP traffic, the TPP buffer pool can be used. In the case where there is active TPP data, a general purpose buffer needs to be used. Additionally, when TPP data traffic is active, the end of packet (EOP) interrupt generation will require an indication data type configured in the header, which describes where the data to be processed is to be found.” AV7110 Preview at 21.</p> <p>“trick mode</p> <p>When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error</li> <li>• Continuously displays the decoded I frame.” AV7110 Preview at 26; <i>see id.</i> tbl. 6 (showing video decoder commands enabling trick mode functionality).</li> </ul> <p>“The HSDI supports the following concurrent data transfers.</p> <ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/program to 1394 (using dedicated I/F - see NOTE XXXX of Table 29)</li> <li>• TPP/program to decoder; 1394/OMA to/from memory</li> </ul>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• TPP/program to decoder; memory/DMA to/from HSDI</li> <li>• TPP/program to decoder; TPP/DMA to HSDI</li> <li>• TPP/program to decoder; TPP/program to 1394; memory/DMA to/from 1394</li> <li>• TPP/program to decoder; 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; TPP/DMA to 1394” AV7110 Preview at 61.</li> </ul> <p>AV7110 Preview at 61 (showing the functional blocks of the HSDI); <i>see also id.</i> at 62-65 (showing describing AV7110's reading and writing of data from/to the 1394 interface).</p> <p>“AV7110 internal data path for 1394</p> <p>In recording mode, the 'AV7110 sends either encrypted or clean packets to the 1394 interface. The packet will be transferred as soon as it arrives. When recording encrypted data, the ECO module is bypassed. In the case of recording decrypted byte, the TPP sends the encrypted part of the payload to the ECD module, and then forwards each byte to the 1394 interface. No CPU processing is done to the packet during recording. The TPP automatically modifies the header if the packet is decrypted.</p> <p>Note that the same team cannot be sent to the 1394 interface twice (such as, once after decryption, and twice as part of a full transport stream with the by-pass capability). Both Timon and the 'AV7110 support only one MPEG-2 transport stream channel on the bulky data interface.</p> <p>During playback mode, MPEG-2 transport packets coming from the 1394 interface go directly to the TPP module.</p> <p>Figure 29 shows the functional block diagram of the data flow between the TPP, ECD, and 1394 interface. Note that the major portion of the 1394 interface function is implemented in the HSDI module. Dedicated data lines are used for the 1394 interface that allows the 'AV7110 to work in different modes.</p> <ul style="list-style-type: none"> <li>• Decode/decrypt/display one channel and record it</li> <li>• Decode/decrypt/display one channel and record it encrypted (pay-per-view)</li> <li>• Decode/display one channel while recording all or part of 32 PIDs from a transponder, with each selected PIDs either encrypted or decrypted. In addition non selected PIDs can also be recorded in their original format (decryption is not possible for non selected PIDs).</li> <li>• While the TPP is receiving MPEG-2 data from the 1394 port, the 'AV7110 can also record part of the bit stream it is receiving to the 1394 port</li> </ul>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Send the whole transport stream from the FEC to the 1394 port without any filtering or decryption and, at the same time, decode/decrypt/display a program from either the same transport stream or from another transport stream received through the 1394 port..” AV7110 Preview at 65.</li> </ul> <p>AV7110 Preview at 65 fig. 29 (showing functional block diagram of data flow between TPP, ECD, and 1394 interface).</p> <p>“When configured for EDMA operation (HSDI_ STATUS[1 LO] = 01), the HSDI is capable of a glue less connection to an external enhanced SCSI controller (ESC) device such as the NCR 53CF94-1 /53CF96-1. Figure 30 shows the connections for this example configuration.</p> <p>....</p> <p>Since there is only an 8-bit bus on the HSDI, the ESC is limited to an 8-bit, single bus architecture so its mode selection inputs should be set to mode 0. The upper data bits can be left floating since they have internal pullups on the ESC. Likewise, the AD?-0 inputs of the ESC will not be used for this mode and can be left unconnected. The ESC requires an external clock source from 10 MHz to 40 MHz. Since the CLK40 signal of the 'AV7110 is actually a 40.5 MHz clock it cannot be used directly for this controller without violating its specification. Table 32 shows the signals needed for the EDMA interface.</p> <p>....</p> <p>All data transfers (using the HSDI DMA unit) as well as external controller communications (using the A[3:0] output signals), are controlled by the firmware. Firmware will handle MPEG-2 program stream and MPEG-1 system stream input. This firmware will not be available with the initial samples of the 'AV7110. The other input data formats will be handled by user application software. This includes specific interfaces such as the ESC. Table 33 details the EDMA register which allows the user to configure the wait states and other factors of the EDMA port.” AV7110 Preview at 66-67.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p style="text-align: center;">Figure 26. 1394 Interface</p> </div> <p>AV7110 Preview at 62 fig. 26 (showing connection between AV7110 and external packetizer, link layer controller, and physical layer device); <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) packets to and from the internal data RAM. This data can then be processed by the user software as needed.”).</p> <p>“The application software interfaces with the peripheral interface controller via RTSL API calls. To send data to the host the application software will issue an API call to transfer the data from memory to the peripheral interface via a DMA. To receive data from the host, the application software will issue an API to transfer a predetermined number of bytes from the peripheral interface to internal data memory via the HSDI DMA unit. The user application software must have a way to determine the number of bytes of data that is expected from the host.” AV7110 Preview at 70.</p> <p><i>See claim 1 at 1j, infra.</i></p>

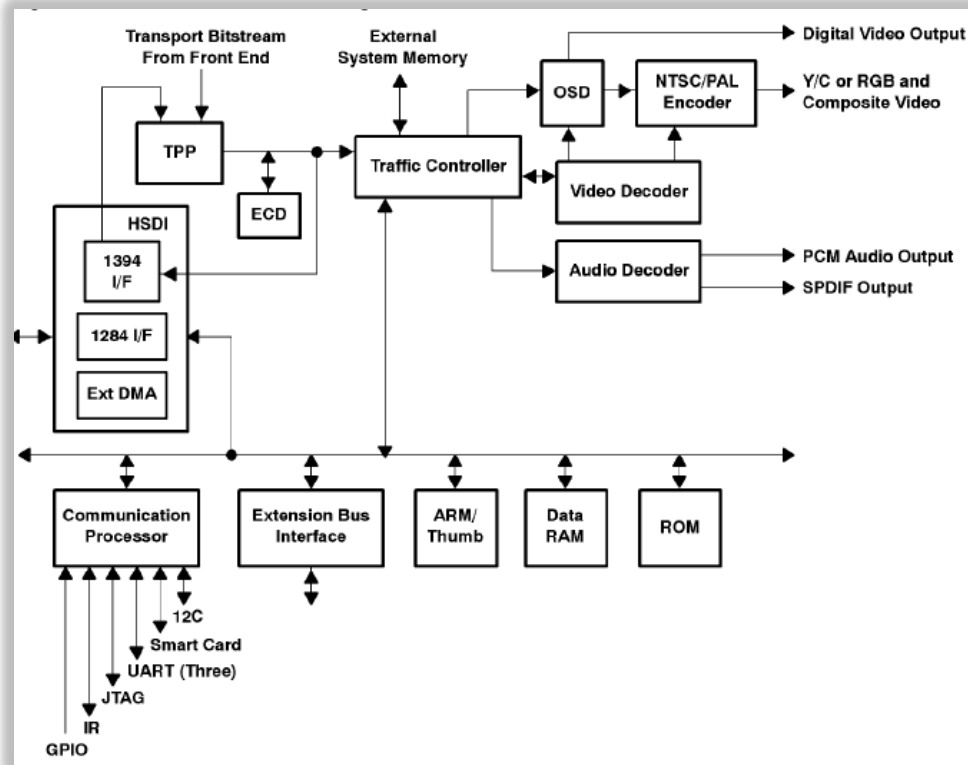
'472 Patent Claim	Exemplary Prior Art Disclosure
[1a] an input section for acquiring an input signal;	<p>AV7110 Preview discloses or at least renders obvious an input section for acquiring an input signal. For example:</p> <p>“The ‘AV7110 accepts a DVB transport bit-stream from the output of a Forward Error Correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet).” AV7110 Preview at 13.</p> <p>“The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO), and MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infra-red (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.” AV7110 Preview at 1.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PIO table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.” AV7110 Preview at 21.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>“transport parser input interface  The ‘AV7110 accepts DVB transport packet data from a front end such as a Forward Error Correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB Conditional Access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23; <i>see also id.</i> at 24 tbl. 4 (describing transport packet input interface pin description).</p> <div> </div> <p>AV7110 Preview at 12 fig. 1.</p>
[1b] an output section, wherein said input signal is passed to said output section as a	AV7110 Preview discloses or at least renders obvious an output section, wherein said input signal is passed to said output section as a transport stream. For example:



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transport stream; said output section including:

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AV7110 Preview at 12 fig. 1.

“The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.” AV7110 Preview at 13.

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	<p>“The TPP hardware is capable of detecting packets lost from the transport stream. With error concealment by the audio and the video decoders the ‘AV7110 minimizes the effect of lost data.” AV7110 Preview at 13.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PIO table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.” AV7110 Preview at 21.</p> <p>“MPEG transport decoder (TPP) TPP module features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps Maximum input bit rate through the 1394 interface ..... 64.8 Mbps Maximum video bit rate ..... 15 Mbps Maximum audio bit rate ..... 1.13 Mbps</p>

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	<p>Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec</p> <p>Maximum number of PIDs that can be filtered ..... 32</p> <p>Maximum number of PIDs that can be descrambled ..... 32</p> <p>Maximum number of pairs of keys for the descrambler ..... 16</p> <p>Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination. The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“transport parser input interface</p>

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	<p>The 'AV7110 accepts DVB transport packet data from a front end such as a Forward Error Correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB Conditional Access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23; <i>see also id.</i> at 24 tbl. 4 (describing transport packet input interface pin description).</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SDRAM, and produces three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs. After being configured and activated by the ARM CPU, the OSD module reads OSD data and mixes it with the video output. The CPU is responsible for turning on and off OSD operations. The bitBLT hardware which is attached to the OSD module provides acceleration for memory block moves and graphics operations.” AV7110 Preview at 33.</p> <div> <pre> graph LR     OSDData[OSD Data] --&gt; FIFO[FIFO]     FIFO --&gt; OSL1[OSD Component Latch]     VideoDecoder[Video Decoder] --&gt; OSL2[OSD Component Latch]     OSL1 --&gt; CLUT[CLUT and Window Attributes]     OSL2 --&gt; CLUT     CLUT --&gt; OCS[Output Channel Selection]     CLUT --&gt; Blending[Blending]     XPos[X Position] --&gt; WinSel[Window Selection]     YPos[Y Position] --&gt; WinSel     WinSel --&gt; DisplayCtrl[Display Control]     DisplayCtrl --&gt; OCS     DisplayCtrl --&gt; Blending     OCS -- Ch0 --&gt; AnalogCVBS[Analog CVBS]     OCS -- Ch2 --&gt; AnalogRGB[Analog RGB]     OCS -- Ch1 --&gt; DigitalYC[Digital Y/C]     Blending --&gt; OCS     Blending --&gt; DisplayCtrl </pre> </div> <p>AV7110 Preview at 33 fig. 8 (showing block diagram of the OSD module).</p>

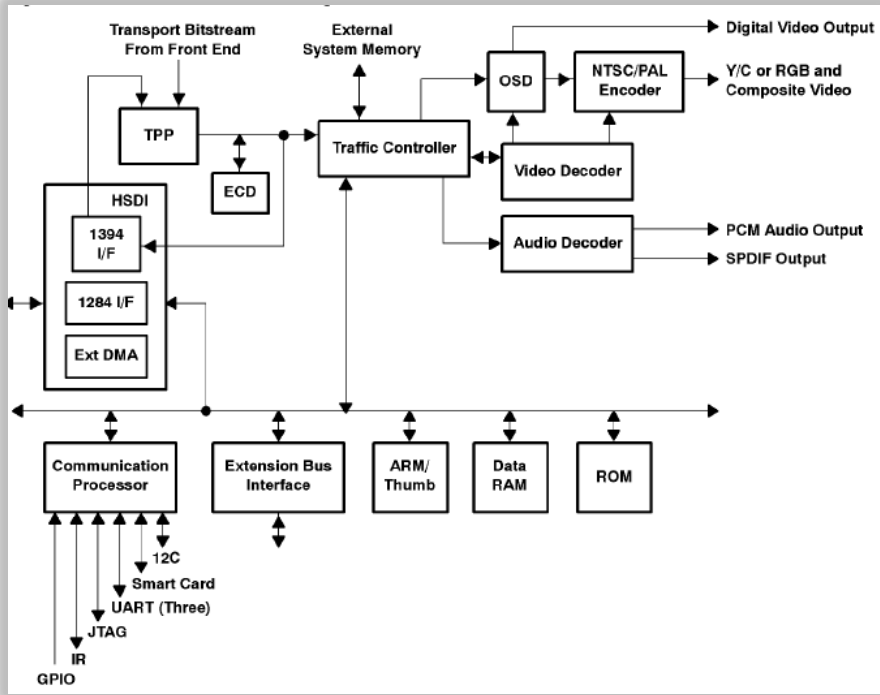
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	<div> </div> <p>AV7110 Preview at 36 fig. 9.</p> <p>“video output interfaces</p> <p>analog video output - NTSC/PAL encoder module</p> <ul style="list-style-type: none"> <li>• Supports NTSC and PAL B, D, G/H, and I display formats</li> <li>• Outputs Y/C or RGB, and composite video with 9-bit DACs</li> <li>• Generates 100/75 format color bar for PAL mode testing</li> <li>• Complies to the RS170A standard</li> <li>• Composite and RGB signals comply with ITU-R BT.470-3 and ITUR BT.471-1</li> <li>• Supports Macro Vision anti-taping function on composite video</li> <li>• Provides sync signals with option to accept external sync signals</li> </ul> <p>The composite video output can be either PAL or NTSC format. The default output format is PAL at powerup. Changing between NTSC and PAL mode can be done via an API which selects the output mode of the NTSC/PAL encoder. Note that the video decoder microcode ROM is specific to NTSC or PAL and required for proper operation.</p> <p>The sync signal pins Vsync and Hsync on the 'AV7110 are defaulted to 3-state mode at powerup, where internally generated sync signals will be used by the NTSC/PAL encoder. The user can then select the source of video sync signals via an API. If internal source is selected then the Vsync and Hsync pins will be configured as output pins. In addition to composite video, the 'AV7110 also provides either an analog S-video (Y - luminance , C - chrominance) signal or an analog RGB output with 720 pixel resolution. All outputs conform to the RS170A</p>

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	<p>standard. Selection of RGB or S-video output is done via API software. Macro Vision version 7 is enabled via an API; the default state is off. A version of the 'AV7110 where the MacroVision anti-taping circuitry is permanently disabled is also available.” AV7110 Preview at 39.</p> <p>“digital video output (not supported when 32-bit EBI is used)</p> <p>PAL mode digital video output</p> <p>The digital output is in 4:2:2 component format. The content of the video could be either pure video or the blended combination of video and OSD. The pin assignments for the digital video output signals are:</p> <p style="padding-left: 40px;">YCOUT(8) 8-bit Cb/Y/Cr/Y data output</p> <p style="padding-left: 40px;">YCCLK(1) 27 MHz clock output</p> <p>The timing of 4:2:2 digital video output is shown in Figure 12.</p> <p>...</p> <p>NTSC mode digital video output</p> <p>The digital output includes video in either 4:4:4 or 4:2:2 component format, plus the aspect ratio VARIS code at the beginning of each video frame. The video output format is programmable by the user but defaults to 4:2:2. The content of the video could be either pure video or the blended combination of video and OSD.</p> <p>The pin assignments for the digital video output signals are:</p> <p style="padding-left: 40px;">YCOUT(8) 8-bit Cb/Y/Cr/Y and VARIS multiplexed data output</p> <p style="padding-left: 40px;">YCCLK(1) 27 MHz clock output</p> <p style="padding-left: 40px;">YCCTRL(2) 2-bit control signals to distinguish between Y/Cb/Cr components and VARIS code</p> <p>The interpretation of YCCTRL is defined in Table 20. . . .” AV7110 Preview at 41.</p> <p>“PCM audio output</p> <p>The PCM audio output from the 'AV7110 is a serial PCM data line, with associated bit clock (ASCLK) and left/right clock (LRCLK). PCM data is output serially on PCM OUT using the serial clock ASCLK as shown in Figure 15. The data output of PCM OUT alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7110 Preview at 46; <i>see generally id.</i> at 46-47 (describing additional aspects of PCM audio output).</p> <p>“elementary stream playback</p> <p>In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing</p>

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	<p>off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.</p> <p>SPDIF audio output The SPDIF output conforms to the consumer format of the AES3 standard for serial transmission of digital audio data. When using an external PLL (PCMSRC=1), SPDIF is supported only if Bx over-sampled PCMCLK is supplied (that is, PCMSEL[0]=1).” AV7110 Preview at 48.</p> <p><i>See generally</i> AV7110 Preview at 32-38 (describing OSD and graphics acceleration); <i>id.</i> at 41-43 (describing different aspects of digital video output).</p> <p><i>See</i> claim 1 at 1c-1j, <i>infra</i>.</p>
[1c] a processor;	<p>AV7110 Preview discloses or at least renders obvious a processor. For example:</p> <p>AV7110 Preview at 1 (listing a “32/16 Bit ARM/Thumb Processor” as one of the components present in the TMS320AV7110 decoder chip).</p> <p>“ARM CPU features</p> <ul style="list-style-type: none"> <li>• Runs at 40.5 MHz</li> <li>• Supports byte (8-bit), half-word (16-bit), and word (32-bit) data types</li> <li>• Reads instructions from on-chip ROM or from the extension bus</li> <li>• Can switch between ARM (32-bit) or Thumb (16-bit) instruction mode</li> <li>• 32-bit data and 32-bit address lines</li> <li>• 7 processing modes</li> <li>• Two interrupts, FIQ and I RO</li> </ul> <p>The 32-bit ARM processor running at 40.5 MHz and its associated firmware provide the following:</p> <ul style="list-style-type: none"> <li>• Initialization and management of all hardware modules</li> <li>• Service for selected interrupt generated by hardware modules and I/O ports</li> <li>• Application program interface (API) for users to develop their own applications”</li> </ul> <p>AV7110 Preview at 15.</p>

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	<p>“The CPU in the 'AV7110 is a 32-bit RISC processor, the ARM7TDM I/Thumb, which has the capability to execute instructions in 16- or 32-bit format at a clock frequency of 40.5 MHz. The regular ARM instructions are exactly one word (32-bit) long, and the data operations are only performed on word quantities. The LOAD and STORE instructions however, can transfer either byte, half-word or word quantities.</p> <p>The Thumb uses the same 32-bit architecture with an 16-bit instruction set. That is, it retains the 32-bit performance but reduces the code size with 16-bit instructions. With 16-bit instruction, the Thumb still gives 70-80% of the performance of the ARM when running ARM instructions from 32-bit memory.” AV7110 Preview at 15; <i>see also id.</i> (stating that ARM and Thumb are used interchangeably in the AV7110 Preview’s disclosure).</p> <p>“ARM uses a LOAD and STORE architecture, that is, all operations are on the registers. ARM has 7 different processing modes with 16, 32-bit registers visible in user mode. In the Thumb state, there are only 8 registers available in user mode. The high registers may still be accessed through special instructions in this case. The instruction pipeline is three stage, fetch ~ decode ~ execute, and most instructions only take one cycle to execute. Figure 3 shows the data path of ARM processor core.” AV7110 Preview at 16.</p> <div> <pre> graph LR     RB[Register Bank] -- B-Bus --&gt; BS[Barrel Shifter]     BS --&gt; ALU[ALU]     RB -- A-Bus --&gt; ALU     BM[Booth Multiplier] --&gt; ALU     ALU -- ALU-Bus --&gt; RB </pre> <p><b>Figure 3. ARM Core Data Path</b></p> </div> <p>AV7110 Preview at 16 fig. 3 (figure showing data path of the ARM Core); <i>see id.</i> (describing ARM CPU’s performance of hardware and software resource management).</p>



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<p>[1d] a decoder subsystem that decodes said transport stream, said decoder subsystem connected to said processor by a first data bus; and</p>	<p>AV7110 Preview discloses or at least renders obvious a decoder subsystem that decodes said transport stream, said decoder subsystem connected to said processor by a first data bus. For example:</p>  <p>AV7110 Preview at 12 fig. 1.</p> <p>“After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards. The chip decodes MPEG-1 and MPEG-2 main profile at main level for video and Layer I and II MPEG-1 and MPEG-2 stereo for audio. Both video and audio decoders synchronize their presentation of reconstructed data using the transmitted presentation time stamps (PTS) and their local system clock. The local system clock is continuously updated by the ARM.” AV7110 Preview at 13.</p> <p>“video decoder</p>

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	<p>features</p> <ul style="list-style-type: none"> <li>• Real-time decoding of MPEG-2 Main Profile@Main level and MPEG-1 video bit-streams</li> <li>• Error detection and concealment</li> <li>• Internal 90 kHz/27 MHz system time clock</li> <li>• Sustained input rate of 15 Mbps</li> <li>• Supports trick mode with full size trick mode picture</li> <li>• Provides 1/4 and 1/16 decimated size picture</li> <li>• Extracts closed caption and other picture user data from the bit-stream</li> <li>• 3:2 pulldown in NTSC mode</li> <li>• Provides read access to video input buffer's read/write pointers</li> <li>• Pan-and-scan for 16:9 and 20:9 source material according to MPEG syntax</li> <li>• Letterbox support</li> <li>• High level command interface</li> <li>• Synchronization using presentation time stamps (PTS); also supports VBV delay based and free run (no synchronization) video playback</li> <li>• Supports the following display format with polyphase horizontal resampling and vertical chrominance filtering.” AV7110 at 25.</li> </ul> <p>“The video decoder module receives a video bit-stream from the SDRAM. It also uses the SDRAM as its working memory to store tables, buffers, and reconstructed images. The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.</p> <p>The 'AV7110 synchronizes the presentation of video with the audio using the transmitted PTS which are extracted by the ARM from the PES packets. it compares the PTS with the local system time clock (STC) and performs synchronization recovery if the difference is outside of a user programmable threshold range given as follows:</p> $\text{STC} - \text{threshold} < \text{PTS} < \text{STC} + \text{threshold}$ <p>If synchronization recovery is needed, the video decoder will either redisplay or skip a frame, depending on the PTS value. If the PTS lags, that is, the time for displaying the current picture has already passed, the video decoder discards the following B pictures without decoding them until the PTS catches up with the STC. If the PTS leads, that is, the time for displaying the current picture has not arrived yet, the video decoder pauses the decoding and continuously displays the last picture (see Synchronization for more details).” AV7110 Product Preview at 25-26.</p>

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	<p>“trick mode</p> <p>When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error</li> <li>• Continuously displays the decoded I frame.” AV7110 Preview at 26; <i>see id.</i> tbl. 6 (showing video decoder commands enabling trick mode functionality).</li> </ul> <p>“The video decoder contains a polyphase filter and a vertical interpolation filter for performing horizontal resampling and luma/chroma vertical interpolation to support decimation and scaling of pictures. In operation, the firmware first loads picture data from the video storage space in the SDRAM to the internal buffer of the video decoder.” AV7110 Preview at 27; <i>see id.</i> (describing additional aspects).</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers I and II</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Outputs in both PCM and SPDIF formats</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information</li> <li>• Supports half-frequency modes</li> <li>• Supports playback of 16-bit PCM data (PCM bypass), audio elementary stream, and audio PES</li> <li>• Provides read/write accesses to audio input buffers read/write pointers</li> </ul> <p>The audio module receives MPEG compressed audio data from the TC, decodes it, and outputs audio samples in PCM format. APIs are provided for the ARM CPU to initialize/control the audio decoder via a control register and to read status information from the decoder's status register.</p>

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	<p>Audio frame data and PTS information are stored in the SDRAM in packet form. The audio module decodes the packets to extract the PTS and audio data. The audio decoder uses this PTS value to perform playback synchronization (see Synchronization for more details). It is application software's responsibility to determine and enable the PIO of the MPEG-1 compliant bit-stream in a MPEG-2 audio program which contains both the MPEG-1 compliant bit-stream and the MPEG-2 extension bit-stream.</p> <p>The ARM can control the operation of the audio module via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and over-sampling ratio, and choose the output format for dual channel mode. The ARM will also be able to read status information from the audio module. One 32-bit register provides the MPEG header information and sync, CRC, and PCM status.” AV7110 Preview at 44; <i>see also id.</i> at 45-46 (listing registers used by the audio module).</p> <p>“MPEG transport decoder (TPP)  TPP module  features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15  Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32  Maximum number of pairs of keys for the descrambler ..... 16  Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul>

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	<p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination. The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“transport parser input interface</p> <p>The 'AV7110 accepts DVB transport packet data from a front end such as a Forward Error Correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB Conditional Access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23; <i>see also id.</i> at 24 tbl. 4 (describing transport packet input interface pin description).</p> <p>“The 'AV7110 uses the STC and PTS to determine the play back time of the decoded audio and video data. The relationship between STC and PTS is determined at the time of the generation of the generation of the respective elementary streams (ES). Upon reception, the demultiplexing software in the 'AV7110 extracts the</p>

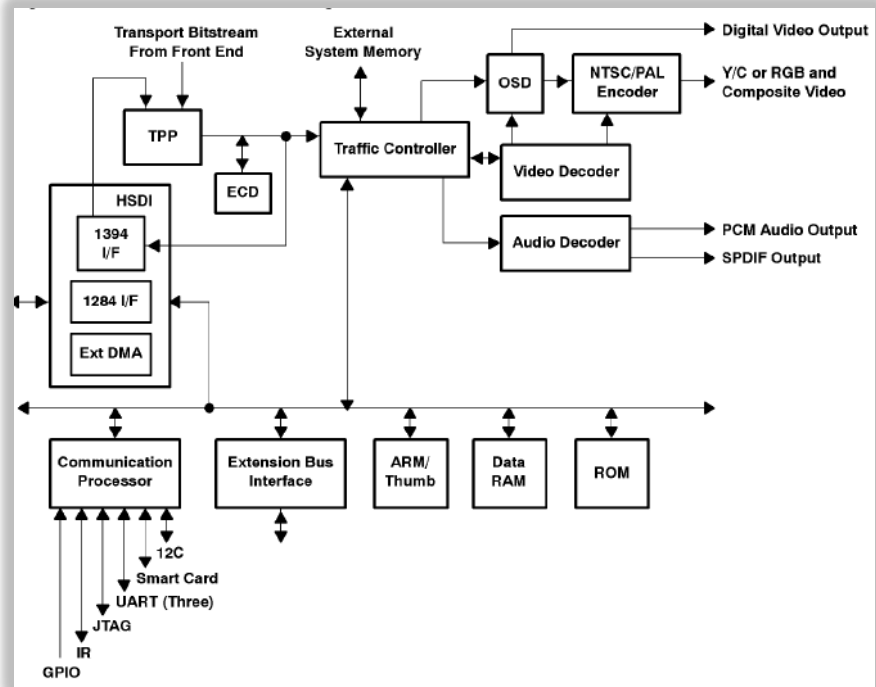
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	<p>video PTS and inserts it in an array of PTS and byte-count information maintained for the video decoder. For the audio the PTS information is extracted by the audio decoder front end from the PES. The video decoder contains an STC counter that is clocked by the system clock (27 MHz) and normalized to a 90 kHz reference. The audio decoder does not contain a counter. Instead, it gets updated from the system time reference counter every 1 .4 ms.” AV7110 Preview at 48.</p> <p>“elementary stream playback In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.” AV7110 Preview at 48.</p> <p>“extension bus interface (EBI) The extension bus interface is a 32-bit or 16-bit bidirectional data bus with a 25-bit address. It also provides 3 external interrupts and a wait line. All the external memories or I/O devices are mapped to the 32-bit address space of the ARM. There are six internally generated chips selects (CSx) for devices such as EEPROM memory, modem, front panel, front panel, front end control, parallel output port, and 1394 link device. Each CS has its own defined memory space and a programmable wait register which has a default of maximum allowable values as defined in Table 27. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. These are all programmable by user application software using APIs.” AV7110 Preview at 50.</p> <p>“CS1 is intended for ARM application code, but writes will not be prevented. CS2, CS3, CS4, and CS5 all have the same characteristics. The ARM performs reads and writes to these devices through the extension bus. CS6 is read and write accessible by the ARM. It is also accessed by the TC for TPP DMAs, and it is write only. User C application software selects the PIO of the packets to be sent through this port, the TPP will then send the data Q via DMAs. The parallel port is one byte wide and it is accessed via the least significant byte.” AV7110 Preview at 51.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure																																				
	<div><p>Table 27. An Example of Extension Bus Chip Select Assignment</p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 Mbytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2EFF FFFF</td><td>N/A</td><td>DRAM (up to 16 Mbytes, on RAS1)</td></tr><tr><td>N/A</td><td>2F00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 16 Mbytes, on RAS3)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7110 Preview at 51 tbl. 27.</p> <p>“The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it has to become active before the programmable wait cycle expires. If the combined total wait states exceeds its maximum, the decoder is not guaranteed to function properly. The EXTWAIT signal is synchronized internally with the on-chip 81 MHz clock. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT signal should be at least 24.7 ns. Since the EXTWAIT signal has the potential to stall the whole decoding process, the ARM will cap its wait to 500 ns. Afterwards, the ARM assumes the device that generated the EXTWAIT has failed and will ignore EXTWAIT from then on. Only a software or hardware reset can activate the EXTWAIT signal again. The timing diagram shown in Figure 19 is an example of a read using the EXTWAIT signal.” AV7110 Preview at 53.</p> <p>“The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 32-bit or 16-bit data and 25-bit address. It also supports DMA transfers to/from the extension bus. DMA transfers within the extension bus are not supported directly. They may be accomplished from user application software by using one DMA to the internal data RAM, followed by a second DMA to transfer back to the EBI. Extension bus single read and write cycle timings are shown in Figure 17 and Figure 18 respectively.” AV7110 Preview at 51; <i>see also id.</i> at 52 figs. 17 and 18.</p> <p>“traffic controller (TC)</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)	N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)	N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
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CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port																																		

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	<p>features</p> <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>• Authorizes and manages DMA transfers</li> <li>• Provides SDRAM interface</li> <li>• Manages extension bus</li> <li>• Provides memory access protection</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> <li>- Audio/video decoder to/from SDRAM</li> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> </ul> </li> <li>• Generates chip selects (CS) for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus</li> <li>• Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.</li> </ul>



'472 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p>The diagram illustrates the data flow of a Traffic Controller (TC) within a system. The TC is a central component connected to several peripheral blocks. Above the TC is SDRAM. To the left, a block contains ECD, TPP, and HSDI. Below that is the CP (Control Processor). To the right of the TC is the Extension Bus I/F. Below that is the ARM Core. To the right of the ARM Core are the 32-Bit Data RAM and 32-Bit Program ROM, which includes INT Vectors. Further right is a block containing Palette and Mixer, OSD, and MPEG Audio and Video. Arrows indicate the direction of data flow between the TC and these components.</p> </div> <p>Figure 4. Traffic Controller Data Flow</p> <p>AV7110 Preview at 18 fig. 4.</p> <p><i>See</i> AV7110 Preview at 7 (stating that the TMS320AV7110 includes “an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory.”).</p> <p>“The ARM can control the operation of the audio module via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and over-sampling ratio, and choose the output format for dual channel mode. The ARM will also be able to read status information from the audio module. One 32-bit register provides the MPEG header information and sync, CRC, and PCM status.” AV7110 Preview at 44.</p> <p><i>See</i> AV7110 Preview at 58 fig. 23 (showing examples of DRAM Connections to 16-Bit and 32-Bit Extension buses).</p>

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<p>[1e] a media switch connected to said decoder subsystem by a second data bus, said media switch operative to interface a plurality of system components and operates asynchronously from said processor, wherein said media switch comprises a media manager, said media manager including:</p>	<p>AV7110 Preview discloses or at least renders obvious a media switch connected to said decoder subsystem by a second data bus, said media switch operative to interface a plurality of system components and operates asynchronously from said processor, wherein said media switch comprises a media manager. For example:</p>  <p>The diagram illustrates a system architecture centered around a <b>Traffic Controller</b>. Key components and their connections include:</p> <ul style="list-style-type: none"> <li><b>Input/Output and Processing Blocks:</b> <ul style="list-style-type: none"> <li><b>TPP</b> (Transport Processing Processor) receives a <b>Transport Bitstream From Front End</b> and connects to the <b>Traffic Controller</b> and <b>ECD</b>.</li> <li><b>ECD</b> (Error Correction Decoder) connects to the <b>Traffic Controller</b>.</li> <li><b>Video Decoder</b> and <b>Audio Decoder</b> receive data from the <b>Traffic Controller</b>. The <b>Video Decoder</b> outputs to an <b>OSD</b> (On-Screen Display) and an <b>NTSC/PAL Encoder</b>, which produces <b>Digital Video Output</b> and <b>Y/C or RGB and Composite Video</b>.</li> <li>The <b>Audio Decoder</b> outputs <b>PCM Audio Output</b> and <b>SPDIF Output</b>.</li> </ul> </li> <li><b>System Bus and Memory:</b> <ul style="list-style-type: none"> <li><b>External System Memory</b> is connected to the <b>Traffic Controller</b>.</li> <li>A central <b>System Bus</b> connects the <b>Traffic Controller</b> to the <b>Communication Processor</b>, <b>Extension Bus Interface</b>, <b>ARM/Thumb</b>, <b>Data RAM</b>, and <b>ROM</b>.</li> </ul> </li> <li><b>Communication Processor and I/O:</b> <ul style="list-style-type: none"> <li>The <b>Communication Processor</b> is connected to the <b>System Bus</b> and various external interfaces: <b>GPIO</b>, <b>IR</b>, <b>JTAG</b>, <b>UART (Three)</b>, <b>Smart Card</b>, and <b>12C</b>.</li> <li>It also interfaces with an <b>HSDI</b> block containing <b>1394 I/F</b>, <b>1284 I/F</b>, and <b>Ext DMA</b>.</li> </ul> </li> </ul> <p>AV7110 Preview at 12 fig. 1.</p> <p>“traffic controller (TC) features</p> <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> </ul>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Authorizes and manages DMA transfers</li> <li>• Provides SDRAM interface</li> <li>• Manages extension bus</li> <li>• Provides memory access protection</li> <li>• Manages the data flow between processors and memories               <ul style="list-style-type: none"> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> <li>- Audio/video decoder to/from SDRAM</li> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> </ul> </li> <li>• Generates chip selects (CS) for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus</li> <li>• Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.</li> </ul>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p>The diagram illustrates the data flow of a Traffic Controller (TC) within a system. The TC is a central component that manages data flow between various subsystems. It is connected to SDRAM for memory storage. On the left, it interfaces with ECD (External Control Device), TPP (Timing and Power Processor), HSDI (High-Speed Digital Interface), and CP (Control Processor). On the right, it connects to the Palette and Mixer, OSD (On-Screen Display), and MPEG Audio and Video processing blocks. Below the TC, it interfaces with the ARM Core, 32-Bit Data RAM, and 32-Bit Program ROM (which includes INT Vectors). An Extension Bus I/F (Interface) is also connected to the TC, providing a bidirectional data path to external components.</p> </div> <p>Figure 4. Traffic Controller Data Flow</p> <p>AV7110 Preview at 18 fig. 4.</p> <p>“extension bus interface (EBI)</p> <p>The extension bus interface is a 32-bit or 16-bit bidirectional data bus with a 25-bit address. It also provides 3 external interrupts and a wait line. All the external memories or I/O devices are mapped to the 32-bit address space of the ARM. There are six internally generated chips selects (CSx) for devices such as EEPROM memory, modem, front panel, front panel, front end control, parallel output port, and 1394 link device. Each CS has its own defined memory space and a programmable wait register which has a default of maximum allowable values as defined in Table 27. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. These are all programmable by user application software using APIs.” AV7110 Preview at 50.</p>

'472 Patent Claim	Exemplary Prior Art Disclosure																																				
	<p>“CS1 is intended for ARM application code, but writes will not be prevented. CS2, CS3, CS4, and CS5 all have the same characteristics. The ARM performs reads and writes to these devices through the extension bus. CS6 is read and write accessible by the ARM. It is also accessed by the TC for TPP DMAs, and it is write only. User C application software selects the PIO of the packets to be sent through this port, the TPP will then send the data Q via DMAs. The parallel port is one byte wide and it is accessed via the least significant byte.” AV7110 Preview at 51.</p> <div><p><b>Table 27. An Example of Extension Bus Chip Select Assignment</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 Mbytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2EFF FFFF</td><td>N/A</td><td>DRAM (up to 16 Mbytes, on RAS1)</td></tr><tr><td>N/A</td><td>2F00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 16 Mbytes, on RAS3)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7110 Preview at 51 tbl. 27.</p> <p>“The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it has to become active before the programmable wait cycle expires. If the combined total wait states exceeds its maximum, the decoder is not guaranteed to function properly. The EXTWAIT signal is synchronized internally with the on-chip 81 MHz clock. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT signal should be at least 24.7 ns. Since the EXTWAIT signal has the potential to stall the whole decoding process, the ARM will cap its wait to 500 ns. Afterwards, the ARM assumes the device that generated the EXTWAIT has failed and will ignore EXTWAIT from then on. Only a software or hardware reset can activate the EXTWAIT signal again. The timing diagram shown in Figure 19 is an example of a read using the EXTWAIT signal.” AV7110 Preview at 53.</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)	N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)	N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
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	<p>“The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 32-bit or 16-bit data and 25-bit address. It also supports DMA transfers to/from the extension bus. DMA transfers within the extension bus are not supported directly. They may be accomplished from user application software by using one DMA to the internal data RAM, followed by a second DMA to transfer back to the EBI. Extension bus single read and write cycle timings are shown in Figure 17 and Figure 18 respectively.” AV7110 Preview at 51; <i>see also id.</i> at 52 figs. 17 and 18.</p> <p>“The descrambling of the incoming data is performed automatically with minimum intervention by the CPU. The TPP module detects which transport packets are scrambled, at either the program elementary stream (PES) or the transport stream level, and routes the data through the ECD as necessary. The ECD stores the descrambler keys locally and automatically selects the correct key of a specific PID. Up to 16 sets of keys are stored in the key table for use by the ECD. It is possible for more than one PIO to use the same key. The descrambler keys are derived by the conditional access software using the command packet from the bit-stream.” AV7110 Preview at 23.</p> <p>“The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.</p> <p>Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM, and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.” AV7110 Preview at 13.</p> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start</p>

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	<p>up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.” AV7110 Preview at 22.</p> <p>Together with the ARM, the TPP also handles program clock reference (PCR) recovery with an external VCXO. The TPP will latch and transfer to the ARM its internal system clock upon the arrival of any packet which contains a PCR. After further processing on the packet and identifying the system clock, the ARM calculates the difference between the system clock from a bit-stream and the actual system clock at the time the packet arrives. Then, the ARM filters the difference and sends it through an 8-bit sigma-delta DAC to control the external VCXO. The ARM will drive the VCXO to its center frequency during start-up or, if enabled by an API, after channel change when there is no incoming PCR.” AV7110 Preview at 13.</p> <p>“At startup the hardware STC counter is free running and the increments to the software extension of the system STC take place every 1 .4 ms. Both audio and video decoders are initialized to free-run. This condition is identical for system startup as well as for re-synchronization after a channel change. Once a PCR channel is activated by user software through an API, the on-chip software will monitor the incoming data in the PCR designated channel and reset the system common reference counter STCs<sub>sys</sub> to the first PCR that arrives in the designated stream (full 42 bits). At the same time, the video and audio STC are initialized to the same value, if they are enabled via the appropriate API calls.” AV7110 Preview at 48.</p> <p>“Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PC Rs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“The video synchronization of STC and PTS can be enabled/disabled via an API. The STC for the video decoder</p>

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	<p>is clocked by the 27 MHz system clock. The initial value of the video STC (STCvid) is written to the video decoder from the firmware. This happens at the time that the first PCR from the designated PCR channel arrives at the AF. In some cases the PTS can consistently be off by a certain amount, causing the video buffer to eventually over- or under-run. If this occurs, the firmware will detect the under/over-runs via FIQ-s and adjust the video STC with an offset, such that the under/over-run ceases.” AV7110 Preview at 50.</p> <p>“Command communication from the 'AV7110 to the ESC is done using the 4-bit EDMA A bus which is mapped into the ARM addressing space of the 'AV7110 when the EDMA port is selected. This will allow user software to write directly to the registers of the ESC. For details of these registers, refer to the appropriate external controller documentation. The 'AV7110 does not processing of this data and thus places no restriction on its function. An access to this memory space while the EDMA is selected will automatically generate a read or write cycle on the HSDI using the EDMA_RO and EDMA_WR signals and the EDMA_CS signal. Timing for these access is shown in Figure 31.” AV7110 Preview at 67.</p> <p>“communication processor features</p> <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> <li>• Provides 3 general purpose UARTs - two at up to 115.2 Kbps and one at up to 9.6 Kbps</li> <li>• Accepts IR input signals</li> <li>• Generates IR output signals</li> <li>• Provides up to nine general purpose I/Os</li> <li>• Manages 12C and JTAG interfaces</li> </ul> <p>This module contains a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR, and 12C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM CPU. Interrupts are used to communicate between these interface modules and the ARM CPU.” AV7110 Preview at 72; <i>see generally id.</i> at 72-78 (describing different functions and functional blocks of the communication processor).</p> <p>“Together with the ARM, the TPP also handles program clock reference (PCR) recovery with an external VCXO. The TPP will latch and transfer to the ARM its internal system clock upon the arrival of any packet which contains a PCR. After further processing on the packet and identifying the system clock, the ARM calculates the difference between the system clock from a bit-stream and the actual system clock at the time the packet arrives. Then, the ARM filters the difference and sends it through an 8-bit sigma-delta DAC to control the external</p>



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	<p>VCXO. The ARM will drive the VCXO to its center frequency during start-up or, if enabled by an API, after channel change when there is no incoming PCR.” AV7110 Preview at 13; <i>see also id.</i> at 22-23.</p> <p>“The 'AV7110 uses the STC and PTS to determine the play back time of the decoded audio and video data. The relationship between STC and PTS is determined at the time of the generation of the generation of the respective elementary streams (ES). Upon reception, the demultiplexing software in the 'AV7110 extracts the video PTS and inserts it in an array of PTS and byte-count information maintained for the video decoder. For the audio the PTS information is extracted by the audio decoder front end from the PES. The video decoder contains an STC counter that is clocked by the system clock (27 MHz) and normalized to a 90 kHz reference. The audio decoder does not contain a counter. Instead, it gets updated from the system time reference counter every 1 .4 ms.” AV7110 Preview at 48.</p> <p>“The audio synchronization of STC and PTS can be enabled/disabled through an API. The STC for the audio decoder time reference is loaded by the firmware every time the system reference counter (STCs<sub>sys</sub>) rolls over. This roll over will occur every 26 ticks of the 90 kHz portion of the hardware system clock counter in the AV7110. This is approximately every 1 .4 ms. The firmware will receive an FIQ from the counter and write STCs<sub>sys</sub> + aud_offset to the STC register in the audio decoder. The value for aud_offset is 0 by default after initialization and after audio channel change.” AV7110 Preview at 49.</p> <p>“IEEE 1394 interface On power-up the IEEE 1394 interface is enabled on the HSDI. An API call can be used to configure the HSDI for another mode or to return to the 1394 interface if necessary. To complete the 1394 implementation, the 'AV7110 requires an external packetizer and link layer controller, and a physical layer device. Figure 26 shows the connection between the 'AV7110 and these devices.” AV7110 Preview at 62; <i>see id.</i> at fig. 26.</p> <p>“IEEE 1284 interface The IEEE 1284 interface on the 'AV7110 has the following characteristics:</p> <ul style="list-style-type: none"> <li>• Supports transfer of up to 10 Mbits/sec</li> <li>• Supports the compatibility, nibble and byte mode</li> <li>• Supports the ECP mode except for run length coding compression</li> <li>• Does not support the EPP mode</li> <li>• Peripheral mode only</li> </ul> <p>The IEEE 1284 interface is used to connect the 'AV7110 to an external host. The 'AV7110 side of the protocol</p>

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	<p>can be handled by an IEEE 1284 peripheral interface controller on the chip such as the SN54ACT1284/SN? 4ACT1284. Since the signals on the HSDI are 5-V-tolerant, they can be connected directly to this external 1284 driver.” AV7110 Preview at 69; <i>see id.</i> fig.33; <i>see also id.</i> at 69-70.</p> <p>“high speed data interface (HSDI) The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device. Logic for these three interfaces share signal pins and hence only one can be active at any given time. Table 28 shows the pin definitions for the HSDI in its various configurations. Switching from one interface to another will require a predefined sequence of API calls. Two signal pins (HSDI_ STATUS[1 :OJ) indicate which of the three interfaces is active. They can be used to control external logic for interface arbitration. The definition of these signals is shown at the bottom of Table 28.” AV7110 Preview at 60.</p> <p>“The 32-bit ARM processor running at 40.5 MHz and its associated firmware provide the following:</p> <ul style="list-style-type: none"> <li>• Initialization and management of all hardware modules</li> <li>• Service for selected interrupt generated by hardware modules and I/O ports</li> <li>• Application program interface (API) for users to develop their own applications” AV7110 Preview at 15.</li> </ul> <p>“The CPU in the 'AV7110 is a 32-bit RISC processor, the ARM7TDM I/Thumb, which has the capability to execute instructions in 16- or 32-bit format at a clock frequency of 40.5 MHz. The regular ARM instructions are exactly one word (32-bit) long, and the data operations are only performed on word quantities. The LOAD and STORE instructions however, can transfer either byte, half-word or word quantities. The Thumb uses the same 32-bit architecture with an 16-bit instruction set. That is, it retains the 32-bit performance but reduces the code size with 16-bit instructions. With 16-bit instruction, the Thumb still gives 70-80% of the performance of the ARM when running ARM instructions from 32-bit memory.” AV7110 Preview at 15; <i>see also id.</i> (stating that ARM and Thumb are used interchangeably in the AV7110 Preview’s disclosure).</p> <p>“The 'AV7110 includes three general purpose UARTs that are memory mapped and fully accessible by user application programs. A set of APIs exists to assist in programming them. The output of the UARTs are digital and require external level shifters for RS232 compliance. These UARTs support full duplex mode and are double buffered with sufficient FIFO space to minimize the interrupt frequency to the ARM even when they are operating at their maximum transmission speeds.” AV7110 Preview at 75.</p>

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	<p>“IR input port Hardware is provided to capture and deliver IR data bits to user software for command decoding. Sample IR command decoding driver software for several commonly used IR formats are provided with the 'AV7110. API software is provided to configure the hardware to recognize IR format with different parameter settings:</p> <ul style="list-style-type: none"> <li>• data frame length (up to 32 bits)</li> <li>• maximum time between frame (a 13-bit count equals one period of CLK40)</li> <li>• LSB/MSB first</li> <li>• repeat pattern present</li> <li>• stop pattern present</li> <li>• compare enable (ignore repeated frames if this bit is set)</li> </ul> <p>At start up, user application software sets up the parameters above and defines the encoding pattern of the preamble, stop, repeat, data zero, and data one by storing the duration of the high and low levels of each pattern in the IR-input-RAM. The IR hardware will then look for IR input (assumed demodulated) which matches the pattern” AV7110 Preview at 75.</p> <p>“general purpose I/Os The 'AV7110 has four dedicated (101, 102, 104, and 105) and five multiplexed general purpose I/O pins (103 and 106 to 109) which are user configurable. Each I/O port has its own 32-bit control/status register, IOCSR<sub>n</sub>, where n ranges from 1 to 9.</p> <p>If an I/O is configured as an input and the delta interrupt mask is cleared, an IRQ is generated whenever an input changes state. If the delta interrupt mask is set, interrupts to the ARM are disabled. If no other device drives the I/O pin while it is configured as an input, it will be held high by an internal pullup resistor.</p> <p>If an I/O is configured as an output (by setting the cio bit in the corresponding control/status register), the value contained in the io_out) bit of the control/status register is output. Interrupt generation is disabled when an I/O is configured as an output.” AV7110 Preview at 77; <i>see also id.</i> tbl. 37.</p> <p>“Hardware is provided on the 'AV7110 to generate drive signal on the output pin according to input data bit and format control signals provided by user software or to just retransmit the input signal received at the IR input port. External buffering is required to drive an IR LED.</p> <p>In order to communicate with IR receivers of different IR formats, the 'AV7110s IR output encoder supports a very flexible IR frame format. The format of the frame is specified through APIs and can be changed as frequently as per IR command transmission.” AV7110 Preview at 75.</p>

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	<p>“The smart card interface on the 'AV7110 supports clock frequencies of: 2.025, 3.375, 4.05, 4.5, 6.0, 6.75, 8.1, and 13.5 MHz. All these clock frequencies are generated internally from the 81 MHz clock.” AV7110 Preview at 72.</p> <p>“Since there is only an 8-bit bus on the HSDI, the ESC is limited to an 8-bit, single bus architecture so its mode selection inputs should be set to mode 0. The upper data bits can be left floating since they have internal pullups on the ESC. Likewise, the AD-0 inputs of the ESC will not be used for this mode and can be left unconnected. The ESC requires an external clock source from 10 MHz to 40 MHz. Since the CLK40 signal of the 'AV7110 is actually a 40.5 MHz clock it cannot be used directly for this controller without violating its specification. Table 2 shows the signals needed for the EDMA interface.” AV7110 Preview at 66; <i>see id.</i> tbl. 32 (listing DMA interface signals).</p> <p><i>See</i> AV7110 Preview at 58 fig. 23 (showing examples of DRAM Connections to 16-Bit and 32-Bit Extension buses).</p> <p><i>See</i> AV7110 Preview at 60, table 29 (“Types of DMA Transfers Allowed for Data Ports”).</p> <p><i>See</i> claim 1 at 1f-1i, <i>infra</i>.</p>
[1f] a host controller;	<p>AV7110 Preview discloses or at least renders obvious a host controller. For example:</p> <p>“high speed data interface (HSDI)  The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device. Logic for these three interfaces share signal pins and hence only one can be active at any given time. Table 28 shows the pin definitions for the HSDI in its various configurations. Switching from one interface to another will require a predefined sequence of API calls. Two signal pins (HSDI_ STATUS[1:0]) indicate which of the three interfaces is active. They can be used to control external logic for interface arbitration. The definition of these signals is shown at the bottom of Table 28.” AV7110 Preview at 60.</p>

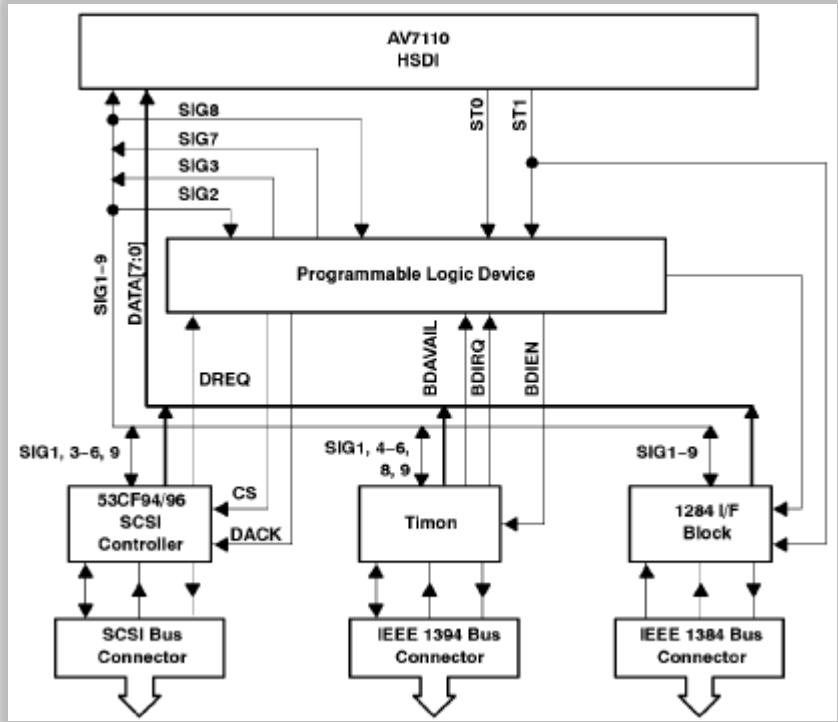
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	<div><p><b>Table 28. High Speed Data Interface Signal Pin Assignment</b></p><table><tr><th>PIN NAME</th><th>I/O</th><th>IEEE 1394 I/F</th><th>IEEE 1284 I/F</th><th>EXTERNAL DMA</th></tr><tr><td>HSDI_DATA[7:0]</td><td>I/O</td><td>BDI[7:0] (In/Out)</td><td>1284_D[7:0] (In/Out)</td><td>EDMA_DB[7:0] (In/Out)</td></tr><tr><td>HSDI_SIG1</td><td>O</td><td>BDIRW (Out)</td><td>1284_ERROR (Out)</td><td>EDMA_RD (Out)</td></tr><tr><td>HSDI_SIG2</td><td>O</td><td>BDIEN (Out)</td><td>1284_ACK (Out)</td><td>EDMA_DACK (Out)<sup>†</sup></td></tr><tr><td>HSDI_SIG3</td><td>I or O</td><td>BDAVAIL (In)</td><td>1284_STROBE (In)</td><td>EDMA_A[3] (Out)</td></tr><tr><td>HSDI_SIG4</td><td>I/O, I or O</td><td>BDIF[2] (In/Out)</td><td>1284_SLCTIN (In)</td><td>EDMA_A[2] (Out)</td></tr><tr><td>HSDI_SIG5</td><td>I/O, I or O</td><td>BDIF[1] (In/Out)</td><td>1284_AF (In)</td><td>EDMA_A[1] (Out)</td></tr><tr><td>HSDI_SIG6</td><td>I/O or O</td><td>BDIF[0] (In/Out)</td><td>1284_SLT (Out)</td><td>EDMA_A[0] (Out)</td></tr><tr><td>HSDI_SIG7</td><td>I</td><td>BDIRQ (In)</td><td>1284_INIT (In)</td><td>EDMA_DREQ (In)<sup>†</sup></td></tr><tr><td>HSDI_SIG8</td><td>O</td><td>N/A (drives high)</td><td>1284_PEND (Out)</td><td>EDMA_CS (Out)</td></tr><tr><td>HSDI_SIG9</td><td>O</td><td>N/A (drives high)</td><td>1284_BUSY (Out)</td><td>EDMA_WR (Out)</td></tr><tr><td>HSDI_STATUS[1:0]</td><td>O</td><td>00</td><td>1x (see IEEE 1284 Interface)</td><td>01</td></tr></table></div> <p>AV7110 Preview at 60 tbl. 28; <i>see also id.</i> tbl. 29 (listing different types of DMA transfers allowed for data ports).</p> <div><p>The diagram illustrates the functional block diagram of the High Speed Data Interface (HSDI) within a chip boundary. Key components include:</p><ul style="list-style-type: none"><li><b>TPP (Test Point Probe)</b> and <b>ECD (Error Correction Decoder)</b> are connected to the <b>Reconfigurable I/O</b> block.</li><li>The <b>Reconfigurable I/O</b> block is divided into three sections: <b>1394</b>, <b>1284</b>, and <b>Ext. DMA</b>.</li><li>The <b>Reconfigurable I/O</b> block is connected to the <b>DMA Controller</b>.</li><li>The <b>DMA Controller</b> is connected to <b>SRAM</b>, <b>DMA</b>, and <b>SDRAM</b>.</li><li><b>SRAM</b> is connected to <b>DMA</b>, which in turn is connected to <b>DRAM</b>.</li><li>The <b>DMA</b> block is also connected to <b>SDRAM</b>.</li></ul></div> <p>AV7110 Preview at 61 fig. 25 (showing functional block diagram of HSDI).</p> <p>“IEEE 1394 interface</p>	PIN NAME	I/O	IEEE 1394 I/F	IEEE 1284 I/F	EXTERNAL DMA	HSDI_DATA[7:0]	I/O	BDI[7:0] (In/Out)	1284_D[7:0] (In/Out)	EDMA_DB[7:0] (In/Out)	HSDI_SIG1	O	BDIRW (Out)	1284_ERROR (Out)	EDMA_RD (Out)	HSDI_SIG2	O	BDIEN (Out)	1284_ACK (Out)	EDMA_DACK (Out) <sup>†</sup>	HSDI_SIG3	I or O	BDAVAIL (In)	1284_STROBE (In)	EDMA_A[3] (Out)	HSDI_SIG4	I/O, I or O	BDIF[2] (In/Out)	1284_SLCTIN (In)	EDMA_A[2] (Out)	HSDI_SIG5	I/O, I or O	BDIF[1] (In/Out)	1284_AF (In)	EDMA_A[1] (Out)	HSDI_SIG6	I/O or O	BDIF[0] (In/Out)	1284_SLT (Out)	EDMA_A[0] (Out)	HSDI_SIG7	I	BDIRQ (In)	1284_INIT (In)	EDMA_DREQ (In) <sup>†</sup>	HSDI_SIG8	O	N/A (drives high)	1284_PEND (Out)	EDMA_CS (Out)	HSDI_SIG9	O	N/A (drives high)	1284_BUSY (Out)	EDMA_WR (Out)	HSDI_STATUS[1:0]	O	00	1x (see IEEE 1284 Interface)	01
PIN NAME	I/O	IEEE 1394 I/F	IEEE 1284 I/F	EXTERNAL DMA																																																									
HSDI_DATA[7:0]	I/O	BDI[7:0] (In/Out)	1284_D[7:0] (In/Out)	EDMA_DB[7:0] (In/Out)																																																									
HSDI_SIG1	O	BDIRW (Out)	1284_ERROR (Out)	EDMA_RD (Out)																																																									
HSDI_SIG2	O	BDIEN (Out)	1284_ACK (Out)	EDMA_DACK (Out) <sup>†</sup>																																																									
HSDI_SIG3	I or O	BDAVAIL (In)	1284_STROBE (In)	EDMA_A[3] (Out)																																																									
HSDI_SIG4	I/O, I or O	BDIF[2] (In/Out)	1284_SLCTIN (In)	EDMA_A[2] (Out)																																																									
HSDI_SIG5	I/O, I or O	BDIF[1] (In/Out)	1284_AF (In)	EDMA_A[1] (Out)																																																									
HSDI_SIG6	I/O or O	BDIF[0] (In/Out)	1284_SLT (Out)	EDMA_A[0] (Out)																																																									
HSDI_SIG7	I	BDIRQ (In)	1284_INIT (In)	EDMA_DREQ (In) <sup>†</sup>																																																									
HSDI_SIG8	O	N/A (drives high)	1284_PEND (Out)	EDMA_CS (Out)																																																									
HSDI_SIG9	O	N/A (drives high)	1284_BUSY (Out)	EDMA_WR (Out)																																																									
HSDI_STATUS[1:0]	O	00	1x (see IEEE 1284 Interface)	01																																																									

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	<p>On power-up the IEEE 1394 interface is enabled on the HSDI. An API call can be used to configure the HSDI for another mode or to return to the 1394 interface if necessary. To complete the 1394 implementation, the 'AV7110 requires an external packetizer and link layer controller, and a physical layer device. Figure 26 shows the connection between the 'AV7110 and these devices.” AV7110 Preview at 62; see id. at fig. 26.</p> <p>“IEEE 1284 interface  The IEEE 1284 interface on the 'AV7110 has the following characteristics:</p> <ul style="list-style-type: none"> <li>• Supports transfer of up to 10 Mbits/sec</li> <li>• Supports the compatibility, nibble and byte mode</li> <li>• Supports the ECP mode except for run length coding compression</li> <li>• Does not support the EPP mode</li> <li>• Peripheral mode only</li> </ul> <p>The IEEE 1284 interface is used to connect the 'AV7110 to an external host. The 'AV7110 side of the protocol can be handled by an IEEE 1284 peripheral interface controller on the chip such as the SN54ACT1284/SN? 4ACT1284. Since the signals on the HSDI are 5-V-tolerant, they can be connected directly to this external 1284 driver.” AV7110 Preview at 69; see id. fig.33; see also id. at 69-70.</p>

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	<div> <p style="text-align: center;"><b>Figure 26. 1394 Interface</b></p> </div> <p>AV7110 Preview at 62; <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) C packets to and from the internal data RAM. This data can then be processed by the user software as needed.”); <i>see also id.</i> at 63 (listing signals associated with the 1394 interface).</p> <p>“external DMA interface (EDMA) When configured for EDMA operation (HSDI_STATUS[1 LO] = 01), the HSDI is capable of a glue less connection to an external enhanced SCSI controller (ESC) device such as the NCR 53CF94-1 /53CF96-1. Figure 30 shows the connections for this example configuration.” AV7110 Preview at 66.</p>

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	<div><p>Figure 30. Interfacing the 'AV7110 to a SCSI Chip</p></div> <p>AV7110 Preview at 66 fig. 30.</p>



'472 Patent Claim	Exemplary Prior Art Disclosure
	 <p>The diagram illustrates the AV7110 HSDI system architecture. At the top is the AV7110 HSDI block, which connects to a central Programmable Logic Device (PLD). The PLD manages three main interfaces: a SCSI interface, an IEEE 1394 interface, and an IEEE 1384 interface. The SCSI interface includes a 53CF94/96 SCSI Controller connected to a SCSI Bus Connector. The IEEE 1394 interface includes a Timon block connected to an IEEE 1394 Bus Connector. The IEEE 1384 interface includes a 1284 I/F Block connected to an IEEE 1384 Bus Connector. The PLD receives HSDI signals (SIG2, SIG3, SIG7, SIG8, SIG1-9, STO, ST1) and outputs control signals (DREQ, BDAVAIL, BDIRQ, BDIEN) to the interface blocks. The 1284 I/F Block is shown in a tri-stated condition, indicating it is disabled when not selected.</p> <p>AV7110 Preview at 71 fig. 34; <i>see id.</i> (“In this example, the logic is grouped into a single programmable logic device, For simplicity, some of the HSDI signal names have been shorted (i.e., ST1 and STO to represent HSDI_STATUS[1 :O], etc.). Note that the 1284 interface block is completely disabled (tri-stated) when it is not selected and so can be directly connected to the HSDI bus.”).</p> <p><i>See</i> AV7110 Preview at 1 (stating that the AV7110 includes a “[c]onfigurabe High Speed Data Interface to Connect to Either an IEEE 1394 Link Device, an IEEE 1284 Interface, or an External DMA Device Like SCSI that Supports Up to 16 Mbps Data Rate “).</p>

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	<div> <p>The diagram illustrates the AV7110 HSDI interface. At the top, a block labeled 'AV7110 HSDI' has several output lines: 1284_BUSY, 1284_PEND, 1284_D[7:0], 1284_SLT, 1284_ACK, 1284_ERROR, 1284_STROBE, 1284_SLCTIN, 1284_AF, 1284_INIT, HSDI_STATUS[1], and HSDI_STATUS[0]. Below this, two identical blocks labeled '74ACT1284' are shown, each with inputs A, B, HD, and DIR. The first 74ACT1284 block is connected to the AV7110 HSDI block via 1284_BUSY, 1284_PEND, 1284_D[7:0], 1284_SLT, 1284_ACK, and 1284_ERROR. The second 74ACT1284 block is connected to the first via 1284_D[7:0], 1284_SLT, 1284_ACK, and 1284_ERROR. Both 74ACT1284 blocks are connected to an 'IEEE 1284 Bus Connector' block at the bottom via 1284_STROBE, 1284_SLCTIN, 1284_AF, 1284_INIT, HSDI_STATUS[1], and HSDI_STATUS[0]. The IEEE 1284 Bus Connector block has a large arrow pointing downwards, indicating connection to the host.</p> </div> <p>AV7110 Preview at 69; <i>see also id.</i> at 70 tbl. 34 (listing signals associated with IEEE 1284 interface).</p> <p>“The application software interfaces with the peripheral interface controller via RTSL API calls. To send data to the host the application software will issue an API call to transfer the data from memory to the peripheral interface via a DMA. To receive data from the host, the application software will issue an API to transfer a predetermined number of bytes from the peripheral interface to internal data memory via the HSDI DMA unit. The user application software must have a way to determine the number of bytes of data that is expected from the host.” AV7110 Preview at 70.</p> <p>“combining the 1394, 1284 and external controller interfaces  With additional external logic it is possible to combine the three HSDI interfaces within a single design. Note that performing the API call to switch between interfaces will involve resetting the HSDI and so transfers between interfaces are not practical (i.e., 1394 to 1284). Switching between HSDI modes should be detected by external logic and proper care should be taken to prevent contention between the external devices and the HSDI interface.</p>

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	<p>Figure 34 shows the block diagram of an example of this configuration based on the devices used previously.” AV7110 Preview at 70.</p>
<p>[1g] a DMA controller;</p>	<p>AV7110 Preview discloses or at least renders obvious a DMA controller. For example:</p> <p>“The data transfer from TPP to the data RAM is done via DMA. Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM, and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.” AV7110 Preview at 13.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PIO table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.</p> <p>The only difference between the two scenarios is that in the case where there is no TPP traffic, the TPP buffer pool can be used. In the case where there is active TPP data, a general purpose buffer needs to be used.</p>

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	<p>Additionally, when TPP data traffic is active, the end of packet (EOP) interrupt generation will require an indication data type configured in the header, which describes where the data to be processed is to be found.” AV7110 Preview at 21.</p> <p>“managing DMA transfer</p> <p>The TC in the 'AV7110 provides DMA capability to facilitate large block transfers between memories and buffers. The burst length (in multiple of 4 bytes) of the DMAs are independently selectable via 6-bit registers with an API. This provides a burst value from 4 to 188 bytes.</p> <p>The SDRAM is used to store system level tables, video and audio bit-streams, reconstructed video images, OSD data, video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware.</p> <p>The TC manages two types of DMA transfers, but only one of them, the general purpose DMA (GPDMA), is accessible to the user. The user has no knowledge of the other type of DMAs which are initiated by the TPP, the video decoder, the audio decoder, and the OSD module. The GPDMA includes ARM-generated and bitBLT-generated DMAs. The TC can accept up to 4 GPDMA at any given time. DMA from the data RAM to the extension bus (and vice versa) is byte aligned. Table 3 describes the allowable GPDMA transfers.</p> <p>....</p> <p>Note that there is no direct DMA transfer between the extension bus memories and the SDRAM. the user can use the bitBLT hardware which uses the internal data RAM as an intermediate step for this process. Alternatively, an API is provided to transfer data from the extension bus memories to the SDRAM (and vice versa). This is accomplished using this internal data RAM and two DMAs. One from the extension bus to the internal data RAM and the second from the internal data RAM to the SDRAM.” AV7110 Preview at 20; <i>see also id.</i> tbl. 3 (showing allowed DMA transfers between different functional blocks).</p> <p>“The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 32-bit or 16-bit data and 25-bit address. It also supports DMA transfers to/from the extension bus. DMA transfers within the extension bus are not supported directly. They may be accomplished from user application software by using one DMA to the internal data RAM, followed by a second DMA to transfer back to the EBI. Extension bus single read and write cycle timings are shown in Figure 17 and Figure 18 respectively.” AV7110 Preview at 51; <i>see also id.</i> at 52 figs. 17 and 18.</p> <p>“An internal DMA unit is dedicated for the HSDI port and is under user level API control. There are some restrictions to the source, destinations and data types of this DMA unit. These are detailed in Table 29. The</p>

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	<p>firmware available in the first samples will not support I/A packets, multiple I packet channels or the Program Map Table insertion for IEEE 1394. In any event, a DMA write from the TPP to the HSDI in any of its configurations, only sends the payload. It is impossible to view and perform a DMA transfer to the HSDI from the same program source..” AV7110 Preview at 60.</p> <div><p>Table 29. Types of DMA Transfers Allowed for Data Ports</p><table><tr><th>INTERFACE CONFIGURATION</th><th>SOURCE DATA TYPES</th><th>POSSIBLE DESTINATION FOR DMA INPUT</th><th>POSSIBLE SOURCES FOR DMA OUTPUT</th></tr><tr><td>IEEE 1394/TPP (Dedicated I/F<sup>†</sup>)</td><td>M Packets</td><td>TPP</td><td>TPP</td></tr><tr><td>IEEE 1394 I/F</td><td>M Packets<sup>‡</sup></td><td>DRAM or SDRAM<sup>§</sup></td><td>TPP, DRAM or SDRAM</td></tr><tr><td>IEEE 1284 I/F</td><td>Elementary Stream or Data<sup>‡</sup></td><td>DRAM or SDRAM</td><td>TPP, DRAM or SDRAM</td></tr><tr><td>External DMA</td><td>Elementary Stream or Data<sup>‡</sup></td><td>DRAM or SDRAM</td><td>TPP, DRAM or SDRAM</td></tr></table><p><sup>†</sup> This is a dedicated data path which is separate from the DMA channel.</p><p><sup>‡</sup> Other data types or support like I/A packets, MPEG1 system and MPEG2 program require versions of the firmware which will not be available in the first samples.</p><p><sup>§</sup> The source or destination between DRAM and SDRAM is a two-stage process using the on chip SRAM as an intermediate step.</p></div> <p>AV7110 Preview at 60 fig. 29.</p> <p>“external DMA Interface (EDMA)</p> <p>When configured for EDMA operation (HSDI_ STATUS[1 LO] = 01), the HSDI is capable of a glue less connection to an external enhanced SCSI controller (ESC) device such as the NCR 53CF94-1 /53CF96-1. Figure 30 shows the connections for this example configuration.” AV7110 Preview at 66.</p> <p>“Command communication from the 'AV7110 to the ESC is done using the 4-bit EDMA A bus which is mapped into the ARM addressing space of the 'AV7110 when the EDMA port is selected. This will allow user software to write directly tot he registers of the ESC. For details of these registers, refer to the appropriate external controller documentation. The 'AV7110 does not processing of this data and thus places no restriction on its function. An access to this memory space while the EDMA is selected will automatically generate a read or write cycle on the HSDI using the EDMA_RO and EDMA_WR signals and the EDMA_CS signal. Timing for these access is shown in Figure 31.” AV7110 Preview at 67.</p> <p>“The EDMA DREQ signal should be used by the external controller to initiate an external DMA ('AV7110 DMA between the HSDI and the external device). EDMA_DREQ will be ignored until the DMA has been properly</p>	INTERFACE CONFIGURATION	SOURCE DATA TYPES	POSSIBLE DESTINATION FOR DMA INPUT	POSSIBLE SOURCES FOR DMA OUTPUT	IEEE 1394/TPP (Dedicated I/F <sup>†</sup> )	M Packets	TPP	TPP	IEEE 1394 I/F	M Packets <sup>‡</sup>	DRAM or SDRAM <sup>§</sup>	TPP, DRAM or SDRAM	IEEE 1284 I/F	Elementary Stream or Data <sup>‡</sup>	DRAM or SDRAM	TPP, DRAM or SDRAM	External DMA	Elementary Stream or Data <sup>‡</sup>	DRAM or SDRAM	TPP, DRAM or SDRAM
INTERFACE CONFIGURATION	SOURCE DATA TYPES	POSSIBLE DESTINATION FOR DMA INPUT	POSSIBLE SOURCES FOR DMA OUTPUT																		
IEEE 1394/TPP (Dedicated I/F <sup>†</sup> )	M Packets	TPP	TPP																		
IEEE 1394 I/F	M Packets <sup>‡</sup>	DRAM or SDRAM <sup>§</sup>	TPP, DRAM or SDRAM																		
IEEE 1284 I/F	Elementary Stream or Data <sup>‡</sup>	DRAM or SDRAM	TPP, DRAM or SDRAM																		
External DMA	Elementary Stream or Data <sup>‡</sup>	DRAM or SDRAM	TPP, DRAM or SDRAM																		

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	<p>configured using the appropriate API calls. The source/destination addresses, the DMA size and the burst are under user software control via this API. Once asserted, the 'AV7110 will respond by transferring the data one byte at a time between the external device and the internal data RAM using the EDMA_RD and EDMA_WR signals and the EDMA_DACK signal as shown in Figure 32.” AV7110 Preview at 67.</p> <p>“When the 'AV7110 is transferring data to/from the DRAM via DMA, it makes full use of the page mode read/write cycle and will read/write a byte/half-word/word every 50 ns (2 clock cycles). When 16-bit wide DRAM is accessed from the ARM, the DRAM controller will make use of page mode read cycle to transfer each 32 bit word. Each new 32-bit write/read is addressed independently to the DRAM.” AV7110 Preview at 57.</p> <p>“The HSDI supports the following concurrent data transfers.</p> <ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/program to 1394 (using dedicated I/F - see NOTE XXXX of Table 29)</li> <li>• TPP/program to decoder; 1394/DMA to/from memory</li> <li>• TPP/program to decoder; memory/DMA to/from HSDI</li> <li>• TPP/program to decoder; TPP/DMA to HSDI</li> <li>• TPP/program to decoder; TPP/program to 1394; memory/DMA to/from 1394</li> <li>• TPP/program to decoder; 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; TPP/DMA to 1394” AV7110 Preview at 61.</li> </ul> <div> </div> <p>AV7110 Preview at 61 fig. 25 (showing the functional blocks of the HSDI); <i>see also id.</i> at 62-65 (showing describing AV7110’s reading and writing of data from/to the 1394 interface).</p>

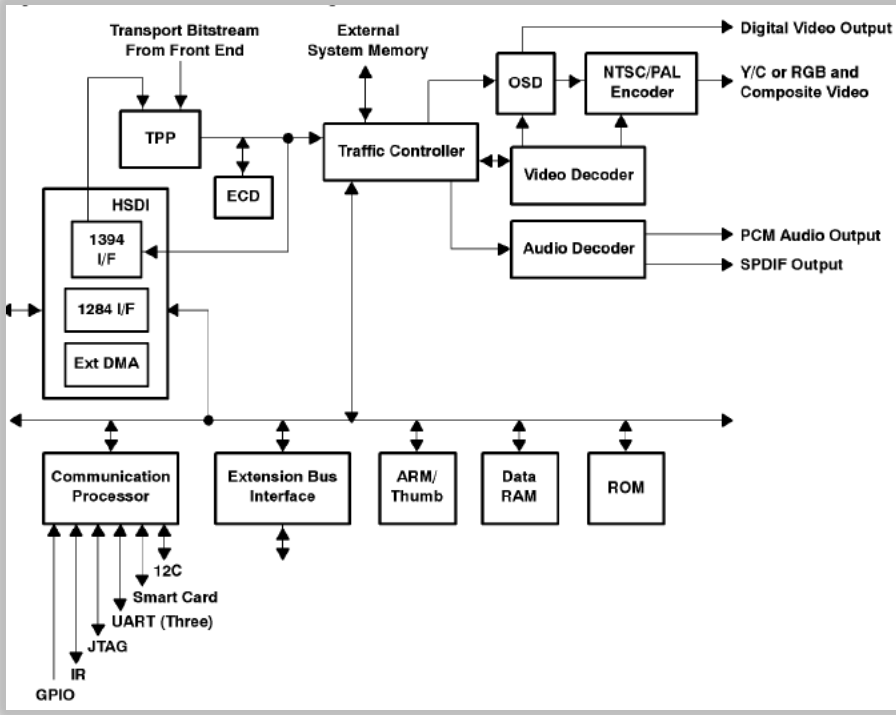
'472 Patent Claim	Exemplary Prior Art Disclosure																																																												
	<p>“high speed data interface (HSDI) The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device. Logic for these three interfaces share signal pins and hence only one can be active at any given time. Table 28 shows the pin definitions for the HSDI in its various configurations. Switching from one interface to another will require a predefined sequence of API calls. Two signal pins (HSDI_ STATUS[1:0]) indicate which of the three interfaces is active. They can be used to control external logic for interface arbitration. The definition of these signals is shown at the bottom of Table 28.” AV7110 Preview at 60.</p> <div><p><b>Table 28. High Speed Data Interface Signal Pin Assignment</b></p><table><tr><th>PIN NAME</th><th>I/O</th><th>IEEE 1394 I/F</th><th>IEEE 1284 I/F</th><th>EXTERNAL DMA</th></tr><tr><td>HSDI_DATA[7:0]</td><td>I/O</td><td>BDI[7:0] (In/Out)</td><td>1284_D[7:0] (In/Out)</td><td>EDMA_DB[7:0] (In/Out)</td></tr><tr><td>HSDI_SIG1</td><td>O</td><td>BDIRW (Out)</td><td>1284_ERROR (Out)</td><td>EDMA_RD (Out)</td></tr><tr><td>HSDI_SIG2</td><td>O</td><td>BDIEN (Out)</td><td>1284_ACK (Out)</td><td>EDMA_DACK (Out)<sup>†</sup></td></tr><tr><td>HSDI_SIG3</td><td>I or O</td><td>BDAVAIL (In)</td><td>1284_STROBE (In)</td><td>EDMA_A[3] (Out)</td></tr><tr><td>HSDI_SIG4</td><td>I/O, I or O</td><td>BDIF[2] (In/Out)</td><td>1284_SLCTIN (In)</td><td>EDMA_A[2] (Out)</td></tr><tr><td>HSDI_SIG5</td><td>I/O, I or O</td><td>BDIF[1] (In/Out)</td><td>1284_AF (In)</td><td>EDMA_A[1] (Out)</td></tr><tr><td>HSDI_SIG6</td><td>I/O or O</td><td>BDIF[0] (In/Out)</td><td>1284_SLT (Out)</td><td>EDMA_A[0] (Out)</td></tr><tr><td>HSDI_SIG7</td><td>I</td><td>BDIRQ (In)</td><td>1284_INIT (In)</td><td>EDMA_DREQ (In)<sup>†</sup></td></tr><tr><td>HSDI_SIG8</td><td>O</td><td>N/A (drives high)</td><td>1284_PEND (Out)</td><td>EDMA_CS (Out)</td></tr><tr><td>HSDI_SIG9</td><td>O</td><td>N/A (drives high)</td><td>1284_BUSY (Out)</td><td>EDMA_WR (Out)</td></tr><tr><td>HSDI_STATUS[1:0]</td><td>O</td><td>00</td><td>1x (see IEEE 1284 Interface)</td><td>01</td></tr></table></div> <p>AV7110 Preview at 60 tbl. 28; <i>see also id.</i> tbl. 29 (listing different types of DMA transfers allowed for data ports).</p>	PIN NAME	I/O	IEEE 1394 I/F	IEEE 1284 I/F	EXTERNAL DMA	HSDI_DATA[7:0]	I/O	BDI[7:0] (In/Out)	1284_D[7:0] (In/Out)	EDMA_DB[7:0] (In/Out)	HSDI_SIG1	O	BDIRW (Out)	1284_ERROR (Out)	EDMA_RD (Out)	HSDI_SIG2	O	BDIEN (Out)	1284_ACK (Out)	EDMA_DACK (Out) <sup>†</sup>	HSDI_SIG3	I or O	BDAVAIL (In)	1284_STROBE (In)	EDMA_A[3] (Out)	HSDI_SIG4	I/O, I or O	BDIF[2] (In/Out)	1284_SLCTIN (In)	EDMA_A[2] (Out)	HSDI_SIG5	I/O, I or O	BDIF[1] (In/Out)	1284_AF (In)	EDMA_A[1] (Out)	HSDI_SIG6	I/O or O	BDIF[0] (In/Out)	1284_SLT (Out)	EDMA_A[0] (Out)	HSDI_SIG7	I	BDIRQ (In)	1284_INIT (In)	EDMA_DREQ (In) <sup>†</sup>	HSDI_SIG8	O	N/A (drives high)	1284_PEND (Out)	EDMA_CS (Out)	HSDI_SIG9	O	N/A (drives high)	1284_BUSY (Out)	EDMA_WR (Out)	HSDI_STATUS[1:0]	O	00	1x (see IEEE 1284 Interface)	01
PIN NAME	I/O	IEEE 1394 I/F	IEEE 1284 I/F	EXTERNAL DMA																																																									
HSDI_DATA[7:0]	I/O	BDI[7:0] (In/Out)	1284_D[7:0] (In/Out)	EDMA_DB[7:0] (In/Out)																																																									
HSDI_SIG1	O	BDIRW (Out)	1284_ERROR (Out)	EDMA_RD (Out)																																																									
HSDI_SIG2	O	BDIEN (Out)	1284_ACK (Out)	EDMA_DACK (Out) <sup>†</sup>																																																									
HSDI_SIG3	I or O	BDAVAIL (In)	1284_STROBE (In)	EDMA_A[3] (Out)																																																									
HSDI_SIG4	I/O, I or O	BDIF[2] (In/Out)	1284_SLCTIN (In)	EDMA_A[2] (Out)																																																									
HSDI_SIG5	I/O, I or O	BDIF[1] (In/Out)	1284_AF (In)	EDMA_A[1] (Out)																																																									
HSDI_SIG6	I/O or O	BDIF[0] (In/Out)	1284_SLT (Out)	EDMA_A[0] (Out)																																																									
HSDI_SIG7	I	BDIRQ (In)	1284_INIT (In)	EDMA_DREQ (In) <sup>†</sup>																																																									
HSDI_SIG8	O	N/A (drives high)	1284_PEND (Out)	EDMA_CS (Out)																																																									
HSDI_SIG9	O	N/A (drives high)	1284_BUSY (Out)	EDMA_WR (Out)																																																									
HSDI_STATUS[1:0]	O	00	1x (see IEEE 1284 Interface)	01																																																									
[1h] a bus arbiter; and	<p>AV7110 Preview discloses or at least renders obvious a bus arbiter. For example:</p> <p>“prioritized interrupt Interrupt requests are generated from internal modules like the TPP, OSD, A/V decoder, communication processor, and devices on the extension bus. Some of the requests are for data transfers to internal RAM, while others are true interrupts to the ARM CPU. The TC handles data transfers to internal RAM, while others are true interrupts to the ARM CPU. The TC handles data transfers, and the ARM provides services to true interrupts. The</p>																																																												

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	<p>interrupts are grouped into FIQs and IRQs. The firmware will use FIQs, while the application software will use IRQs. The priorities for FIQs are managed by the firmware while those of IRQ are managed by the application software.” AV7110 Preview at 19.</p> <p>“video/audio buffer monitoring support The TC continuously monitors the fullness of the video and audio input buffers. If overflow or underflow occurs, a maskable FIQ interrupt will be used to alert the firmware so that corrective action can be taken in a timely manner. Alternatively, user software can periodically inspect (read access) the read/write pointers of the circular video and audio input buffers and take preemptive actions if overflow/underflow is deemed imminent. Moreover, the TC also keeps the number of bytes of video data being sent to the video decoder in a wrap-around counter. This byte-count is used by the firmware for accurate video PTS synchronization.” AV7110 Preview at 20.</p> <p>“interrupts There are three external interrupt lines on the extension bus of the 'AV7110. Each interrupt has a dedicated acknowledge pin (EXTACK[2:0]). One additional interrupt, BDIRQ (HSDI_ SIG7), is dedicated to the 1394 interface and it has no associated acknowledge signal. All the interrupts generate IRQ to the ARM and user application software needs to provide their service routine. These interrupts are handled by a centralized interrupt controller. The interrupt mask and priority are managed by the firmware. The BDIRQ and three extension bus interrupts are connected to a total of four different IRQs. When the interrupt handler on the ARM begins servicing one of the extension bus IRQs, it should first issue the corresponding acknowledge signal. At the completion of the IRQ, the ARM should reset the acknowledge signal.” AV7110 Preview at 53.</p> <p>“high speed data interface (HSDI) The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device. Logic for these three interfaces share signal pins and hence only one can be active at any given time. Table 28 shows the pin definitions for the HSDI in its various configurations. Switching from one interface to another will require a predefined sequence of API calls. Two signal pins (HSOI_ STATUS[1 :0J) indicate which of the three interfaces is active. They can be used to control external logic for interface arbitration. The definition of these signals is shown at the bottom of Table 28.” AV7110 Preview at 60.</p>



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	<div><p><b>Table 28. High Speed Data Interface Signal Pin Assignment</b></p><table><tr><th>PIN NAME</th><th>I/O</th><th>IEEE 1394 I/F</th><th>IEEE 1284 I/F</th><th>EXTERNAL DMA</th></tr><tr><td>HSDI_DATA[7:0]</td><td>I/O</td><td>BDI[7:0] (In/Out)</td><td>1284_D[7:0] (In/Out)</td><td>EDMA_DB[7:0] (In/Out)</td></tr><tr><td>HSDI_SIG1</td><td>O</td><td>BDIRW (Out)</td><td>1284_ERROR (Out)</td><td>EDMA_RD (Out)</td></tr><tr><td>HSDI_SIG2</td><td>O</td><td>BDIEN (Out)</td><td>1284_ACK (Out)</td><td>EDMA_DACK (Out)<sup>†</sup></td></tr><tr><td>HSDI_SIG3</td><td>I or O</td><td>BDAVAIL (In)</td><td>1284_STROBE (In)</td><td>EDMA_A[3] (Out)</td></tr><tr><td>HSDI_SIG4</td><td>I/O, I or O</td><td>BDIF[2] (In/Out)</td><td>1284_SLCTIN (In)</td><td>EDMA_A[2] (Out)</td></tr><tr><td>HSDI_SIG5</td><td>I/O, I or O</td><td>BDIF[1] (In/Out)</td><td>1284_AF (In)</td><td>EDMA_A[1] (Out)</td></tr><tr><td>HSDI_SIG6</td><td>I/O or O</td><td>BDIF[0] (In/Out)</td><td>1284_SLT (Out)</td><td>EDMA_A[0] (Out)</td></tr><tr><td>HSDI_SIG7</td><td>I</td><td>BDIRQ (In)</td><td>1284_INIT (In)</td><td>EDMA_DREQ (In)<sup>†</sup></td></tr><tr><td>HSDI_SIG8</td><td>O</td><td>N/A (drives high)</td><td>1284_PEND (Out)</td><td>EDMA_CS (Out)</td></tr><tr><td>HSDI_SIG9</td><td>O</td><td>N/A (drives high)</td><td>1284_BUSY (Out)</td><td>EDMA_WR (Out)</td></tr><tr><td>HSDI_STATUS[1:0]</td><td>O</td><td>00</td><td>1x (see IEEE 1284 Interface)</td><td>01</td></tr></table></div> <p>AV7110 Preview at 60 tbl. 28; <i>see also id.</i> tbl. 29 (listing different types of DMA transfers allowed for data ports).</p> <p>“IEEE 1394 interface</p> <p>On power-up the IEEE 1394 interface is enabled on the HSDI. An API call can be used to configure the HSDI for another mode or to return to the 1394 interface if necessary. To complete the 1394 implementation, the 'AV7110 requires an external packetizer and link layer controller, and a physical layer device. Figure 26 shows the connection between the 'AV7110 and these devices.” AV7110 Preview at 62; <i>see id.</i> at fig. 26.</p> <p>“IEEE 1284 interface</p> <p>The IEEE 1284 interface on the 'AV7110 has the following characteristics:</p> <ul style="list-style-type: none"><li>• Supports transfer of up to 10 Mbits/sec</li><li>• Supports the compatibility, nibble and byte mode</li><li>• Supports the ECP mode except for run length coding compression</li><li>• Does not support the EPP mode</li><li>• Peripheral mode only</li></ul> <p>The IEEE 1284 interface is used to connect the 'AV7110 to an external host. The 'AV7110 side of the protocol</p>	PIN NAME	I/O	IEEE 1394 I/F	IEEE 1284 I/F	EXTERNAL DMA	HSDI_DATA[7:0]	I/O	BDI[7:0] (In/Out)	1284_D[7:0] (In/Out)	EDMA_DB[7:0] (In/Out)	HSDI_SIG1	O	BDIRW (Out)	1284_ERROR (Out)	EDMA_RD (Out)	HSDI_SIG2	O	BDIEN (Out)	1284_ACK (Out)	EDMA_DACK (Out) <sup>†</sup>	HSDI_SIG3	I or O	BDAVAIL (In)	1284_STROBE (In)	EDMA_A[3] (Out)	HSDI_SIG4	I/O, I or O	BDIF[2] (In/Out)	1284_SLCTIN (In)	EDMA_A[2] (Out)	HSDI_SIG5	I/O, I or O	BDIF[1] (In/Out)	1284_AF (In)	EDMA_A[1] (Out)	HSDI_SIG6	I/O or O	BDIF[0] (In/Out)	1284_SLT (Out)	EDMA_A[0] (Out)	HSDI_SIG7	I	BDIRQ (In)	1284_INIT (In)	EDMA_DREQ (In) <sup>†</sup>	HSDI_SIG8	O	N/A (drives high)	1284_PEND (Out)	EDMA_CS (Out)	HSDI_SIG9	O	N/A (drives high)	1284_BUSY (Out)	EDMA_WR (Out)	HSDI_STATUS[1:0]	O	00	1x (see IEEE 1284 Interface)	01
PIN NAME	I/O	IEEE 1394 I/F	IEEE 1284 I/F	EXTERNAL DMA																																																									
HSDI_DATA[7:0]	I/O	BDI[7:0] (In/Out)	1284_D[7:0] (In/Out)	EDMA_DB[7:0] (In/Out)																																																									
HSDI_SIG1	O	BDIRW (Out)	1284_ERROR (Out)	EDMA_RD (Out)																																																									
HSDI_SIG2	O	BDIEN (Out)	1284_ACK (Out)	EDMA_DACK (Out) <sup>†</sup>																																																									
HSDI_SIG3	I or O	BDAVAIL (In)	1284_STROBE (In)	EDMA_A[3] (Out)																																																									
HSDI_SIG4	I/O, I or O	BDIF[2] (In/Out)	1284_SLCTIN (In)	EDMA_A[2] (Out)																																																									
HSDI_SIG5	I/O, I or O	BDIF[1] (In/Out)	1284_AF (In)	EDMA_A[1] (Out)																																																									
HSDI_SIG6	I/O or O	BDIF[0] (In/Out)	1284_SLT (Out)	EDMA_A[0] (Out)																																																									
HSDI_SIG7	I	BDIRQ (In)	1284_INIT (In)	EDMA_DREQ (In) <sup>†</sup>																																																									
HSDI_SIG8	O	N/A (drives high)	1284_PEND (Out)	EDMA_CS (Out)																																																									
HSDI_SIG9	O	N/A (drives high)	1284_BUSY (Out)	EDMA_WR (Out)																																																									
HSDI_STATUS[1:0]	O	00	1x (see IEEE 1284 Interface)	01																																																									

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	<p>can be handled by an IEEE 1284 peripheral interface controller on the chip such as the SN54ACT1284/SN? 4ACT1284. Since the signals on the HSDI are 5-V-tolerant, they can be connected directly to this external 1284 driver.” AV7110 Preview at 69; see id. fig.33; see also id. at 69-70.</p> <div> <p>Figure 26. 1394 Interface</p> </div> <p>AV7110 Preview at 62; <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) C packets to and from the internal data RAM. This data can then be processed by the user software as needed.”); <i>see also id.</i> at 63 (listing signals associated with the 1394 interface).</p>
[1i] a multimedia data stream processor; and	<p>AV7110 Preview discloses or at least renders obvious a multimedia data stream processor. For example:</p> <p>“The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or</p>

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	<p>containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.” AV7110 Preview at 13.</p> <p>“Together with the ARM, the TPP also handles program clock reference (PCR) recovery with an external VCXO. The TPP will latch and transfer to the ARM its internal system clock upon the arrival of any packet which contains a PCR. After further processing on the packet and identifying the system clock, the ARM calculates the difference between the system clock from a bit-stream and the actual system clock at the time the packet arrives. Then, the ARM filters the difference and sends it through an 8-bit sigma-delta DAC to control the external VCXO. The ARM will drive the VCXO to its center frequency during start-up or, if enabled by an API, after channel change when there is no incoming PCR.” AV7110 Preview at 13; see also id. at 22-23.</p>  <p>The diagram illustrates a system architecture. At the top left, a 'Transport Bitstream From Front End' enters a 'TPP' (Traffic Processing Processor) block. The TPP is connected to an 'HSDI' block containing '1394 I/F', '1284 I/F', and 'Ext DMA'. The TPP also connects to a 'Traffic Controller' block. Between the TPP and the Traffic Controller is an 'ECD' (Error Correction Decoder) block. The Traffic Controller is connected to 'External System Memory'. Below the Traffic Controller is a 'Video Decoder' block, which connects to an 'Audio Decoder' block. The Audio Decoder has two outputs: 'PCM Audio Output' and 'SPDIF Output'. The Video Decoder connects to an 'OSD' (On-Screen Display) block, which then connects to an 'NTSC/PAL Encoder'. The encoder has two outputs: 'Digital Video Output' and 'Y/C or RGB and Composite Video'. A central horizontal bus connects the Traffic Controller, External System Memory, Video Decoder, Audio Decoder, and the bottom components. The bottom components include a 'Communication Processor' (with inputs for 'GPIO', 'IR', 'JTAG', 'UART (Three)', 'Smart Card', and '12C'), an 'Extension Bus Interface', 'ARM/Thumb', 'Data RAM', and 'ROM'.</p> <p>AV7110 Preview at 12 fig. 1.</p>

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	<p>“MPEG transport decoder (TPP)  TPP module  features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15  Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32  Maximum number of pairs of keys for the descrambler ..... 16  Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the</p>

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	<p>CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination. The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“conditional access and descrambling processing  The 'AV7110 contains a full implementation of the ECD hardware.  The descrambling of the incoming data is performed automatically with minimum intervention by the CPU. The TPP module detects which transport packets are scrambled, at either the program elementary stream (PES) or the transport stream level, and routes the data through the ECD as necessary. The ECD stores the descrambler keys locally and automatically selects the correct key of a specific PID. Up to 16 sets of keys are stored in the key table for use by the ECD. It is possible for more than one PIO to use the same key. The descrambler keys are derived by the conditional access software using the command packet from the bit-stream.” AV7110 Preview at 23.</p>

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	<div> <p style="text-align: center;"><b>Figure 26. 1394 Interface</b></p> </div> <p>AV7110 Preview at 62; <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) C packets to and from the internal data RAM. This data can then be processed by the user software as needed.”); <i>see also id.</i> at 63 (listing signals associated with the 1394 interface).</p> <p>“communication processor features</p> <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> <li>• Provides 3 general purpose UARTs - two at up to 115.2 Kbps and one at up to 9.6 Kbps</li> <li>• Accepts IR input signals</li> <li>• Generates IR output signals</li> <li>• Provides up to nine general purpose I/Os</li> <li>• Manages 12C and JTAG interfaces</li> </ul> <p>This module contains a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR, and 12C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM CPU. Interrupts are used to communicate between these interface modules and the ARM CPU.”</p>

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	<p>AV7110 Preview at 72; <i>see generally id.</i> at 72-78 (describing different functions and functional blocks of the communication processor).</p> <p>“UARTs The 'AV7110 includes three general purpose UARTs that are memory mapped and fully accessible by user application programs. A set of APIs exists to assist in programming them. The output of the UARTs are digital and require external level shifters for RS232 compliance. These UARTs support full duplex mode and are double buffered with sufficient FIFO space to minimize the interrupt frequency to the ARM even when they are operating at their maximum transmission speeds. UART 1 and 2 support handshaking through RTS and CTS signals. They work with baud rates of 1200, 2400, 4800, 9600, 14,400, 19,200, 28,800, 57,600 and 115,200 bps. These two UARTs transmit/receive 1 start bit, 7 or 8 data bits, optional parity, and 1 or 2 stop bits. UART 3 has no support for hardware handshaking, it works with baud rates of 1200, 2400, 4800, 9600 bps. It is possible for the user application software to implement software handshaking with any of the UARTs. The UARTs are fully accessible using the API and can generate interrupts when data is received or the transmit buffer is empty. The CPU also has access to a status register for each UART that contains flags for such errors as data overrun or framing errors.” AV7110 Preview at 75.</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SDRAM, and produces three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs. After being configured and activated by the ARM CPU, the OSD module reads OSD data and mixes it with the video output. The CPU is responsible for turning on and off OSD operations. The bitBLT hardware which is attached to the OSD module provides acceleration for memory block moves and graphics operations.” AV7110 Preview at 33; <i>see id.</i> (showing block diagram of the OSD module).</p>
[1j] a storage subsystem connected to said media switch, wherein multimedia data are stored on said storage subsystem and retrieved from	<p>AV7110 Preview discloses or at least renders obvious a storage subsystem connected to said media switch, wherein multimedia data are stored on said storage subsystem and retrieved from said storage subsystem essentially simultaneously. For example:</p> <p>“After removing packet headers and other system related information, both audio and video data is stored in the</p>

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said storage subsystem essentially simultaneously.	<p>external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards. The chip decodes MPEG-1 and MPEG-2 main profile at main level for video and Layer I and II MPEG-1 and MPEG-2 stereo for audio. Both video and audio decoders synchronize their presentation of reconstructed data using the transmitted presentation time stamps (PTS) and their local system clock. The local system clock is continuously updated by the ARM.” AV7110 Preview at 13.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APis, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PIO table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.</p> <p>The only difference between the two scenarios is that in the case where there is no TPP traffic, the TPP buffer pool can be used. In the case where there is active TPP data, a general purpose buffer needs to be used. Additionally, when TPP data traffic is active, the end of packet (EOP) interrupt generation will require an indication data type configured in the header, which describes where the data to be processed is to be found.” AV7110 Preview at 21.</p> <p>“trick mode When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur.</p>



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	<p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error <ul style="list-style-type: none"> <li>• Continuously displays the decoded I frame.”</li> </ul> </li> </ul> <p>AV7110 Preview at 26; <i>see id.</i> tbl. 6 (showing video decoder commands enabling trick mode functionality).</p> <p>“The HSDI supports the following concurrent data transfers.</p> <ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/program to 1394 (using dedicated I/F - see NOTE XXXX of Table 29)</li> <li>• TPP/program to decoder; 1394/DMA to/from memory</li> <li>• TPP/program to decoder; memory/DMA to/from HSDI</li> <li>• TPP/program to decoder; TPP/DMA to HSDI</li> <li>• TPP/program to decoder; TPP/program to 1394; memory/DMA to/from 1394</li> <li>• TPP/program to decoder; 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; TPP/DMA to 1394” AV7110 Preview at 61.</li> </ul> <div> <p><b>Figure 25. Functional Block Diagram of High Speed Data Interface</b></p> </div> <p>AV7110 Preview at 61 (showing the functional blocks of the HSDI); <i>see also id.</i> at 62-65 (showing describing AV7110’s reading and writing of data from/to the 1394 interface).</p> <p>“AV7110 internal data path for 1394</p>

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	<p>In recording mode, the 'AV7110 sends either encrypted or clean packets to the 1394 interface. The packet will be transferred as soon as it arrives. When recording encrypted data, the ECD module is bypassed. In the case of recording decrypted byte, the TPP sends the encrypted part of the payload to the ECD module, and then forwards each byte to the 1394 interface. No CPU processing is done to the packet during recording. The TPP automatically modifies the header if the packet is decrypted.</p> <p>Note that the same bit stream cannot be sent to the 1394 interface twice (such as, once after decryption, and twice as part of a full transport stream with the by-pass capability). Both Timon and the 'AV7110 support only one MPEG-2 transport stream channel on the bulky data interface.</p> <p>During playback mode, MPEG-2 transport packets coming from the 1394 interface go directly to the TPP module. Figure 29 shows the functional block diagram of the data flow between the TPP, ECD, and 1394 interface. Note that the major portion of the 1394 interface function is implemented in the HSDI module. Dedicated data lines are used for the 1394 interface that allows the 'AV7110 to work in different modes.</p> <ul style="list-style-type: none"> <li>• Decode/decrypt/display one channel and record it</li> <li>• Decode/decrypt/display one channel and record it encrypted (pay-per-view)</li> <li>• Decode/display one channel while recording all or part of 32 PIDs from a transponder, with each selected PIDs either encrypted or decrypted. In addition non selected PIDs can also be recorded in their original format (decryption is not possible for non selected PIDs).</li> <li>• While the TPP is receiving MPEG-2 data from the 1394 port, the 'AV7110 can also record part of the bit stream it is receiving to the 1394 port</li> <li>• Send the whole transport stream from the FEC to the 1394 port without any filtering or decryption and, at the same time, decode/decrypt/display a program from either the same transport stream or from another transport stream received through the 1394 port..” AV7110 Preview at 65.</li> </ul>

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	<div> <p>Figure 25. 1394 Data Flow Block Diagram</p> </div> <p>AV7110 Preview at 69 fig. 25 (showing functional block diagram of data flow between TPP, ECD, and 1394 interface).</p> <p>“Since there is only an 8-bit bus on the HSDI, the ESC is limited to an 8-bit, single bus architecture so its mode selection inputs should be set to mode 0. The upper data bits can be left floating since they have internal pullups on the ESC. Likewise, the AD<sup>?</sup>-0 inputs of the ESC will not be used for this mode and can be left unconnected. The ESC requires an external clock source from 10 MHz to 40 MHz. Since the CLK40 signal of the 'AV7110 is actually a 40.5 MHz clock it cannot be used directly for this controller without violating its specification. Table 32 shows the signals needed for the EDMA interface.” AV7110 Preview at 66; <i>see id.</i> tbl. 32 (listing EDMA interface signals).</p> <p>“When configured for EDMA operation (HSDI_ STATUS[1 LO] = 01), the HSDI is capable of a glue less connection to an external enhanced SCSI controller (ESC) device such as the NCR 53CF94-1 /53CF96-1. Figure 30 shows the connections for this example configuration.</p> <p>. . . .</p> <p>All data transfers (using the HSDI DMA unit) as well as external controller communications (using the A[3:0] output signals), are controlled by the firmware. Firmware will handle MPEG-2 program stream and MPEG-1 system stream input. This firmware will not be available with the initial samples of the 'AV7110. The other input data formats will be handled by user application software. This includes specific interfaces such as the ESC. Table 33 details the EDMA register which allows the user to configure the wait states and other factors of the EDMA port.” AV7110 Preview at 66, 67.</p>

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	<div> <p>Figure 26. 1394 Interface</p> </div> <p>AV7110 Preview at 62; <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) C packets to and from the internal data RAM. This data can then be processed by the user software as needed.”); <i>see also id.</i> at 63 (listing signals associated with the 1394 interface).</p> <p>“The application software interfaces with the peripheral interface controller via RTSL API calls. To send data to the host the application software will issue an API call to transfer the data from memory to the peripheral interface via a DMA. To receive data from the host, the application software will issue an API to transfer a predetermined number of bytes from the peripheral interface to internal data memory via the HSDI DMA unit. The user application software must have a way to determine the number of bytes of data that is expected from the host.” AV7110 Preview at 70.</p> <p>“Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM, and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the</p>

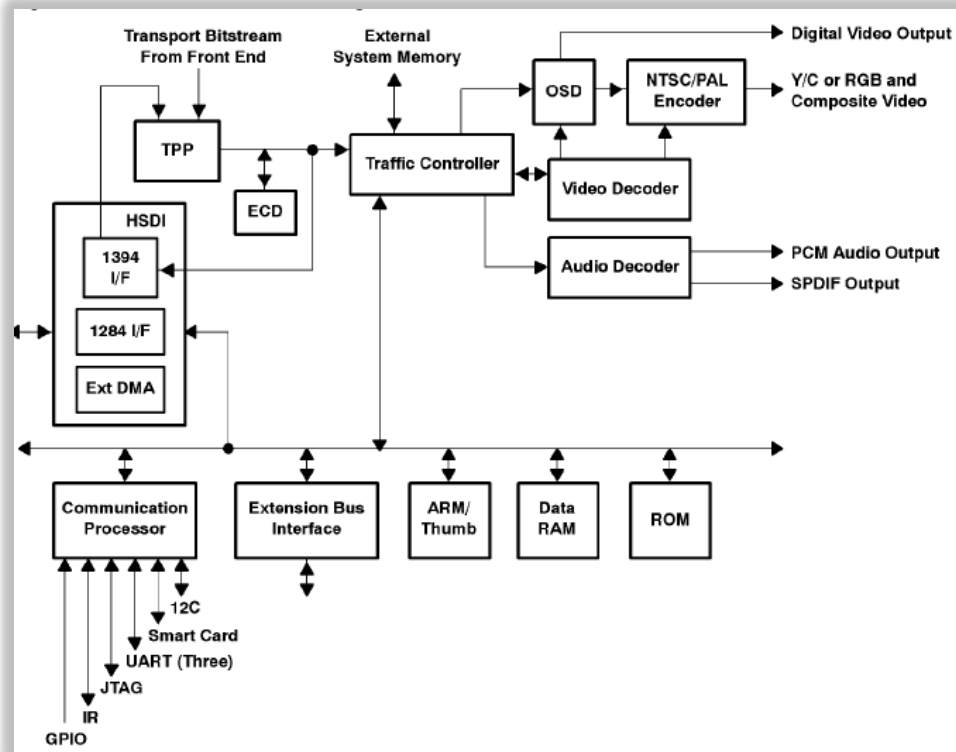
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	<p>FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.</p> <p>....</p> <p>After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards. The chip decodes MPEG-1 and MPEG-2 main profile at main level for video and Layer I and II MPEG-1 and MPEG-2 stereo for audio. Both video and audio decoders synchronize their presentation of reconstructed data using the transmitted presentation time stamps (PTS) and their local system clock. The local system clock is continuously updated by the ARM.” AV7110 Preview at 13.</p> <p>“The SDRAM must be 16-bits wide. The 'AV7110 provides control signals for up to two SDRAMs. Any combination of 4 or 16 Mbit SDRAMs may be used, provided they total at least 16 Mbits. The SDRAM must operate at an 81 MHz clock frequency and have the same timing parameters as the TI TMS626162, a 16 Mbit SDRAM. Other supported sizes and configurations are:</p> <p>16 Mbit → one 16 Mbit SDRAM  20 Mbit → one 16 Mbit and one 4 Mbit SDRAM  32 Mbit → two 16 Mbit SDRAM</p> <p>The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 2D macroblock. The interface also supports decrement mode for bitBLT block transfers.</p> <p>....</p> <p>During DVB decoding, the 'AV7110 allocates the 16 Mbit SDRAM for PAL mode according to the default layout shown in Table 2. All the address pointers of the SDRAM partitioning are user programmable and hence the actual layout can be customized according to needs.” AV7110 Preview at 19.</p> <p>“memory usage reduction</p> <p>In the minimum memory configuration, the 'AV7110 is designed to work with two memory devices: a single 16 Mbit SDRAM device for system data storage (audio, video data, etc.) and a 4 Mbit DRAM for local data storage (private data, SI information, etc.). Table 11 shows what the two memories are used for, in bytes. The amount of memory available for OSD applications depends upon the mode of operation of the 'AV7110. For example, if the letterbox display format is used, more memory is required to store B frames and hence less OSD space will be available.” AV7110 Preview at 30.</p>

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	<p>“Figure 27 shows the functionality of the interface signals when the 'AV7110 reads data from Timon. The maximum input rate of MPEG-2 data coming from Timon and routed through the transport stream hardware demultiplexer block (TPP) is approximately 64.8 Mbits/second. The maximum input bit rate over one transport packet is 60 Mbits/second.</p> <p>....</p> <p>When the 'AV7110 writes data to Timon (record mode), it drives BDIF, BDIEN, and BDIRW for one clock (system) period. BDIEN is driven low for only one byte and must be driven high between two byte transmissions. This is shown in Figure 28.” AV7110 Preview at 64; <i>see also id.</i> figs. 27-28.</p> <p><i>See also claim 1 at 1f, supra.</i></p>
Claim 12	
<p>12. The system of claim 1, said output section further comprising a transport interface, wherein said transport interface receives said transport stream from said input section.</p>	<p>AV7110 Preview discloses or at least renders obvious “said output section further comprising a transport interface, wherein said transport interface receives said transport stream from said input section.” For example:</p> <p>“MPEG transport decoder (TPP) TPP module features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15  Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32  Maximum number of pairs of keys for the descrambler ..... 16  Recording mode through 1394 interface</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination.</p> <p>The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“transport parser input interface</p> <p>The 'AV7110 accepts DVB transport packet data from a front end such as a Forward Error Correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB Conditional Access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23; see also id. at 24 tbl. 4 (describing transport packet input interface pin description).</p>

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See AV7110 Preview at 1 (“[TMS320AV7110] [a]ccepts Transport bit-streams of Up to 72.8Mbps Burst Rate (60 Mbps average Over One Transport Packet.”).

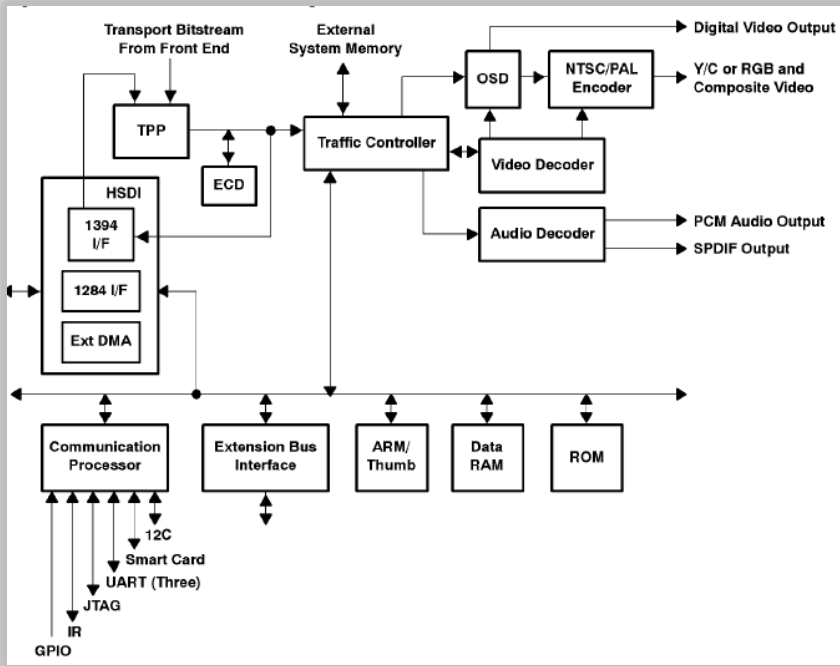


AV7110 Preview at 12 fig. 1.

See also claim 1 at 1a, 1b, and 1j, *supra*.

**Claim 13**



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<p>13. The system of claim 12, said decoder further comprising a transport stream decoder/graphics subsystem.</p>	<p>AV7110 Preview discloses or at least renders obvious “said decoder further comprising a transport stream decoder/graphics subsystem.” For example:</p>  <p>AV7110 Preview at 12 fig. 1.</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SDRAM, and produces three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs. After being configured and activated by the ARM CPU, the OSD module reads OSD data and mixes it with the video output. The CPU is responsible for turning on and off OSD operations. The bitBLT hardware which is attached to the OSD module provides acceleration for memory block moves and graphics operations.” AV7110 Preview at 33; <i>see also id.</i> fig. 8 (showing block diagram of the OSD module); <i>id.</i> at 36 fig. 9 (showing use of OSD_ACTIVE signal for external analog video).</p>

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	<p>“MPEG transport decoder (TPP)  TPP module  features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15 Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32  Maximum number of pairs of keys for the descrambler ..... 16  Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.  Transport packets containing only audio or video payloads are automatically transferred to the proper external</p>

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	<p>SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination. The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“video output interfaces analog video output - NTSC/PAL encoder module</p> <ul style="list-style-type: none"> <li>• Supports NTSC and PAL B, D, G/H, and I display formats</li> <li>• Outputs Y/C or RGB, and composite video with 9-bit DACs</li> <li>• Generates 100/75 format color bar for PAL mode testing</li> <li>• Complies to the RS170A standard</li> <li>• Composite and RGB signals comply with ITU-R BT.470-3 and ITUR BT.471-1</li> <li>• Supports Macro Vision anti-taping function on composite video</li> <li>• Provides sync signals with option to accept external sync signals</li> </ul> <p>The composite video output can be either PAL or NTSC format. The default output format is PAL at powerup. Changing between NTSC and PAL mode can be done via an API which selects the output mode of the NTSC/PAL encoder. Note that the video decoder microcode ROM is specific to NTSC or PAL and required for proper operation.</p> <p>The sync signal pins Vsync and Hsync on the 'AV7110 are defaulted to 3-state mode at powerup, where internally generated sync signals will be used by the NTSC/PAL encoder. The user can then select the source of video sync signals via an API. If internal source is selected then the Vsync and Hsync pins will be configured as output pins. In addition to composite video, the 'AV7110 also provides either an analog S-video (Y - luminance , C - chrominance) signal or an analog RGB output with 720 pixel resolution. All outputs conform to the RS170A standard. Selection of RGB or S-video output is done via API software. Macro Vision version 7 is enabled via an</p>

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	<p>API; the default state is off. A version of the 'AV7110 where the MacroVision anti-taping circuitry is permanently disabled is also available.” AV7110 Preview at 39.</p> <p>“digital video output (not supported when 32-bit EBI is used)</p> <p>PAL mode digital video output</p> <p>The digital output is in 4:2:2 component format. The content of the video could be either pure video or the blended combination of video and OSD. The pin assignments for the digital video output signals are:</p> <p style="padding-left: 40px;">YCOUT(8) 8-bit Cb/Y/Cr/Y data output</p> <p style="padding-left: 40px;">YCCLK(1) 27 MHz clock output</p> <p>The timing of 4:2:2 digital video output is shown in Figure 12.</p> <p>...</p> <p>NTSC mode digital video output</p> <p>The digital output includes video in either 4:4:4 or 4:2:2 component format, plus the aspect ratio VARIS code at the beginning of each video frame. The video output format is programmable by the user but defaults to 4:2:2. The content of the video could be either pure video or the blended combination of video and OSD. The pin assignments for the digital video output signals are:</p> <p style="padding-left: 40px;">YCOUT(8) 8-bit Cb/Y/Cr/Y and VARIS multiplexed data output</p> <p style="padding-left: 40px;">YCCLK(1) 27 MHz clock output</p> <p style="padding-left: 40px;">YCCTRL(2) 2-bit control signals to distinguish between Y/Cb/Cr components and VARIS code</p> <p>The interpretation of YCCTRL is defined in Table 20.</p> <p>...” AV7110 Preview at 41.</p> <p>“PCM audio output</p> <p>The PCM audio output from the 'AV7110 is a serial PCM data line, with associated bit clock (ASCLK) and left/right clock (LRCLK). PCM data is output serially on PCM OUT using the serial clock ASCLK as shown in Figure 15. The data output of PCM OUT alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7110 Preview at 46; <i>see generally id.</i> at 46-47 (describing additional aspects of PCM audio output).</p> <p>“elementary stream playback</p> <p>In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing</p>

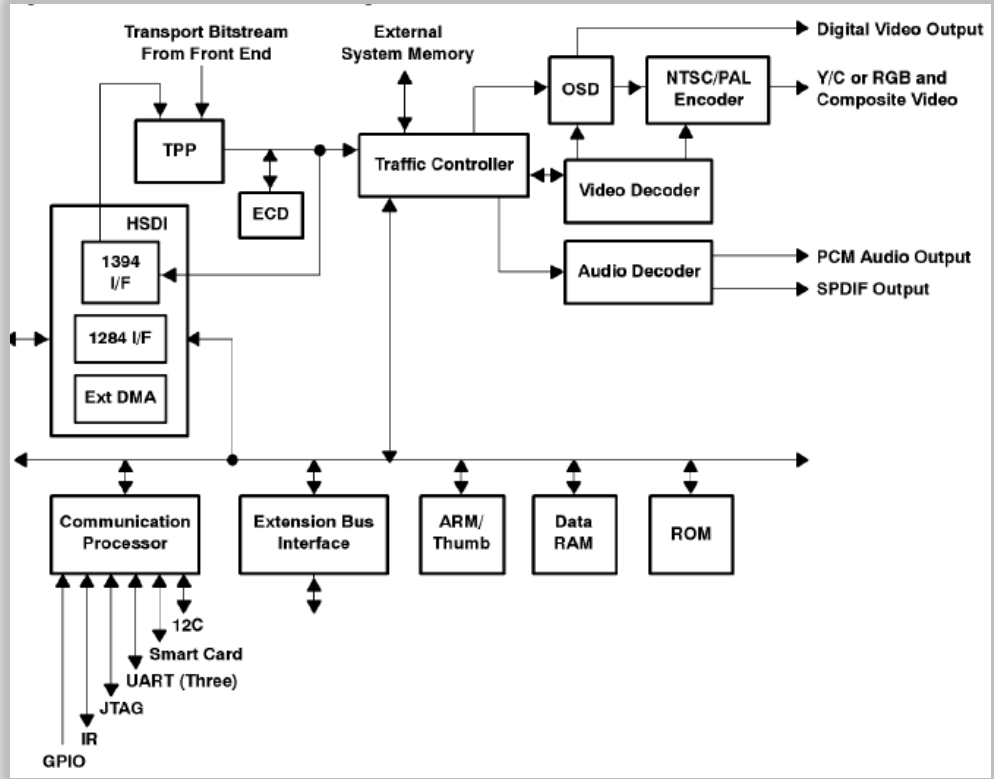
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	<p>off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.</p> <p>SPDIF audio output The SPDIF output conforms to the consumer format of the AES3 standard for serial transmission of digital audio data. When using an external PLL (PCMSRC=1), SPDIF is supported only if Bx over-sampled PCMCLK is supplied (that is, PCMSEL[0]=1).” AV7110 Preview at 48.</p> <p><i>See claim 1 at 1b and 1d, supra.</i></p>
Claim 14	
<p>14. The system of claim 13, wherein said transport stream decoder/graphics subsystem includes any combination of: a host bridge; a memory controller; an MPEG-2 transport demultiplexer; an MPEG-2 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller.</p>	<p>AV7110 Preview discloses or at least renders obvious “said transport stream decoder/graphics subsystem includes any combination of: a host bridge; a memory controller; an MPEG-2 transport demultiplexer; an MPEG-2 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller.” For example:</p> <p><i>See AV7110 Preview at 1 (stating that the AV7110 includes an “On-Chip SDRAM Controller for 16, 20, or 32 Mbit SDRAM”).</i></p> <p>“The SDRAM must be 16-bits wide. The 'AV7110 provides control signals for up to two SDRAMs. Any combination of 4 or 16 Mbit SDRAMs may be used, provided they total at least 16 Mbits. The SDRAM must operate at an 81 MHz clock frequency and have the same timing parameters as the TI TMS626162, a 16 Mbit SDRAM. Other supported sizes and configurations are:</p> <p>16 Mbit → one 16 Mbit SDRAM  20 Mbit → one 16 Mbit and one 4 Mbit SDRAM  32 Mbit → two 16 Mbit SDRAM</p> <p>The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 2D macroblock. The interface also supports decrement mode for bitBLT block transfers.</p> <p>....</p> <p>During DVB decoding, the 'AV7110 allocates the 16 Mbit SDRAM for PAL mode according to the default layout shown in Table 2. All the address pointers of the SDRAM partitioning are user programmable and hence the actual layout can be customized according to needs.” AV7110 Preview at 19.</p>

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	<p>“traffic controller (TC) features</p> <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>• Authorizes and manages DMA transfers</li> <li>• Provides SDRAM interface</li> <li>• Manages extension bus</li> <li>• Provides memory access protection</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> <li>- Audio/video decoder to/from SDRAM</li> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> </ul> </li> <li>• Generates chip selects (CS) for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus</li> <li>• Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.</li> </ul> <p>“Software on the 'AV7110 is divided into three sections: firmware, API, and user software. Firmware is masked into the internal ROM of the 'AV7110. This software is supplied by Texas Instruments (TI™) and is used for low level control of the hardware and bit-stream demultiplexing in the 'AV7110. The user software is resident in external memory and contains all the software written by the user. The user software communicates with the firmware through application programming interfaces (AP Is). These AP Is are contained in external ROM. APIs are written by TI and provided in the form of run time support library (RTSL).” AV7110 Preview at 13.</p> <p>“The 'AV7110 uses the STC and PTS to determine the play back time of the decoded audio and video data. The relationship between STC and PTS is determined at the time of the generation of the generation of the respective elementary streams (ES). Upon reception, the demultiplexing software in the 'AV7110 extracts the video PTS and inserts it in an array of PTS and byte-count information maintained for the video decoder. For the audio the PTS information is extracted by the audio decoder front end from the PES. The video decoder contains an STC counter that is clocked by the system clock (27 MHz) and normalized to a 90 kHz reference. The audio decoder does not</p>

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	<p>contain a counter. Instead, it gets updated from the system time reference counter every 1 .4 ms.” AV7110 Preview at 48.</p> <p>“Figure 27 shows the functionality of the interface signals when the 'AV7110 reads data from Timon. The maximum input rate of MPEG-2 data coming from Timon and routed through the transport stream hardware demultiplexer block (TPP) is approximately 64.8 Mbits/second. The maximum input bit rate over one transport packet is 60 Mbits/second.” AV7110 Preview at 64; <i>see also id.</i> fig. 27.</p> <p>“MPEG transport decoder (TPP)  TPP module  features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15  Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32  Maximum number of pairs of keys for the descrambler ..... 16  Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter</p>

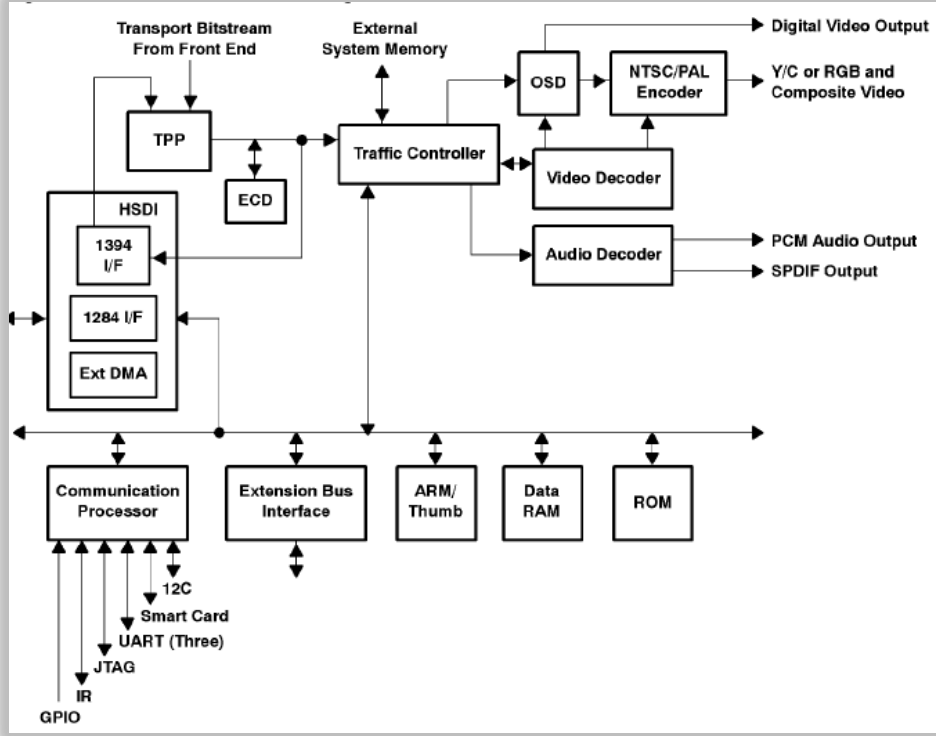
'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination.</p> <p>The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p>



'472 Patent Claim	Exemplary Prior Art Disclosure
	 <p>The diagram illustrates the AV7110 system architecture. At the top left, a 'Transport Bitstream From Front End' enters a 'TPP' (Transport Processing Processor) block. The TPP is connected to an 'HSDI' block containing '1394 I/F', '1284 I/F', and 'Ext DMA'. The HSDI block is connected to a 'Traffic Controller' block. The Traffic Controller is also connected to 'External System Memory' and an 'OSD' (On-Screen Display) block. The OSD is connected to an 'NTSC/PAL Encoder' block, which produces 'Digital Video Output' and 'Y/C or RGB and Composite Video'. The Traffic Controller is also connected to a 'Video Decoder' block, which produces 'PCM Audio Output' and 'SPDIF Output'. The Traffic Controller is connected to a 'Communication Processor' block, which is connected to an 'Extension Bus Interface' block. The Communication Processor is also connected to 'ARM/Thumb', 'Data RAM', and 'ROM' blocks. The Communication Processor is connected to various external interfaces: 'GPIO', 'IR', 'JTAG', 'UART (Three)', 'Smart Card', and '12C'.</p> <p>AV7110 Preview at 12 fig. 1.</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SDRAM, and produces three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs. After being configured and activated by the ARM CPU, the OSD module reads OSD data and mixes it with the video output. The CPU is responsible for turning on and off OSD operations. The bitBLT hardware which is attached to the OSD module provides acceleration for memory block moves and graphics operations.” AV7110 Preview at 33; <i>see also id.</i> fig. 8</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>(showing block diagram of the OSD module); <i>id.</i> at 36 fig. 9 (showing use of OSD_ACTIVE signal for external analog video).</p> <p>“The video decoder module receives a video bit-stream from the SDRAM. It also uses the SDRAM as its working memory to store tables, buffers, and reconstructed images. The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.” AV7110 Preview at 25-26.</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers I and II</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Outputs in both PCM and SPDIF formats</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information</li> <li>• Supports half-frequency modes</li> <li>• Supports playback of 16-bit PCM data (PCM bypass), audio elementary stream, and audio PES</li> <li>• Provides read/write accesses to audio input buffers read/write pointers</li> </ul> <p>The audio module receives MPEG compressed audio data from the TC, decodes it, and outputs audio samples in PCM format. APIs are provided for the ARM CPU to initialize/control the audio decoder via a control register and to read status information from the decoder's status register.</p> <p>Audio frame data and PTS information are stored in the SDRAM in packet form. The audio module decodes the packets to extract the PTS and audio data. The audio decoder uses this PTS value to perform playback synchronization (see Synchronization for more details). It is application software's responsibility to determine and enable the PIO of the MPEG-1 compliant bit-stream in a MPEG-2 audio program which contains both the MPEG-1 compliant bit-stream and the MPEG-2 extension bit-stream.</p> <p>The ARM can control the operation of the audio module via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and over-sampling ratio, and choose the output format for dual channel mode. The ARM will also be able to read status information from the audio module. One 32-bit register</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>provides the MPEG header information and sync, CRC, and PCM status.” AV7110 Preview at 44; see also id. at 45-46 (listing registers used by the audio module).</p> <p><i>See</i> claim 1 at 1b and 1d, and claim 13, <i>supra</i>.</p>
<b>Claim 15</b>	
<p>15. The system of claim 14, said transport stream decoder/graphics subsystem further comprising at least one transport stream interface, wherein said transport stream interface receives said transport stream from said input section.</p>	<p>AV7110 Preview discloses or at least renders obvious said transport stream decoder/graphics subsystem further comprising at least one transport stream interface, wherein said transport stream interface receives said transport stream from said input section. For example:</p> <p><i>See</i> claim 1 at 1b and 1d, and claims 12-14, <i>supra</i>.</p>
<b>Claim 16</b>	
<p>16. The system of claim 14, wherein said transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet streams are stored and played back though [sic] an output side of said transport stream decoder/graphics subsystem.</p>	<p>AV7110 Preview discloses or at least renders obvious “said transport stream is demultiplexed into audio and video packet streams, wherein said audio and video packet streams are stored and played back though [sic] an output side of said transport stream decoder/graphics subsystem.” For example:</p>

'472 Patent Claim	Exemplary Prior Art Disclosure
	 <p>The diagram illustrates the architecture of the TMS320AV7110 integrated set-top box decoder. A central horizontal bus connects various components. On the left, a 'Communication Processor' is connected to the bus and has multiple external interfaces: GPIO, IR, JTAG, UART (Three), Smart Card, and 12C. Above the bus, a 'Traffic Controller' is connected to 'External System Memory' and the bus. To the left of the Traffic Controller is a block containing 'HSDI', '1394 I/F', '1284 I/F', and 'Ext DMA'. A 'Transport Bitstream From Front End' feeds into a 'TPP' (Transport Packet Parser), which connects to the Traffic Controller. Below the Traffic Controller is an 'ECD' (European Common Descrambler). To the right of the Traffic Controller, the bus connects to a 'Video Decoder' and an 'Audio Decoder'. The Video Decoder outputs to an 'OSD' (On-Screen Display) controller and an 'NTSC/PAL Encoder'. The Audio Decoder outputs to 'PCM Audio Output' and 'SPDIF Output'. The OSD controller also outputs to the NTSC/PAL Encoder. The final outputs are 'Digital Video Output' and 'Y/C or RGB and Composite Video' from the NTSC/PAL Encoder. At the bottom, the bus connects to 'ARM/Thumb' processor, 'Data RAM', and 'ROM'.</p> <p>AV7110 Preview at 12 fig. 1.</p> <p>“The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO), and MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infra-red (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.” AV7110 Preview at 1.</p> <p>“transport parser input interface</p>

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	<p>The 'AV7110 accepts DVB transport packet data from a front end such as a Forward Error Correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB Conditional Access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23; see also id. at 24 tbl. 4 (describing transport packet input interface pin description).</p> <p>“The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.” AV7110 Preview at 13.</p> <p>“MPEG transport decoder (TPP)  TPP module  features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15 Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32  Maximum number of pairs of keys for the descrambler ..... 16  Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> </ul>

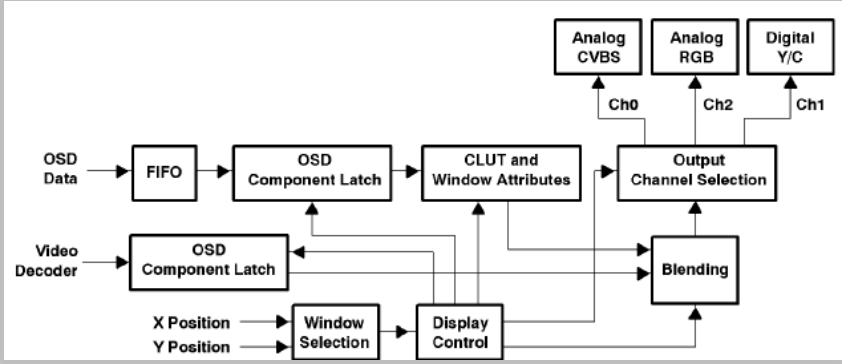
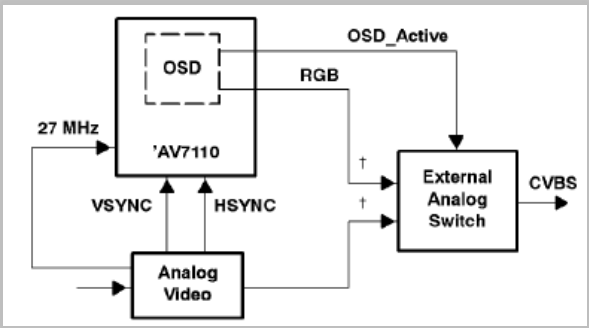
'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination.</p> <p>The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards. The chip decodes MPEG-1 and MPEG-2 main profile at main level for video and Layer I and II MPEG-1 and MPEG-2 stereo for audio. Both video and audio decoders synchronize their presentation of reconstructed data using the transmitted presentation time stamps (PTS) and their local system clock. The local system clock is continuously updated by the ARM.” AV7110 Preview at 13.</p>

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	<p>“video/audio buffer monitoring support The TC continuously monitors the fullness of the video and audio input buffers. If overflow or underflow occurs, a maskable FIQ interrupt will be used to alert the firmware so that corrective action can be taken in a timely manner. Alternatively, user software can periodically inspect (read access) the read/write pointers of the circular video and audio input buffers and take preemptive actions if overflow/underflow is deemed imminent. Moreover, the TC also keeps the number of bytes of video data being sent to the video decoder in a wrap-around counter. This byte-count is used by the firmware for accurate video PTS synchronization.” AV7110 Preview at 20.</p> <p>“Software on the 'AV7110 is divided into three sections: firmware, API, and user software. Firmware is masked into the internal ROM of the 'AV7110. This software is supplied by Texas Instruments (TI™) and is used for low level control of the hardware and bit-stream demultiplexing in the 'AV7110. The user software is resident in external memory and contains all the software written by the user. The user software communicates with the firmware through application programming interfaces (AP Is). These AP Is are contained in external ROM. APIs are written by TI and provided in the form of run time support library (RTSL).” AV7110 Preview at 13.</p> <p>“The interrupt priorities determine the processing sequence, and the demultiplexed input stream packet information determines the data path through the system. There is only minimal inter-process dependency, which eliminates the need for a software control-flow process. Any inter-process dependencies can be handled by proper structuring of the interrupt process in terms of priorities and multi-level processing.” AV7110 Preview at 14.</p> <p>“traffic controller (TC) features</p> <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>• Authorizes and manages DMA transfers</li> <li>• Provides SDRAM interface</li> <li>• Manages extension bus</li> <li>• Provides memory access protection</li> <li>• Manages the data flow between processors and memories</li> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> <li>- Audio/video decoder to/from SDRAM</li> </ul>

'472 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> <li>• Generates chip selects (CS) for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus</li> <li>• Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.</li> </ul> <p>“The video decoder module receives a video bit-stream from the SDRAM. It also uses the SDRAM as its working memory to store tables, buffers, and reconstructed images. The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.</p> <p>The 'AV7110 synchronizes the presentation of video with the audio using the transmitted PTS which are extracted by the ARM from the PES packets. it compares the PTS with the local system time clock (STC) and performs synchronization recovery if the difference is outside of a user programmable threshold range given as follows:</p> $STC - \text{threshold} < PTS < STC + \text{threshold}$ <p>If synchronization recovery is needed, the video decoder will either redisplay or skip a frame, depending on the PTS value. If the PTS lags, that is, the time for displaying the current picture has already passed, the video decoder discards the following B pictures without decoding them until the PTS catches up with the STC. If the PTS leads, that is, the time for displaying the current picture has not arrived yet, the video decoder pauses the decoding and continuously displays the last picture (see Synchronization for more details).” AV7110 Preview at 25-26.</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers I and II</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Outputs in both PCM and SPDIF formats</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information</li> <li>• Supports half-frequency modes</li> </ul>



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	<ul style="list-style-type: none"> <li>• Supports playback of 16-bit PCM data (PCM bypass), audio elementary stream, and audio PES</li> <li>• Provides read/write accesses to audio input buffers read/write pointers</li> </ul> <p>The audio module receives MPEG compressed audio data from the TC, decodes it, and outputs audio samples in PCM format. APIs are provided for the ARM CPU to initialize/control the audio decoder via a control register and to read status information from the decoder's status register.</p> <p>Audio frame data and PTS information are stored in the SDRAM in packet form. The audio module decodes the packets to extract the PTS and audio data. The audio decoder uses this PTS value to perform playback synchronization (see Synchronization for more details). It is application software's responsibility to determine and enable the PIO of the MPEG-1 compliant bit-stream in a MPEG-2 audio program which contains both the MPEG-1 compliant bit-stream and the MPEG-2 extension bit-stream.</p> <p>The ARM can control the operation of the audio module via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and over-sampling ratio, and choose the output format for dual channel mode. The ARM will also be able to read status information from the audio module. One 32-bit register provides the MPEG header information and sync, CRC, and PCM status.” AV7110 Preview at 44; see also id. at 45-46 (listing registers used by the audio module).</p> <p>“The 'AV7110 uses the STC and PTS to determine the play back time of the decoded audio and video data. The relationship between STC and PTS is determined at the time of the generation of the generation of the respective elementary streams (ES). Upon reception, the demultiplexing software in the 'AV7110 extracts the video PTS and inserts it in an array of PTS and byte-count information maintained for the video decoder. For the audio the PTS information is extracted by the audio decoder front end from the PES. The video decoder contains an STC counter that is clocked by the system clock (27 MHz) and normalized to a 90 kHz reference. The audio decoder does not contain a counter. Instead, it gets updated from the system time reference counter every 1 .4 ms.” AV7110 Preview at 48.</p> <p>“elementary stream playback</p> <p>In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.” AV7110 Preview at 48.</p>

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	<p>“The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SDRAM, and produces three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs. After being configured and activated by the ARM CPU, the OSD module reads OSD data and mixes it with the video output. The CPU is responsible for turning on and off OSD operations. The bitBLT hardware which is attached to the OSD module provides acceleration for memory block moves and graphics operations.” AV7110 Preview at 33.</p>  <p>AV7110 Preview at 33 fig. 8 (showing block diagram of the OSD module).</p>  <p>AV7110 Preview at 36 fig. 9.</p>

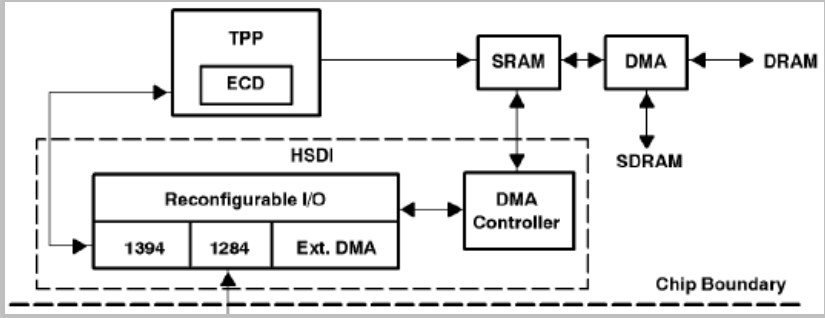
'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>“video output interfaces  analog video output - NTSC/PAL encoder module</p> <ul style="list-style-type: none"> <li>• Supports NTSC and PAL B, D, G/H, and I display formats</li> <li>• Outputs Y/C or RGB, and composite video with 9-bit DACs</li> <li>• Generates 100/75 format color bar for PAL mode testing</li> <li>• Complies to the RS170A standard</li> <li>• Composite and RGB signals comply with ITU-R BT.470-3 and ITUR BT.471-1</li> <li>• Supports Macro Vision anti-taping function on composite video</li> <li>• Provides sync signals with option to accept external sync signals</li> </ul> <p>The composite video output can be either PAL or NTSC format. The default output format is PAL at powerup. Changing between NTSC and PAL mode can be done via an API which selects the output mode of the NTSC/PAL encoder. Note that the video decoder microcode ROM is specific to NTSC or PAL and required for proper operation.</p> <p>The sync signal pins Vsync and Hsync on the 'AV7110 are defaulted to 3-state mode at powerup, where internally generated sync signals will be used by the NTSC/PAL encoder. The user can then select the source of video sync signals via an API. If internal source is selected then the Vsync and Hsync pins will be configured as output pins. In addition to composite video, the 'AV7110 also provides either an analog S-video (Y - luminance , C - chrominance) signal or an analog RGB output with 720 pixel resolution. All outputs conform to the RS170A standard. Selection of RGB or S-video output is done via API software. Macro Vision version 7 is enabled via an API; the default state is off. A version of the 'AV7110 where the MacroVision anti-taping circuitry is permanently disabled is also available.” AV7110 Preview at 39.</p> <p>“digital video output (not supported when 32-bit EBI is used)  PAL mode digital video output</p> <p>The digital output is in 4:2:2 component format. The content of the video could be either pure video or the blended combination of video and OSD. The pin assignments for the digital video output signals are:</p> <p style="padding-left: 40px;">YCOUT(8) 8-bit Cb/Y/Cr/Y data output  YCCLK(1) 27 MHz clock output</p> <p>The timing of 4:2:2 digital video output is shown in Figure 12.</p> <p>...</p> <p>NTSC mode digital video output</p> <p>The digital output includes video in either 4:4:4 or 4:2:2 component format, plus the aspect ratio VARIS code</p>

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	<p>at the beginning of each video frame. The video output format is programmable by the user but defaults to 4:2:2. The content of the video could be either pure video or the blended combination of video and OSD. The pin assignments for the digital video output signals are:</p> <p style="padding-left: 40px;">YCOUT(8) 8-bit Cb/Y/Cr/Y and VARIS multiplexed data output</p> <p style="padding-left: 40px;">YCCLK(1) 27 MHz clock output</p> <p style="padding-left: 40px;">YCCTRL(2) 2-bit control signals to distinguish between Y/Cb/Cr components and VARIS code</p> <p>The interpretation of YCCTRL is defined in Table 20.  . . . .” AV7110 Preview at 41.</p> <p>“PCM audio output  The PCM audio output from the 'AV7110 is a serial PCM data line, with associated bit clock (ASCLK) and left/right clock (LRCLK). PCM data is output serially on PCM OUT using the serial clock ASCLK as shown in Figure 15. The data output of PCM OUT alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7110 Preview at 46; <i>see generally id.</i> at 46-47 (describing additional aspects of PCM audio output).</p> <p>“elementary stream playback  In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.</p> <p>SPDIF audio output  The SPDIF output conforms to the consumer format of the AES3 standard for serial transmission of digital audio data. When using an external PLL (PCMSRC=1), SPDIF is supported only if Bx over-sampled PCMCLK is supplied (that is, PCMSEL[0]=1).” AV7110 Preview at 48.</p> <p>“The data transfer from TPP to the data RAM is done via DMA.  Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM,</p>

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	<p>and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.” AV7110 Preview at 13.</p> <p>“Figure 27 shows the functionality of the interface signals when the 'AV7110 reads data from Timon. The maximum input rate of MPEG-2 data coming from Timon and routed through the transport stream hardware demultiplexer block (TPP) is approximately 64.8 Mbits/second. The maximum input bit rate over one transport packet is 60 Mbits/second.” AV7110 Preview at 64; <i>see id.</i> fig. 27.</p> <p>“The HSDI supports the following concurrent data transfers.</p> <ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/program to 1394 (using dedicated I/F - see NOTE XXXX of Table 29)</li> <li>• TPP/program to decoder; 1394/DMA to/from memory</li> <li>• TPP/program to decoder; memory/DMA to/from HSDI</li> <li>• TPP/program to decoder; TPP/DMA to HSDI</li> <li>• TPP/program to decoder; TPP/program to 1394; memory/DMA to/from 1394</li> <li>• TPP/program to decoder; 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; TPP/DMA to 1394” AV7110 Preview at 61.</li> </ul> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PIO table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA</p>

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	<p>buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.</p> <p>The only difference between the two scenarios is that in the case where there is no TPP traffic, the TPP buffer pool can be used. In the case where there is active TPP data, a general purpose buffer needs to be used.</p> <p>Additionally, when TPP data traffic is active, the end of packet (EOP) interrupt generation will require an indication data type configured in the header, which describes where the data to be processed is to be found.” AV7110 Preview at 21.</p> <p>In recording mode, the 'AV7110 sends either encrypted or clean packets to the 1394 interface. The packet will be transferred as soon as it arrives. When recording encrypted data, the ECD module is bypassed. In the case of recording decrypted byte, the TPP sends the encrypted part of the payload to the ECD module, and then forwards each byte to the 1394 interface. No CPU processing is done to the packet during recording. The TPP automatically modifies the header if the packet is decrypted.</p> <p>Note that the same bit stream cannot be sent to the 1394 interface twice (such as, once after decryption, and twice as part of a full transport stream with the by-pass capability). Both Timon and the 'AV7110 support only one MPEG-2 transport stream channel on the bulky data interface.</p> <p>During playback mode, MPEG-2 transport packets coming from the 1394 interface go directly to the TPP module. Figure 29 shows the functional block diagram of the data flow between the TPP, ECD, and 1394 interface. Note that the major portion of the 1394 interface function is implemented in the HSDI module. Dedicated data lines are used for the 1394 interface that allows the 'AV7110 to work in different modes.</p> <ul style="list-style-type: none"> <li>• Decode/decrypt/display one channel and record it</li> <li>• Decode/decrypt/display one channel and record it encrypted (pay-per-view)</li> <li>• Decode/display one channel while recording all or part of 32 PIDs from a transponder, with each selected PIDs either encrypted or decrypted. In addition non selected PIDs can also be recorded in their original format (decryption is not possible for non selected PIDs).</li> <li>• While the TPP is receiving MPEG-2 data from the 1394 port, the 'AV7110 can also record part of the bit stream it is receiving to the 1394 port</li> <li>• Send the whole transport stream from the FEC to the 1394 port without any filtering or decryption and, at the same time, decode/decrypt/display a program from either the same transport stream or from another transport stream received through the 1394 port..” AV7110 Preview at 65.</li> </ul> <p><i>See claim 1 at 1a, 1b, 1d-1j, and 14, supra.</i></p>

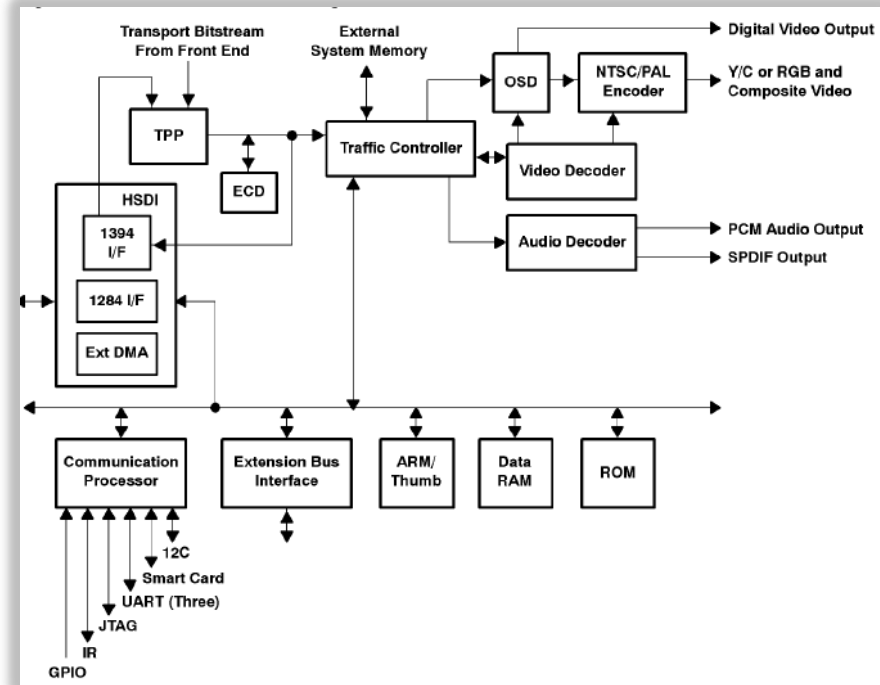
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<b>Claim 20</b>	
<p>20. The system of claim 14, further comprising a SDRAM connected to said transport stream decoder/graphics subsystem.</p>	<p>AV7110 Preview discloses or at least renders obvious a SDRAM connected to said transport stream decoder/graphics subsystem. For example:</p> <p>“Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM, and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.” AV7110 Preview at 13.</p> <p>“The SDRAM must be 16-bits wide. The 'AV7110 provides control signals for up to two SDRAMs. Any combination of 4 or 16 Mbit SDRAMs may be used, provided they total at least 16 Mbits. The SDRAM must operate at an 81 MHz clock frequency and have the same timing parameters as the TI TMS626162, a 16 Mbit SDRAM. Other supported sizes and configurations are:</p> <p style="padding-left: 40px;">16 Mbit → one 16 Mbit SDRAM  20 Mbit → one 16 Mbit and one 4 Mbit SDRAM  32 Mbit → two 16 Mbit SDRAM</p> <p>The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 2D macroblock. The interface also supports decrement mode for bitBLT block transfers.</p> <p>....</p> <p>During DVB decoding, the 'AV7110 allocates the 16 Mbit SDRAM for PAL mode according to the default layout shown in Table 2. All the address pointers of the SDRAM partitioning are user programmable and hence the actual layout can be customized according to needs.” AV7110 Preview at 19.</p> <p>“The video decoder module receives a video bit-stream from the SDRAM. It also uses the SDRAM as its working memory to store tables, buffers, and reconstructed images. The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.” AV7110 Preview at 25-26.</p>

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	<p>“memory usage reduction</p> <p>In the minimum memory configuration, the 'AV7110 is designed to work with two memory devices: a single 16 Mbit SDRAM device for system data storage (audio, video data, etc.) and a 4 Mbit DRAM for local data storage (private data, SI information, etc.). Table 11 shows what the two memories are used for, in bytes. The amount of memory available for OSD applications depends upon the mode of operation of the 'AV7110. For example, if the letterbox display format is used, more memory is required to store B frames and hence less OSD space will be available.” AV7110 Preview at 30.</p> <p>“The video input buffer, which is located in the SDRAM, is made up of three components: a theoretical rate control buffer whose size is specified in the MPEG-2 video standard (229,376 bytes); a buffer space to compensate for the decoder delay (52,000 bytes); and additional storage space to synchronize video decoder's timing with that of the NTSC/PAL encoder's Vsync timing (75,000 bytes). On the 'AV7110, an API is provided to allow user applications to synchronize the video sync pulse to the video decoder timing at channel change. Doing so can potentially recover up to 75,000 bytes (15 Mbps x 40 ms) of storage space for OSD usage. When Vsync reset is activated, the display during channel change is always blank.” AV7110 Preview at 30.</p>  <p>AV7110 Preview at 61 fig. 25 (showing functional block diagram of HSDI).</p>



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AV7110 Preview at 12 fig. 1.

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	<div> <p>Figure 4. Traffic Controller Data Flow</p> </div> <p>AV7110 Preview at 18 fig. 4.</p> <p>See AV7110 Preview at 1 (stating that the AV7110 includes an “On-Chip SDRAM Controller for 16, 20, or 32 Mbit SDRAM”).</p> <p>See claim 1 at 1d and 1j, and claims 12-15, <i>supra</i>.</p>
Claim 22	
<p>22. The system of claim 1, wherein said processor is operative to run system software, middleware, and application software.</p>	<p>AV7110 Preview discloses or at least renders obvious “said processor is operative to run system software, middleware, and application software.” For example:</p> <p>“Software on the 'AV7110 is divided into three sections: firmware, API, and user software. Firmware is masked into the internal ROM of the 'AV7110. This software is supplied by Texas Instruments (TI™) and is used for low</p>

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	<p>level control of the hardware and bit-stream demultiplexing in the 'AV7110. The user software is resident in external memory and contains all the software written by the user. The user software communicates with the firmware through application programming interfaces (AP Is). These AP Is are contained in external ROM. APIs are written by TI and provided in the form of run time support library (RTSL).</p> <p>The 'AV7110s firmware is comprised of a collection of interrupt (FIQ) service routines and supervisor mode run-time support programs. This software isolates the application software from any direct interaction with the hardware. Figure 2 shows the high level block diagram of the complete software system.” AV7110 Preview at 13.</p> <p>“At the lowest level, each hardware component has a firmware module associated with it. A module may consist of:</p> <ul style="list-style-type: none"> <li>Initialization code - executed at processor reset</li> <li>Interrupt Service Routines - executed from interrupt by the associated hardware module.</li> </ul> <p>The run-time support library provides an application programming interface for user software. All run-time modules are written to be invoked from supervisory mode. This prevents software running in user mode from interfering with the built-in firmware.</p> <p>Functionally, the firmware consists of several software processes that are self contained at runtime and operate for the most part, independently and asynchronously. Because of the nature of the processing of a complex input stream, the processes are interrupt driven.</p> <p>The interrupt priorities determine the processing sequence, and the demultiplexed input stream packet information determines the data path through the system. There is only minimal inter-process dependency, which eliminates the need for a software control-flow process. Any inter-process dependencies can be handled by proper structuring of the interrupt process in terms of priorities and multi-level processing.” AV7110 Preview at 13-14.</p>

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	<div> <p style="text-align: center;"><b>Figure 2. Software Block Diagram</b></p> </div> <p>AV7110 Preview at 14 fig. 2.</p> <p>“The ARM CPU is responsible for managing all the hardware and software resources in the 'AV7110. At powerup the ARM verifies the existence and size of external memory. Following that, it initializes all the hardware modules by setting up control registers and tables and then resetting data pointers. It then executes the default firmware from internal ROM and transfers control to the users applications software. A set of run-time library routines provide the access to the firmware and hardware for user application programs. The application programs are stored in external memory attached to the extension bus.</p> <p>During normal operation the ARM constantly responds, based on a programmable priority, to FIQ interrupt requests from any of the hardware modules and devices on the extension bus. The types of interrupt services include transport packet parsing, program clock recovery, traffic controller and OSD service requests, service or</p>

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	<p>data transfer requests from the extension bus and communication processor, and service requests from the audio/video decoder.” AV7110 Preview at 16.</p> <p><i>See claim 1 at 1c, supra.</i></p>
Claim 23	
<p>23. The system of claim 22, wherein said system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components.</p>	<p>AV7110 Preview discloses or at least renders obvious said system software includes at least: an operating system kernel and device drivers, said system software operative to initialize and control hardware components. For example:</p> <div> <p style="text-align: center;"><b>Figure 2. Software Block Diagram</b></p> </div> <p>AV7110 Preview at 14 fig. 2.</p>

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	<p>“ARM CPU Features</p> <ul style="list-style-type: none"> <li>• Runs at 40.5 MHz</li> <li>• Supports byte (8-bit), half-word (16-bit), and word (32-bit) data types</li> <li>• Reads instructions from on-chip ROM or from the extension bus</li> <li>• Can switch between ARM (32-bit) or Thumb (16-bit) instruction mode</li> <li>• 32-bit data and 32-bit address lines</li> <li>• 7 processing modes</li> <li>• Two interrupts, FIQ and I RO</li> </ul> <p>The 32-bit ARM processor running at 40.5 MHz and its associated firmware provide the following:</p> <ul style="list-style-type: none"> <li>• Initialization and management of all hardware modules</li> <li>• Service for selected interrupt generated by hardware modules and I/O ports</li> <li>• Application program interface (API) for users to develop their own applications”</li> </ul> <p>AV7110 Preview at 15.</p> <p>“The 'AV7110 includes an interface to the smart card access control system. The interface consists of a high speed UART and logic to comply with both the ISO 7816-3 and the NOC standards. Both T =0 and T =1 protocols in the ISO 7816-3 standard are supported, but the bit-synchronous protocol is not supported. Applicable firmware drivers to control the interface are also included. Two smart cards can be supported via a smart card select pin which can be set via an API (see Figure 35). Only one smart card can be active at any time and switching from one smart card to another requires a full power down sequence of the active card followed by a full power up sequence on the second card.” AV7110 Preview at 72.</p> <p>“The CPU in the 'AV7110 is a 32-bit RISC processor, the ARM7TDM I/Thumb, which has the capability to execute instructions in 16- or 32-bit format at a clock frequency of 40.5 MHz. The regular ARM instructions are exactly one word (32-bit) long, and the data operations are only performed on word quantities. The LOAD and STORE instructions however, can transfer either byte, half-word or word quantities.” AV7110 Preview at 15.</p> <p>“The ARM CPU is responsible for managing all the hardware and software resources in the 'AV7110. At powerup the ARM verifies the existence and size of external memory. Following that, it initializes all the hardware modules by setting up control registers and tables and then resetting data pointers. It then executes the default firmware from internal ROM and transfers control to the users applications software. A set of run-time library</p>

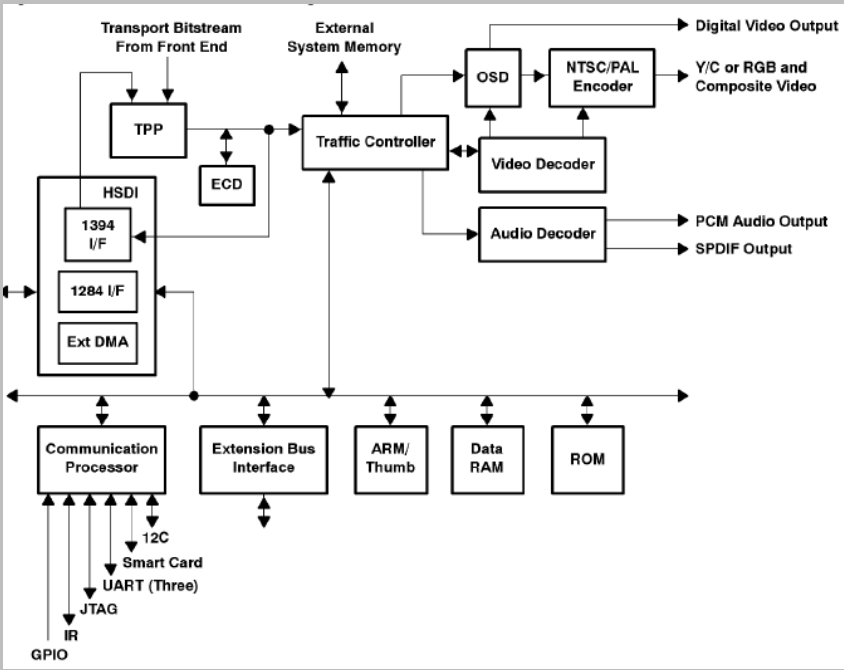
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	<p>routines provide the access to the firmware and hardware for user application programs. The application programs are stored in external memory attached to the extension bus.</p> <p>During normal operation the ARM constantly responds, based on a programmable priority, to FIQ interrupt requests from any of the hardware modules and devices on the extension bus. The types of interrupt services include transport packet parsing, program clock recovery, traffic controller and OSD service requests, service or data transfer requests from the extension bus and communication processor, and service requests from the audio/video decoder.” AV7110 Preview at 16.</p> <p>“At the lowest level, each hardware component has a firmware module associated with it. A module may consist of:</p> <p style="padding-left: 40px;">Initialization code - executed at processor reset</p> <p style="padding-left: 40px;">Interrupt Service Routines - executed from interrupt by the associated hardware module.</p> <p>The run-time support library provides an application programming interface for user software. All run-time modules are written to be invoked from supervisory mode. This prevents software running in user mode from interfering with the built-in firmware.</p> <p>Functionally, the firmware consists of several software processes that are self contained at runtime and operate for the most part, independently and asynchronously. Because of the nature of the processing of a complex input stream, the processes are interrupt driven.</p> <p>The interrupt priorities determine the processing sequence, and the demultiplexed input stream packet information determines the data path through the system. There is only minimal inter-process dependency, which eliminates the need for a software control-flow process. Any inter-process dependencies can be handled by proper structuring of the interrupt process in terms of priorities and multi-level processing.” AV7110 Preview at 13-14.</p> <p><i>See claim 1 at 1c and claim 22, supra.</i></p>
Claim 30	
<p>30. The system of claim 1, further comprising a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in said media manager.</p>	<p>AV7110 Preview discloses or at least renders obvious a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in said media manager. For example:</p> <p>“general purpose I/Os</p>

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	<p>The 'AV7110 has four dedicated (101, 102, 104, and 105) and five multiplexed general purpose I/O pins (103 and 106 to 109) which are user configurable. Each I/O port has its own 32-bit control/status register, IOCSR<sub>n</sub>, where n ranges from 1 to 9.</p> <p>If an I/O is configured as an input and the delta interrupt mask is cleared, an IRQ is generated whenever an input changes state. If the delta interrupt mask is set, interrupts to the ARM are disabled. If no other device drives the I/O pin while it is configured as an input, it will be held high by an internal pullup resistor.</p> <p>If an I/O is configured as an output (by setting the cio bit in the corresponding control/status register), the value contained in the io_out) bit of the control/status register is output. Interrupt generation is disabled when an I/O is configured as an output.” AV7110 Preview at 77; <i>see also id.</i> tbl. 37.</p> <p>“extension bus interface (EBI)</p> <p>The extension bus interface is a 32-bit or 16-bit bidirectional data bus with a 25-bit address. It also provides 3 external interrupts and a wait line. All the external memories or I/O devices are mapped to the 32-bit address space of the ARM. There are six internally generated chips selects (CS<sub>x</sub>) for devices such as EEPROM memory, modem, front panel, front panel, front end control, parallel output port, and 1394 link device. Each CS has its own defined memory space and a programmable wait register which has a default of maximum allowable values as defined in Table 27. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. These are all programmable by user application software using APIs.” AV7110 Preview at 50.</p> <p>“The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO), and MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infra-red (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.” AV7110 Preview at 1.</p>



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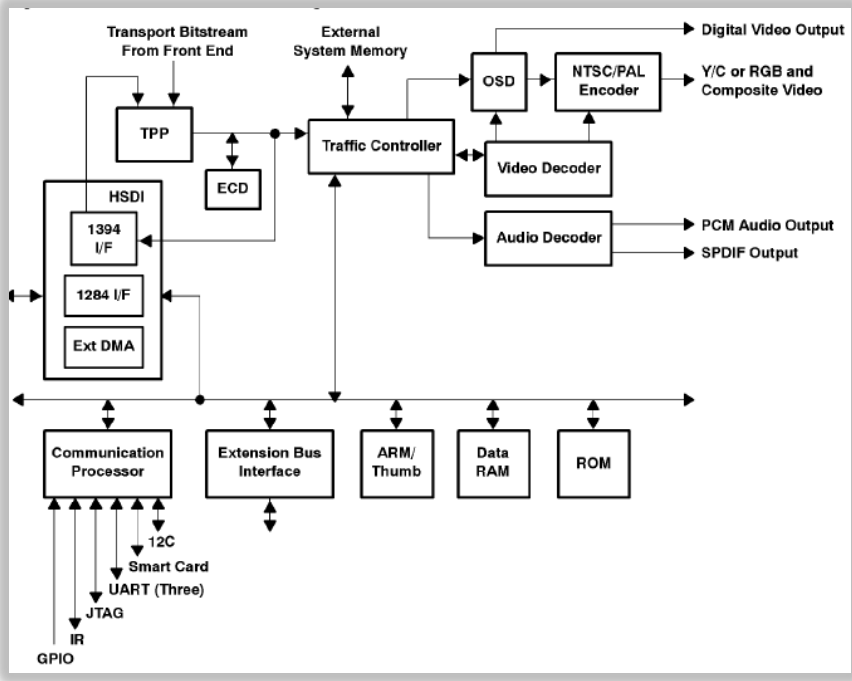


AV7110 Preview at 12 fig. 1.

Table 27. An Example of Extension Bus Chip Select Assignment

CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE
CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)
N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)
N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)
CS2	3000 0000 – 31FF FFFF	1 – 7	Modem
CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel
CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port

AV7110 Preview at 51 tbl. 27.

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	<p>See AV7110 Preview at 2-11, table 1 (e.g., “IO1” — “IO5”)</p> <p>See also claim 1 at 1e, <i>supra</i>.</p>
Claim 32	
<p>32. The system of claim 1, wherein said second bus element comprises a system bus.</p>	<p>AV7110 Preview discloses or at least renders obvious said second bus element comprises a system bus. For example:</p>  <p>The diagram illustrates a system architecture with a central horizontal system bus. Above the bus, from left to right, are: a block containing HSDI, 1394 I/F, 1284 I/F, and Ext DMA; a Traffic Controller; and a block containing OSD, NTSC/PAL Encoder, Video Decoder, and Audio Decoder. Below the bus, from left to right, are: a Communication Processor; an Extension Bus Interface; ARM/Thumb; Data RAM; and ROM. Various input/output interfaces are shown: Transport Bitstream From Front End and External System Memory connect to the Traffic Controller. Digital Video Output, Y/C or RGB and Composite Video, PCM Audio Output, and SPDIF Output are outputs from the top-right block. The Communication Processor is connected to GPIO, IR, JTAG, UART (Three), Smart Card, and 12C. The Traffic Controller is connected to an ECD block. The Extension Bus Interface connects to the Communication Processor and the ARM/Thumb block.</p> <p>AV7110 Preview at 12 fig. 1.</p> <p>“extension bus interface (EBI)</p>

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	<p>The extension bus interface is a 32-bit or 16-bit bidirectional data bus with a 25-bit address. It also provides 3 external interrupts and a wait line. All the external memories or I/O devices are mapped to the 32-bit address space of the ARM. There are six internally generated chips selects (CSx) for devices such as EEPROM memory, modem, front panel, front panel, front end control, parallel output port, and 1394 link device. Each CS has its own defined memory space and a programmable wait register which has a default of maximum allowable values as defined in Table 27. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. These are all programmable by user application software using APIs.” AV7110 Preview at 50.</p> <p>“CS1 is intended for ARM application code, but writes will not be prevented. CS2, CS3, CS4, and CS5 all have the same characteristics. The ARM performs reads and writes to these devices through the extension bus. CS6 is read and write accessible by the ARM. It is also accessed by the TC for TPP DMAs, and it is write only. User C application software selects the PIO of the packets to be sent through this port, the TPP will then send the data Q via DMAs. The parallel port is one byte wide and it is accessed via the least significant byte.” AV7110 Preview at 51.</p> <div><p><b>Table 27. An Example of Extension Bus Chip Select Assignment</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 Mbytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2EFF FFFF</td><td>N/A</td><td>DRAM (up to 16 Mbytes, on RAS1)</td></tr><tr><td>N/A</td><td>2F00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 16 Mbytes, on RAS3)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7110 Preview at 51 tbl. 27.</p> <p>“The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it has to become active before the programmable wait cycle expires. If the combined total wait states exceeds its maximum, the decoder is not guaranteed to function properly. The EXTWAIT signal is synchronized internally with the on-chip 81 MHz clock. When a device needs</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)	N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)	N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE																																		
CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)																																		
N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)																																		
N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)																																		
CS2	3000 0000 – 31FF FFFF	1 – 7	Modem																																		
CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel																																		
CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device																																		
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device																																		
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port																																		

'472 Patent Claim	Exemplary Prior Art Disclosure
	<p>to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT signal should be at least 24.7 ns. Since the EXTWAIT signal has the potential to stall the whole decoding process, the ARM will cap its wait to 500 ns. Afterwards, the ARM assumes the device that generated the EXTWAIT has failed and will ignore EXTWAIT from then on. Only a software or hardware reset can activate the EXTWAIT signal again. The timing diagram shown in Figure 19 is an example of a read using the EXTWAIT signal.” AV7110 Preview at 53.</p> <p>“The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 32-bit or 16-bit data and 25-bit address. It also supports DMA transfers to/from the extension bus. DMA transfers within the extension bus are not supported directly. They may be accomplished from user application software by using one DMA to the internal data RAM, followed by a second DMA to transfer back to the EBI. Extension bus single read and write cycle timings are shown in Figure 17 and Figure 18 respectively.” AV7110 Preview at 51; <i>see also id.</i> at 52 figs. 17 and 18.</p> <p><i>See</i> AV7110 Preview at 60, table 29 (“Types of DMA Transfers Allowed for Data Ports”).</p> <p><i>See</i> claim 1 at 1d, 1e, and 1f, <i>supra</i>.</p>

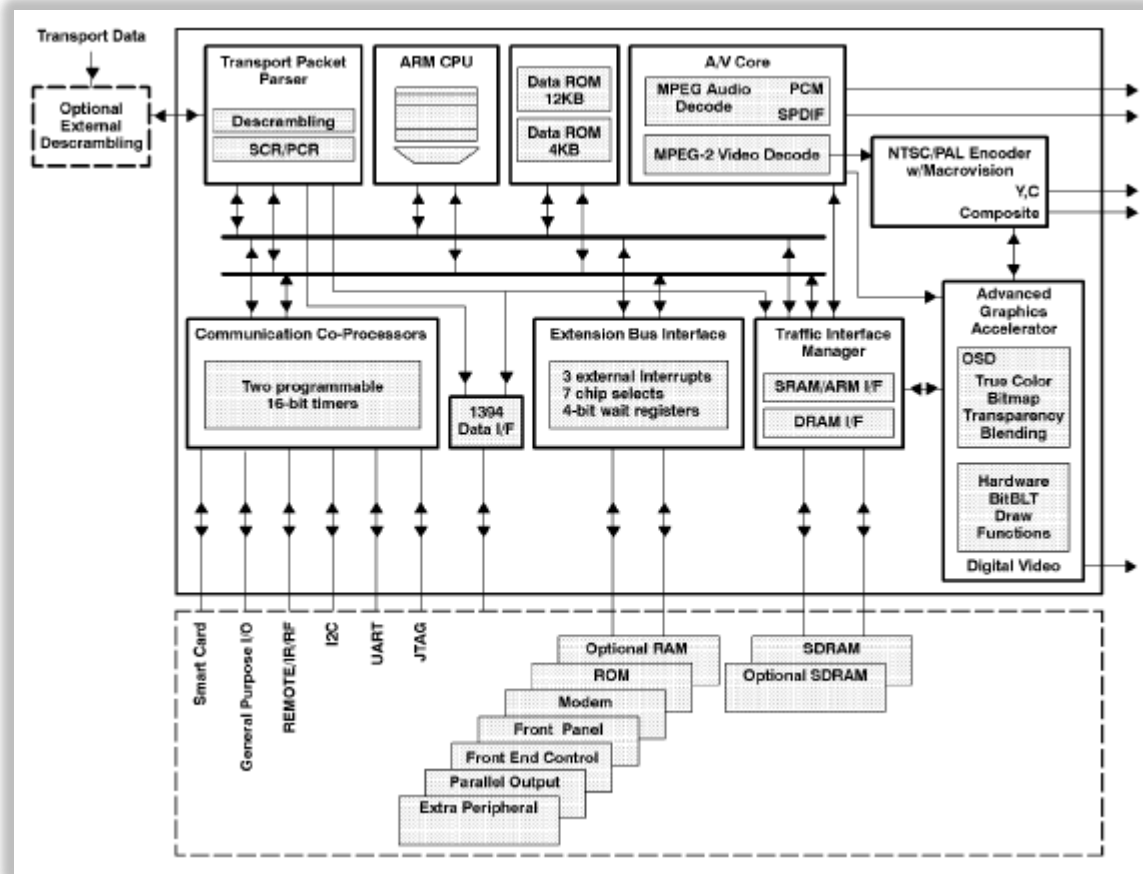
**Invalidity Contentions for U.S. Patent No. 8,457,476****Based on “Product Preview: TMS320AV7100 Integrated Set-Top Digital Signal Processor” (“AV7100 Preview”)**

Based upon TiVo’s Complaint, Infringement Contentions, and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered, the reference charted below anticipates or at least renders obvious the asserted claims. These invalidity contentions are not an admission by Samsung that the accused products are covered by, or infringe the asserted claims, particularly when these claims are properly construed and applied. These invalidity contentions are not an admission that Samsung concedes or acquiesces to any claim construction implied or suggested by TiVo’s Complaint or Infringement Contentions. Nor is Samsung asserting any claim construction positions through these charts, including whether the preamble is a limitation. The portions of the prior art reference cited below are not exhaustive but are exemplary in nature.

<b>’476 Patent Claim</b>	<b>Exemplary Prior Art Disclosure</b>
<b>Claim 1</b>	
[1p] A system for the simultaneous storage and retrieval of multimedia data, comprising:	<p>To the extent that the preamble is limiting, the AV7100 Preview discloses or at least renders obvious a system for the simultaneous storage and retrieval of multimedia data. For example:</p> <p>“The TMS320AV7100 Integrated Digital Satellite System (DSS) Set-Top Digital Signal Processor (‘AV7100) is designed to be the core of a digital set-top box. It incorporates an Advanced RISC Machines (ARM) central processor, a transport bit stream decoder, an MPEG video and audio decoder, an NTSC/PAL (National Television Standards Committee/Phase Alternating Line) video encoder, an on-screen display controller to mix graphics and video, a 1394 interface to an external 1394 device, two universal asynchronous receiver transmitter (UART) serial data interfaces, infra red (IR) and radio frequency (RF) remote control inputs, REMOTE input and output, a smart card interface, and an extension bus to connect peripherals, such as additional RS232 ports, display and control panels, and additional read-only memory (ROM) and dynamic RAM (DRAM). External program and data memory expansion allows the ‘AV7100 to support a range of set-top boxes from low- to high-end.” AV7100 Preview at 1.</p>

## '476 Patent Claim

## Exemplary Prior Art Disclosure



AV7100 Preview at 9 fig. 1.

“trick mode decoding

When decoding a picture from a digital recorder, the ‘AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors.

During trick mode decoding, the video decoder repeats the following steps:

'476 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li> </ul> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p> <div> <pre> graph LR     In(( )) --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM     TPP --&gt; Out(( ))     In --&gt; Out   </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p>

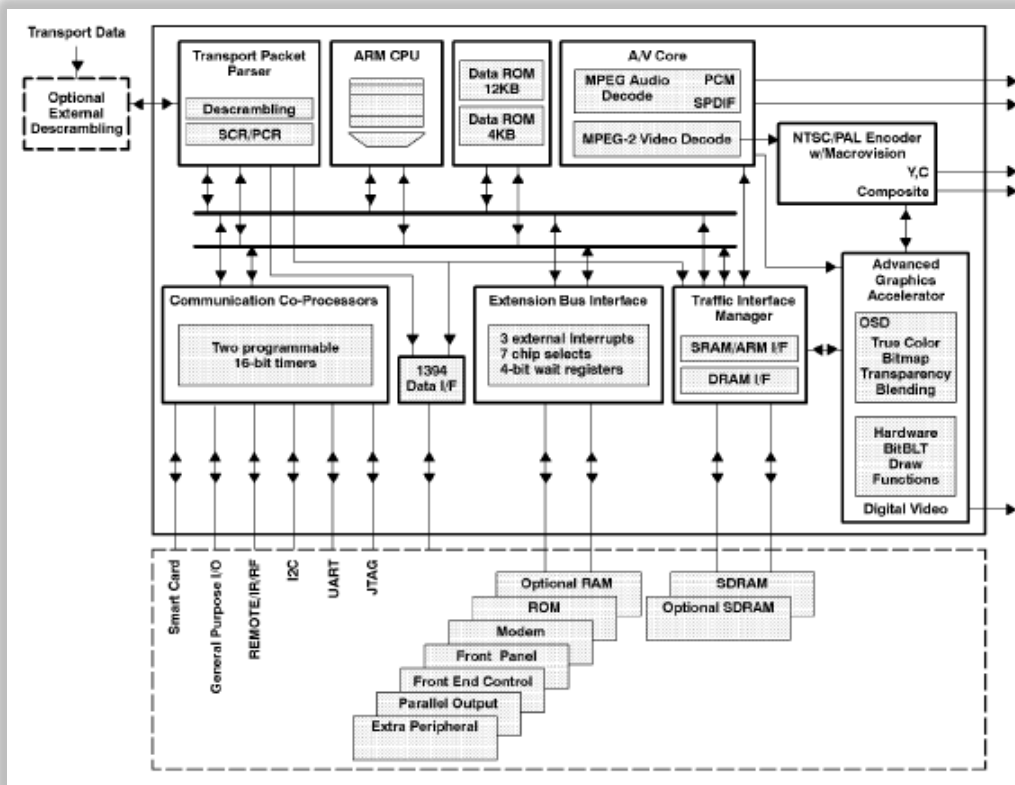
'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“extension bus read and write timing The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p> <p><i>See claim 1 at 1a-1i, infra.</i></p>
[1a] an input section that acquires an input signal, the input section creates a transport stream from the input signal;	<p>AV7100 Preview discloses or at least renders obvious an input section that acquires an input signal, the input section creates a transport stream from the input signal. For example:</p> <p>“input interface The transport packet data from the FEC device is input to the ‘AV7100 eight bits at a time, using the byte clock, DCLK. A high on PACCLK signals valid packet data. During satellite sourced decode, a DERROR signal is</p>



'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>received from the FEC device to indicate that a packet has data errors. The DERROR pin is valid on the first byte or one data byte cycle before the first data byte. It does not change until the following packet.” AV7100 Preview at 16; <i>see also id.</i> at 17 fig. 5 (illustrating input interface timing).</p> <p><i>See</i> AV7100 Preview at 1 (stating that the AV7100 “[a]ccepts Transport Bit Stream Up to 40-MBits per Second”).</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p>“During recording, it is assumed that input data originates from the FEC device. An FEC error signal sets the DERROR pin at or before the first byte of input data. This DERROR value is sent to the PERROR output on the 1394 interface coincident with the first valid PDATA. The PERROR value remains active as long as the FEC device keeps DERROR active. Typically, the FEC device retains DERROR until the beginning of the following packet. In this case, the 1394 link device may check for record errors at the first data byte of the packet.” AV7100 Preview at 54.</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p><i>See</i> AV7100 Preview at 1 (stating that the AV7100 “[a]ccepts Transport Bit Stream Up to 40-MBits per Second”).</p> <p>“Video Decoder Decodes MPEG-1 (Moving Pictures Experts Group) and MPEG-2 Main Profile and Main Level Bit Stream</p> <ul style="list-style-type: none"> <li>• Audio Decoder Decodes MPEG-1 Layer I and II Bit Stream” AV7100 Preview at 1.</li> </ul> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Supports output data in both PCM and SPDIF formats</li> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for sychronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p>“The video decoder is capable of producing decimated pictures using <math>\frac{1}{2}</math> or <math>\frac{1}{4}</math> decimation per dimension, which results in reduced areas of <math>\frac{1}{4}</math> or <math>\frac{1}{16}</math>, respectively. The decimated picture can be viewed in real time. Decimation is achieved by using field data out of a frame, skipping lines, and performing vertical filtering to smooth the decimated image.” AV7100 Preview at 19.</p> <p>See AV7100 Preview at 19 (describing (1) display formats supported by AV7100, (2) aspect ratio conversion supported by the AV7100).</p>
[1b] a processor;	<p>AV7100 Preview discloses or at least renders obvious a processor. For example:</p> <p>“ARM CPU features</p> <ul style="list-style-type: none"> <li>• Operates at 40.5 MHz</li> <li>• Supports byte (8-bit), half-word (16-bit), and word (32-bit) data types</li> <li>• Reads instructions from on-chip ROM or from the ‘AV7100 extension bus</li> <li>• Switchable between ARM (32-bit) or THUMB (16-bit) instruction modes</li> <li>• 32-bit data and 32-bit address lines</li> <li>• Seven processing modes</li> <li>• Two interrupts, fast interrupt request (FIQ) and interrupt request (IRQ)” AV7100 Preview at 11.</li> </ul> <p>“The ARM7TDM I/THUMB is the integrated CPU of the ‘AV7100. The ARM is a 32-bit RISC processor which is capable of executing instructions in 16- or 32-bit format at a clock frequency of 40.5 MHz. The standard ARM instructions are exactly one word (32 bits) in length, and the data operations are performed on word quantities only. However, LOAD and STORE instructions can transfer either byte, half-word, or word quantities. The ARM THUMB mode uses the same 32-bit architecture with a 16-bit instruction set. This mode retains the 32-bit performance, but reduces the code size with 16-bit instructions. With 16-bit instructions, THUMB still gives 70 - 80% of the performance of the ARM as when running ARM instructions from 32-bit memory. In this data sheet, ARM and THUMB are used interchangeably.” AV7100 Preview at 11.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The ARM uses a LOAD and STORE architecture such that all operations are on the registers. The ARM has seven different processing modes, with sixteen 32-bit registers visible in user mode. In the THUMB configuration there are only eight registers available in user mode. However, the high registers may be accessed through special instructions. The instruction pipeline is three stage, fetch - decode - execute, and most instructions take only one cycle to execute.” AV7100 Preview at 11.</p>
<p>[1c] a decoder subsystem that decodes the transport stream, the decoder subsystem is communicatively connected to the processor;</p>	<p>AV7100 Preview discloses or at least renders obvious a decoder subsystem that decodes the transport stream, the decoder subsystem is communicatively connected to the processor. For example:</p>  <p>The diagram illustrates the AV7100 system architecture. At the top, 'Transport Data' enters through an 'Optional External Descrambling' block into a 'Transport Packet Parser' which includes 'Descrambling' and 'SCR/PCR' blocks. This parser is connected to an 'ARM CPU' and a 'Data ROM' (12KB and 4KB). The ARM CPU is also connected to an 'A/V Core' containing 'MPEG Audio Decode', 'PCM', 'SPDIF', and 'MPEG-2 Video Decode' blocks. The A/V Core outputs to an 'NTSC/PAL Encoder w/Macrovision' which produces 'Y,C' and 'Composite' signals. Below the ARM CPU is a 'Communication Co-Processors' block with 'Two programmable 16-bit timers'. To the right is an 'Extension Bus Interface' with '3 external interrupts', '7 chip selects', and '4-bit wait registers'. Further right is a 'Traffic Interface Manager' with 'SRAM/ARM I/F' and 'DRAM I/F' blocks. These components are interconnected via a central bus. At the bottom, various peripherals are shown: 'Smart Card', 'General Purpose I/O', 'REMOTE/IR/RF', 'I2C', 'UART', 'JTAG', 'Optional RAM', 'ROM', 'Modem', 'Front Panel', 'Front End Control', 'Parallel Output', 'Extra Peripheral', 'Optional SDRAM', and 'SDRAM'. The 'Advanced Graphics Accelerator' block, which includes 'OSD', 'True Color', 'Bitmap', 'Transparency', 'Blending', and 'Hardware BitBLT Draw Functions', is connected to the bus and outputs 'Digital Video'.</p> <p>AV7100 Preview at 9 fig. 1.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“Video Decoder Decodes MPEG-1 (Moving Pictures Experts Group) and MPEG-2 Main Profile and Main Level Bit Stream</p> <ul style="list-style-type: none"> <li>• Audio Decoder Decodes MPEG-1 Layer I and II Bit Stream” AV7100 Preview at 1.</li> </ul> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware” AV7100 Preview at 15.</li> </ul> <p>“transport bit stream processing</p> <p>The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.</p> <p>The TPP also activates or deactivates the decryption engine based upon the content of the individual packet. The conditional access keys are stored in RAM and managed by firmware running on the ARM. The TPP will also detect packets lost from the transport stream. Using error concealment by the audio/video decoder and redundant header information from the DSS bit stream, the ‘AV7100 minimizes the effects of lost data.” AV7100 Preview at 15.</p> <p>“video decoder</p>

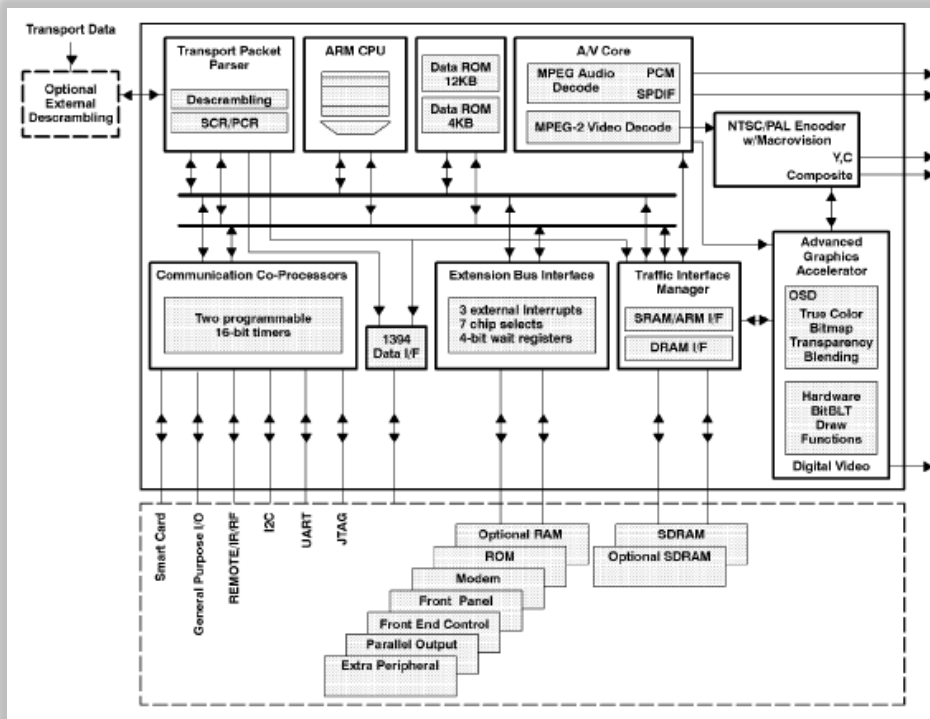
'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>features</p> <ul style="list-style-type: none"> <li>• Real-time video decoding of MPEG-2 Main Profile and Main Level Bit Stream and MPEG-1</li> <li>• Error detection and concealment</li> <li>• Internal 90 kHz/27-MHz system time clock</li> <li>• Sustained input rate of 15 Mbps</li> <li>• Supports trick mode with full trick mode picture</li> <li>• Provides 1/4 and 1/16 decimated picture size</li> <li>• Extracts closed caption and other picture user data from the bit stream</li> <li>• 3:2 pulldown in NTSC mode</li> <li>• Supports various display formats with polyphase horizontal resampling and vertical chrominance filtering</li> <li>• Pan-and-scan for 16:9 source material according to both DSS and MPEG syntax</li> <li>• High-level command interface</li> <li>• Synchronization using presentation time stamps (PTS)</li> <li>• Half resolution display mode allows additional OSD space in the SDRAM” AV7100 Preview at 18.</li> </ul> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p> <p>“trick mode decoding</p> <p>When decoding a picture from a digital recorder, the ‘AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li> </ul> <p>“The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder AP Is. Consult the TMS320AV7100 Software Guide for details.” AV7100 Preview at 20; <i>see id.</i> tbl. 8 (showing video decoder commands).</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Supports output data in both PCM and SPDIF formats</li> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for sychronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p><i>See</i> AV7100 Preview at 31-32 (listing and describing audio decoder control and status registers).</p> <p>“extension bus interface</p> <p>The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus. Each CS has its own defined memory space and a programmable wait register. The number of wait states depends on the content of the</p>

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	<p>register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. . . .</p> <p>The extension bus supports the connection of seven devices using the predefined chip selects. Additional devices may be used by externally decoding the address bus. Table 21 shows the name of the device, its chip select, address range, and programmable wait state. Table 22 and Table 23 show extension bus wait state and configuration registers. Each device on the extension bus is required to have data outputs in high-impedance state within one clock cycle following the removal of chip-select.” AV7100 Preview at 37.</p> <div><p><b>Table 21. Extension Bus Chip Selects</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 MBytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 32 MBytes)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7100 Preview at 37 tbl. 21.</p> <p>“extension bus read and write timing</p> <p>The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p> <p>“EXTWAIT signal</p> <p>The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it must become active before the programmable wait cycle expires. The total number of wait states should not exceed the maximum allowed from Table 21. If the combined total wait states exceed the maximum, the decoder is not guaranteed to function properly. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT should</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)	N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
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CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port																														



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	<p>be at least 24.7 ns. Because the EXTWAIT signal has the potential to stall the decoding process, the ARM will cap its wait at 500 ns. After this time, the ARM assumes the device that generated the EXTWAIT has failed and ignores EXTWAIT from that point forward. Only a software or hardware reset can activate the EXTWAIT signal again. . . .</p> <p>If an 8-bit device is connected to the extension bus, the EBI automatically converts the single ARM word access to four consecutive byte accesses, and the maximum wait time applies to the total of the four byte accesses. In the consecutive read access where the CS remains active during the reading of four bytes, each byte access has to complete within 125 ns. For a device that requires longer access delay, for example 250 ns, then the access from the ARM has to be limited only to half words. In a write access, where the CS toggles for each byte write, each write can take 500 ns.” AV7100 Preview at 42.</p> <p>“The extension bus supports access to 60 or 70 ns DRAM. The DRAM must have an 8-bit, 9-bit, or 10-bit column address and must have a data width of 8 or 16 bits. Byte access is allowed even when the DRAM has a 16-bit data width. The byte access is specified by the signal DCAS for EXTDATA[15:8] and CCAS for EXTDATA[7:0]. The system default DRAM configuration is 70 ns, 9-bit column address, and 16-bit data width. The firmware verifies the DRAM configuration during startup.” AV7100 Preview at 43; <i>see id.</i> at 43-50 (describing additional aspects of extension bus DRAM).</p> <p>“traffic controller features</p> <ul style="list-style-type: none"> <li>• Authorizes and manages direct memory access (DMA) transfers</li> <li>• Provides SDRAM interface</li> <li>• Provides memory access protection</li> <li>• Manages interrupt requests</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>TTP/DES to/from internal data RAM</li> <li>Data RAM to/from extension bus SDRAM to OSD</li> <li>Audio and video decoders to/from SDRAM</li> <li>SDRAM to/from data RAM</li> </ul> </li> <li>• Manages extension bus</li> <li>• Generates chip selects for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus” AV7100 Preview at 12.</li> </ul> <p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video</p>

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	<p>images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p>
<p>[1d] a media switch communicatively connected to the decoder subsystem, the media switch operative to interface a plurality of system components and operates asynchronously from the processor, wherein the media switch includes:</p>	<p>AV7100 Preview discloses or at least renders obvious a media switch communicatively connected to the decoder subsystem, the media switch operative to interface a plurality of system components and operates asynchronously from the processor. For example:</p>  <p>The diagram illustrates the AV7100 system architecture. At the top, 'Transport Data' enters a dashed box labeled 'Optional External Descrambling', which connects to the 'Transport Packet Parser'. The 'Transport Packet Parser' contains 'Descrambling' and 'SCR/PCR' blocks. It is connected to an 'ARM CPU' and 'Data ROM' (12KB and 4KB). The 'ARM CPU' is also connected to the 'A/V Core'. The 'A/V Core' includes 'MPEG Audio Decode', 'PCM', 'SPDIF', and 'MPEG-2 Video Decode' blocks. The 'MPEG-2 Video Decode' block connects to an 'NTSC/PAL Encoder w/Macrovision', which outputs 'Y/C' and 'Composite' signals. Below these, a central horizontal bus connects to several components: 'Communication Co-Processors' (containing 'Two programmable 16-bit timers'), 'Extension Bus Interface' (containing '3 external interrupts', '7 chip selects', and '4-bit wait registers'), and 'Traffic Interface Manager' (containing 'SRAM/ARM I/F' and 'DRAM I/F'). The 'Extension Bus Interface' also connects to a '1394 Data I/F' block. To the right, an 'Advanced Graphics Accelerator' block contains an 'OSD' (True Color, Bitmap, Transparency, Blending) and 'Hardware BitBLT Draw Functions' leading to 'Digital Video' output. At the bottom, a dashed box labeled 'Smart Card' contains various peripheral interfaces: 'General Purpose I/O', 'REMOTE/IR/RF', 'I2C', 'UART', 'JTAG', 'Optional RAM', 'ROM', 'Modem', 'Front Panel', 'Front End Control', 'Parallel Output', and 'Extra Peripheral'. 'SDRAM' and 'Optional SDRAM' are also shown connected to the system.</p>

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	<p>AV7100 Preview at 9 fig. 1.</p> <p>“traffic controller features</p> <ul style="list-style-type: none"> <li>• Authorizes and manages direct memory access (DMA) transfers</li> <li>• Provides SDRAM interface</li> <li>• Provides memory access protection</li> <li>• Manages interrupt requests</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>TTP/DES to/from internal data RAM</li> <li>Data RAM to/from extension bus SDRAM to OSD</li> <li>Audio and video decoders to/from SDRAM</li> <li>SDRAM to/from data RAM</li> </ul> </li> <li>• Manages extension bus</li> <li>• Generates chip selects for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus” AV7100 Preview at 12.</li> </ul> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware” AV7100 Preview at 15.</li> </ul> <p>“transport bit stream processing</p> <p>The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies</p>

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	<p>whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.</p> <p>The TPP also activates or deactivates the decryption engine based upon the content of the individual packet. The conditional access keys are stored in RAM and managed by firmware running on the ARM. The TPP will also detect packets lost from the transport stream. Using error concealment by the audio/video decoder and redundant header information from the DSS bit stream, the 'AV7100 minimizes the effects of lost data." AV7100 Preview at 15.</p> <p>"ARM CPU features</p> <ul style="list-style-type: none"> <li>• Operates at 40.5 MHz</li> <li>• Supports byte (8-bit), half-word (16-bit), and word (32-bit) data types</li> <li>• Reads instructions from on-chip ROM or from the 'AV7100 extension bus</li> <li>• Switchable between ARM (32-bit) or THUMB (16-bit) instruction modes</li> <li>• 32-bit data and 32-bit address lines</li> <li>• Seven processing modes</li> <li>• Two interrupts, fast interrupt request (FIQ) and interrupt request (IRQ)" AV7100 Preview at 11.</li> </ul> <p>"The SDRAM interface supports 16-bit data width SDRAM operating at minimum 81 MHz. The SDRAM selected for use with the 'AV7100 should meet or exceed the timing requirements in Table 3 for proper operation. The TI TMS626162-12 is one example of a compatible 16 Mbit SDRAM." AV7100 Preview at 13.</p> <p>"system clock reference recovery</p> <p>Combined with the ARM, the TPP also handles system clock reference (SCR) recovery with an external VCXO. The TPP latches and transfers its internal system clock to the ARM upon the arrival of any packet which contains system clock information. After further processing of the packet and identification of the system clock, the ARM calculates the difference between the system clock from the bit stream and the internal system clock at the time the packet arrives. The ARM filters this difference and routes it through a Sigma-Delta digital-to-analog converter to control an external VCXO. Output from the 'AV7100 VCXO CTRL pin is a digital pulse train with 8-bit resolution for control. During startup, when there is no incoming SCR, the ARM drives the VCXO to its</p>

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	<p>center frequency. Figure 4 provides an example circuit for the external VCXO.” AV7100 Preview at 15; <i>see id.</i> tbl. 4.</p> <div> </div> <p>AV7100 Preview at 16 fig. 4.</p> <p>“Both the video and audio decoders synchronize their presentation using the transmitted PTS. For DSS the PTS is transmitted as picture user data in the video bit stream and as an MPEG-1 system packet bit stream for audio. Dedicated hardware decodes the PTS if it is in the MPEG-1 system packet and forwards it to the audio decoder. The video decoder decodes PTS from picture user data. Both the video and audio decoders compare PTS to the local system clock in order to synchronize presentation of reconstructed data. The local system clock is continuously updated by the ARM.</p> <p>When the PTS and local system clock do not match within tolerance, the video decoder either redisplay or skips a frame. At that time, the CC/EDS is handled as follows:</p> <ul style="list-style-type: none"> <li>• When the video decoder redisplay a frame, the second display does not contain CC/EDS.</li> <li>• When the video decoder skips a frame, the corresponding CC/EDS is also skipped.” AV7100 Preview at 20.</li> </ul> <p>“When the PCM_SRC pin is low, the ‘AV7100 audio PLL is used to generate the necessary output clocks for the audio data, phase locked to the input bit stream. The clock generator requires an 36.864-MHz external VCXO. The AUD PLLO pin outputs a control voltage that can be applied to the external loop filter and VCXO to produce</p>

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	<p>the required input at the AUD PLLI pin. The clock generator derives the correct output clocks, based on the contents of the audio control register bits PCMSSEL1-0, shown in Table 17. An example of the external clock circuit configuration is illustrated in Figure 23.” AV7100 Preview at 30; <i>see also id.</i> tbl. 17 (showing audio clock frequencies).</p> <p>“All firmware is stored in on-chip ROM, except the OSD graphics and some generic run-time support. The run-time support library (RTSL) and all user application software are stored outside the 'AV7100 in external memory attached to the extension bus. Details of the firmware, RTSL, and application program interface (API) are provided in the companion software document, TMS320AV7100 Software Guide.” AV7100 Product Preview at 11.</p> <p>“communication coprocessor features</p> <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> <li>• Provides three UARTs - one for smart card and two for general use</li> <li>• Accepts IR, REMOTE, and RF signals</li> <li>• Provides a REMOTE output</li> <li>• Provides two general purpose I/Os</li> <li>• Manages I2C and JTAG interfaces” AV7100 Preview at 33.</li> </ul> <p>“The communication coprocessor consists of a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR/RF, I2C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM. Interrupts are used to communicate between these interface modules and the ARM.” AV7100 Preview at 33.</p> <p>“The ‘AV7100 includes an interface to the smart card access control system. The interface consists of a high-speed UART and logic to comply with the News Datacom specification (Document #HU-T052, Release E, dated November 1994, and Release F, dated January 1996) “DirecTV Project: Decoder-Smart Card Interface Requirements.” Applicable software drivers that control the interface are also included, and detailed in the companion software document for the ‘AV7100.” AV7100 Preview at 33.</p> <p>“conditional access and DES processing</p>

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	<p>The conditional access is triggered by the arrival of a control word packet (CWP). The ARM firmware recognizes that a CWP has been received and passes it to the verifier, which is the user-implemented News Datacom application software running on the ARM. The verifier reads the CWP and communicates with the external smart card through a UART I/O interface. After verification, it passes the pointer to an 8-byte key back to the firmware, which then loads the key for the DES to decrypt succeeding packets.” AV7100 Preview at 33; <i>see id.</i> at 16 (describing additional aspects of processing transport data).</p> <p>“UART interfaces The ‘AV7100 includes two general purpose 2-wire UARTs that are memory mapped and fully accessible by application programs. The UARTs operate in asynchronous mode only and support baud rates of 1200, 2400, 4800, 9600, 14400, 19200, 28800, and 57600 kbps. The UARTs are full duplex. The transmitter is double buffered, and the receive interface is buffered with eight bytes of FIFO memory in addition to its internal register. The UARTs transmit/receive 1 start bit, 7 or 8 data bits, optional parity, and 1 or 2 stop bits. The outputs of the UARTs are digital and require external level shifters for RS232 compliance.” AV7100 Preview at 33; <i>see id.</i> at 33-34 (describing additional aspects of the UART interface).</p> <p>“The IR/RF remote control interface is a means of transmitting user commands to the set-top box. This interface consists of a custom hardware receiver implementing a bit frame-based communication protocol. A single bit frame represents a user command. The IR, RF, and REMOTEIN ports require a square wave input with no false transitions; therefore, the signal must reach its threshold prior to being applied to the pins. The interface accepts an IR, RF, or REMOTEIN data stream up to a frequency of 1.3 kHz. Since more than one data stream may be active at any given time, the ‘AV7100 hardware determines priority so that only one IR, RF, or REMOTE input is decoded.” AV7100 Preview at 35; <i>see id.</i> at 35-36 (describing additional aspects of the IR/RF remote control interface).</p> <p>“general purpose I/Os The ‘AV7100 includes two user-configurable I/O pins, 101 and 102. 101 and 102 are supported by dedicated 32-bit control/status registers, named IOSCR1 and IOSCR2, respectively.” AV7100 Preview at 36; <i>see id.</i> tbl. 20 (providing register descriptions for the control/status registers); <i>id.</i> at 37 (describing additional aspects of general purpose I/O).</p> <p>“I2C interface</p>

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	<p>The 'AV7100 includes an 12C serial bus interface that can act as either a master or slave. (Master mode is the default). In master mode, the 'AV7100 initiates and terminates transfers and generates clock signals. Only the standard mode (100 kbit/s) 12C-bus system is implemented; fast mode is not supported. Multi-master mode is also not supported.</p> <p>To put the device in slave mode the application program must set the slave mode select and a 7-bit address for the 'AV7100. The application must also send a software reset to the 12C to complete the transition to slave mode.</p> <p>In slave mode, when the programmable address bits match the applied address, the 'AV7100 responds accordingly. The 'AV7100 also responds to general call commands issued to address 0 (the general call address) that change the programmable part of the slave address. These commands are Ox04 and Ox06. No other general call commands are acknowledged, and no action is taken.” AV7100 Preview at 37.</p> <p>“Note that there is no direct DMA transfer to/from extension bus memories from/to the SDRAM. However, the user can employ the bitBLT hardware (which uses data RAM) as an intermediate step to execute such a transfer. The only constraints for this type of transfer are that the block being transferred must consist of 32-bit multiples, and it must begin at a 32-bit word boundary.” AV7100 Preview at 12.</p> <p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“extension bus interface</p> <p>The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus. Each CS has its own defined memory space and a programmable wait register. The number of wait states depends on the content of the</p>



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	<p>register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. . . .</p> <p>The extension bus supports the connection of seven devices using the predefined chip selects. Additional devices may be used by externally decoding the address bus. . . . Table 22 and Table 23 show extension bus wait state and configuration registers. Each device on the extension bus is required to have data outputs in high-impedance state within one clock cycle following the removal of chip-select.” AV7100 Preview at 37.</p> <div><p><b>Table 21. Extension Bus Chip Selects</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 MBytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 32 MBytes)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7100 Preview at 37 tbl. 21 (showing name of device, its chip select, address range, and programmable wait state).</p> <p>“CS1 is intended for ARM application code, but writes are not prevented. DRAM is read/write accessible by the ARM. It is also accessed by the traffic controller for TPP and bitBLT DMA transfers.</p> <p>CS2, CS3, CS4, and CS5 all have the same characteristics. The ARM performs reads and writes to these devices through the extension bus.</p> <p>CS6 is read and write accessible by the ARM. It is also accessed by the traffic controller for TPP DMAs, and it is write only. The parallel port is one byte wide and accessed via the most significant byte.” AV7100 Preview at 38.</p> <p>“extension bus read and write timing</p> <p>The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)	N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
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	<p>implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p> <p>“EXTWAIT signal The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it must become active before the programmable wait cycle expires. The total number of wait states should not exceed the maximum allowed from Table 21. If the combined total wait states exceed the maximum, the decoder is not guaranteed to function properly. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT should be at least 24.7 ns. Because the EXTWAIT signal has the potential to stall the decoding process, the ARM will cap its wait at 500 ns. After this time, the ARM assumes the device that generated the EXTWAIT has failed and ignores EXTWAIT from that point forward. Only a software or hardware reset can activate the EXTWAIT signal again. . . .</p> <p>If an 8-bit device is connected to the extension bus, the EBI automatically converts the single ARM word access to four consecutive byte accesses, and the maximum wait time applies to the total of the four byte accesses. In the consecutive read access where the CS remains active during the reading of four bytes, each byte access has to complete within 125 ns. For a device that requires longer access delay, for example 250 ns, then the access from the ARM has to be limited only to half words. In a write access, where the CS toggles for each byte write, each write can take 500 ns.” AV7100 Preview at 42.</p> <p>“The extension bus supports access to 60 or 70 ns DRAM. The DRAM must have an 8-bit, 9-bit, or 10-bit column address and must have a data width of 8 or 16 bits. Byte access is allowed even when the DRAM has a 16-bit data width. The byte access is specified by the signal DCAS for EXTDATA[15:8] and CCAS for EXTDATA[7:0]. The system default DRAM configuration is 70 ns, 9-bit column address, and 16-bit data width. The firmware verifies the DRAM configuration during startup.” AV7100 Preview at 43; <i>see id.</i> at 43-50 (describing additional aspects of extension bus DRAM).</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24..” AV7100 Preview at 51-52.</p>

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	<div> <p style="text-align: center;">Figure 19. 1394 Interface</p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p>

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	<div> <pre> graph LR     In(( )) --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM     1394[1394 Interface] --&gt; MUX     </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24.” AV7100 Preview at 52; <i>see id.</i> tbl. 24 (listing 1394 interface signals).</p> <p><i>See</i> AV7100 Preview at 3 (listing 1394 bus in pin descriptions table).</p> <p><i>See</i> AV7100 Preview at 3-8, table 1 (e.g., “SMCLK,” “SMCLK2”)</p> <p><i>See</i> claim 1 at 1e-1h, <i>infra</i>.</p>
[1e] a host controller;	<p>AV7100 Preview discloses or at least renders obvious a host controller. For example:</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24..” AV7100 Preview at 51-52.</p> <div> <pre> graph TD     AV7100[AV7100] --- ExternalBus[External Bus]     subgraph CentralBlock [ ]         direction TB         DVCRPacketizer[DVCR Packetizer]         LINKInterface[LINK Interface]         DVCRPacketizer --- LINKInterface     end     ExternalBus --- CentralBlock     CentralBlock --- PHYInterface[PHY Interface]     DVCRPacketizer --- Data[Data]   </pre> <p style="text-align: center;"><b>Figure 19. 1394 Interface</b></p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP,</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p> <div> <pre> graph LR     In(( )) --&gt; MUX     In --&gt; I1394[1394 Interface]     I1394 --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM   </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p>

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	<p><i>See claim 1 at 1i, infra.</i></p>
<p>[1f] a DMA controller;</p>	<p>AV7100 Preview discloses or at least renders obvious a DMA controller. For example:</p> <p>“traffic controller features</p> <ul style="list-style-type: none"> <li>• Authorizes and manages direct memory access (DMA) transfers</li> <li>• Provides SDRAM interface</li> <li>• Provides memory access protection</li> <li>• Manages interrupt requests</li> <li>• Manages the data flow between processors and memories</li> </ul> <p>TTP/DES to/from internal data RAM  Data RAM to/from extension bus SDRAM to OSD  Audio and video decoders to/from SDRAM  SDRAM to/from data RAM</p> <ul style="list-style-type: none"> <li>• Manages extension bus</li> <li>• Generates chip selects for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus” AV7100 Preview at 12. <p>“DMA transfer  The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“extension bus read and write timing  The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the</p> </li></ul>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p> <p>“The bit BLT hardware provides a fast way to move a block of memory from one space to another. The hardware reads data from a source location, performs shift/mask/merge/expand operations on the data, and finally writes it to a destination location. This hardware enables the following graphics functions:</p> <ul style="list-style-type: none"> <li>• SeVget pixel</li> <li>• Horizontal/vertical line drawing</li> <li>• Block fill</li> <li>• Bit BLT for fonts</li> <li>• Bitmap/graphic bit BLT</li> <li>• Transparency” AV7100 Preview at 25; <i>see id.</i> at 25-26 (describing additional aspects of the bit BLT hardware, including allowable source and destination memories for this module).</li> </ul> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24..” AV7100 Preview at 51-52.</p>



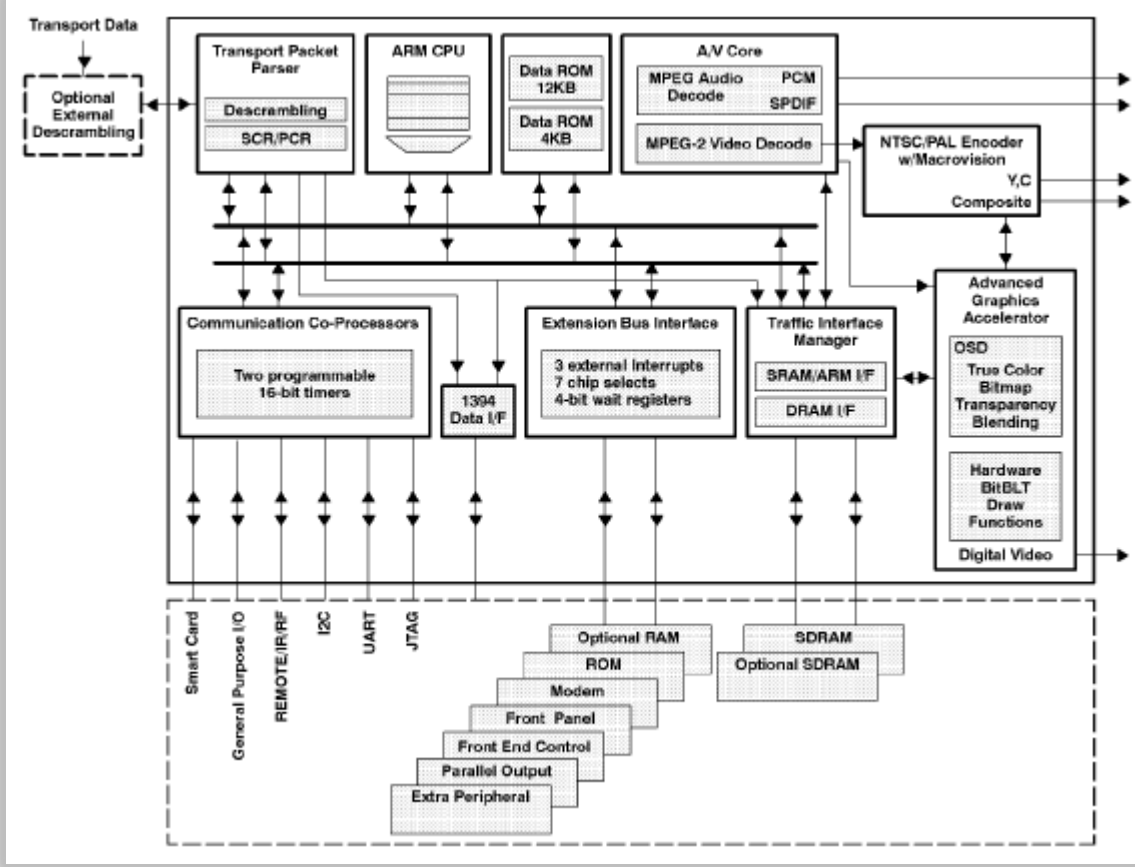
'476 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p style="text-align: center;">Figure 19. 1394 Interface</p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p>

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	<div> <pre> graph LR     In(( )) --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM     TPP --&gt; Out(( ))     In --&gt; Out   </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; see also id. at 53-54 (showing read and write timing relationships on the 1394 interface).</p>

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[1g] a bus arbiter; and	<p>AV7100 Preview discloses or at least renders obvious a bus arbiter. For example:</p> <p>“interrupts There are three externally accessible interrupt lines and three corresponding interrupt acknowledges on the 'AV7100. These three interrupts, along with interrupts generated internally to the 'AV7100, are handled by a centralized interrupt handler. Interrupt mask and priority are managed by the firmware. The three extension bus interrupts are connected to three different interrupt request lines which are visible to the user via the EXTINT2:0 pins. When the interrupt handler on the ARM begins servicing one of these interrupts, the ARM should first issue an interrupt acknowledge, which activates the corresponding EXTACK2:0 output. At the completion of the interrupt servicing, the ARM should reset the interrupt acknowledge, which returns EXTACK2:0 to the inactive state.” AV7100 Preview at 42.</p> <p>“Based on programmable priority, the ARM responds to interrupt requests generated by internal modules and external devices on the extension bus. Some of the requests are for data transfers to internal RAM, whereas others are true interrupts to the ARM. The 'AV7100s traffic controller handles data transfers, and the ARM provides services to true interrupts. Interrupts are grouped into FIQ and IRQ categories. The system software uses FIQ; the application software uses IRQ. The priorities for FIQs and IRQs are managed by the firmware.” AV7100 Preview at 11.</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24.” AV7100 Preview at 51-52; <i>see id.</i> at 51 fig. 19.</p> <p>“extension bus read and write timing The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state.” AV7100 Preview at 39.</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100</p>

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	<p>DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p> <div> <pre> graph LR     In(( )) --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP &lt;--&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM     TC --&gt; Out(( ))     1394[1394 Interface] &lt;--&gt; TPP     </pre> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p>

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[1h] a multimedia data stream processor; and	<p>AV7100 Preview discloses or at least renders obvious a multimedia data stream processor. For example:</p>  <p>AV7100 Preview at 9 fig. 1.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p>“transport bit stream processing</p> <p>The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.</p> <p>The TPP also activates or deactivates the decryption engine based upon the content of the individual packet. The conditional access keys are stored in RAM and managed by firmware running on the ARM. The TPP will also detect packets lost from the transport stream. Using error concealment by the audio/video decoder and redundant header information from the DSS bit stream, the ‘AV7100 minimizes the effects of lost data.” AV7100 Preview at 15.</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending them with the video. The OSD module accepts video from the video decoder, reads OSD data from SDRAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces. OSD defaults to standby mode and simply routes video from the video decoder to both outputs. The ARM is responsible for turning on/off OSD operations and for setting specific window attributes of the OSD windows. Dedicated bitBLT</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>hardware attached to the OSD module provides acceleration to memory block moves and graphics operations. OSD data may originate from the user data in the bit stream or may be generated by applications executed on the ARM. Regardless of the source, the OSD data is stored in the SDRAM and managed by the ARM. Memory space in the single 16 Mbits SDRAM is limited to approximately 241 kbytes for OSD, with capability to increase this to approximately 391 kbytes using the half resolution display mode. The OSD data may be represented in one of the following forms: bitmap, graphics 4:4:4 component, 4:2:2 component, or simply background color.” AV7100 Preview at 22; see also id. at 21, 22-24 (describing additional aspects of the OSD module).</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. Figure 19 depicts the connection.” AV7100 Preview at 51.</p> <div> <pre> graph TD     AV7100[AV7100] --- ExternalBus[External Bus]     ExternalBus --- LINK[LINK Interface]     LINK --- DVCR[DVCR Packetizer]     DVCR --- Data[Data]     LINK --- PHY[PHY Interface]   </pre> <p>The diagram illustrates the 1394 interface architecture. At the top is a horizontal bar labeled 'AV7100'. A vertical line descends from this bar to a horizontal line labeled 'External Bus'. From the 'External Bus', a vertical line continues down to a box labeled 'LINK Interface'. To the right of the 'LINK Interface' box is another box labeled 'DVCR Packetizer', connected to the 'LINK Interface' by a horizontal line. A line labeled 'Data' connects the 'DVCR Packetizer' to the right. Below the 'LINK Interface' box is a box labeled 'PHY Interface', connected by a vertical line.</p> <p style="text-align: center;"><b>Figure 19. 1394 Interface</b></p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“communication coprocessor features</p> <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> </ul>



'476 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Provides three UARTs - one for smart card and two for general use</li> <li>• Accepts IR, REMOTE, and RF signals</li> <li>• Provides a REMOTE output</li> <li>• Provides two general purpose I/Os</li> <li>• Manages 12C and JTAG interfaces” AV7100 Preview at 33.</li> </ul> <p>“The communication coprocessor consists of a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR/RF, 12C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM. Interrupts are used to communicate between these interface modules and the ARM.” AV7100 Preview at 33.</p> <p>“The ‘AV7100 includes an interface to the smart card access control system. The interface consists of a high-speed UART and logic to comply with the News Datacom specification (Document #HU-T052, Release E, dated November 1994, and Release F, dated January 1996) “DirecTV Project: Decoder-Smart Card Interface Requirements.” Applicable software drivers that control the interface are also included, and detailed in the companion software document for the ‘AV7100.” AV7100 Preview at 33.</p> <p>“conditional access and DES processing The conditional access is triggered by the arrival of a control word packet (CWP). The ARM firmware recognizes that a CWP has been received and passes it to the verifier, which is the user-implemented News Datacom application software running on the ARM. The verifier reads the CWP and communicates with the external smart card through a UART I/O interface. After verification, it passes the pointer to an 8-byte key back to the firmware, which then loads the key for the DES to decrypt succeeding packets.” AV7100 Preview at 33.</p> <p>“UART interfaces The ‘AV7100 includes two general purpose 2-wire UARTs that are memory mapped and fully accessible by application programs. The UARTs operate in asynchronous mode only and support baud rates of 1200, 2400, 4800, 9600, 14400, 19200, 28800, and 57600 kbps. The UARTs are full duplex. The transmitter is double buffered, and the receive interface is buffered with eight bytes of FIFO memory in addition to its internal register. The UARTs transmit/receive 1 start bit, 7 or 8 data bits, optional parity, and 1 or 2 stop bits. The outputs of the UARTs are digital and require external level shifters for RS232 compliance.” AV7100 Preview at 33; see id. at 33-34 (describing additional aspects of the UART interface).</p>

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	<p>“The IR/RF remote control interface is a means of transmitting user commands to the set-top box. This interface consists of a custom hardware receiver implementing a bit frame-based communication protocol. A single bit frame represents a user command. The IR, RF, and REMOTEIN ports require a square wave input with no false transitions; therefore, the signal must reach its threshold prior to being applied to the pins. The interface accepts an IR, RF, or REMOTEIN data stream up to a frequency of 1.3 kHz. Since more than one data stream may be active at any given time, the ‘AV7100 hardware determines priority so that only one IR, RF, or REMOTE input is decoded.” AV7100 Preview at 35; see id. at 35-36 (describing additional aspects of the IR/RF remote control interface).</p>
<p>[1i] a storage subsystem communicatively connected to the media switch, wherein multimedia data are stored on the storage subsystem and retrieved from the storage subsystem essentially simultaneously.</p>	<p>AV7100 Preview discloses or at least renders obvious a storage subsystem communicatively connected to the media switch, wherein multimedia data are stored on the storage subsystem and retrieved from the storage subsystem essentially simultaneously. For example:</p> <p>“1394 Interface Allows Connection to External 1394 Devices” AV7100 Preview at 1.</p> <p>“The 'AV7100 provides a dedicated data interface for 1394 data. To complete the implementation, the 'AV7100 requires external packetizer, link layer, and physical layer devices. . . . The control/command to the packetizer or the link layer interface device is transmitted via the extension bus. The 1394 data is transferred via the 1394 interface, which has 14 signals shown in Table 24..” AV7100 Preview at 51-52.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<div> <pre> graph TD     AV7100["'AV7100"]     ExternalBus["External Bus"]     DVCR["DVCR Packetizer"]     LINK["LINK Interface"]     PHY["PHY Interface"]     Data["Data"]      AV7100 --- ExternalBus     AV7100 --- Data     ExternalBus --- LINK     LINK --- PHY     DVCR --- Data     LINK --- DVCR </pre> <p>Figure 19. 1394 Interface</p> </div> <p>AV7100 Preview at 51 fig. 19.</p> <p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“During decoding, the ‘AV7100 allocates the first 16-Mbit SDRAM for NTSC mode, as shown in Figure 3.” AV7100 Preview at 14; see id. fig. 3 (showing memory allocation of 16-Mbit SDRAM).</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> </ul>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p>“trick mode decoding</p> <p>When decoding a picture from a digital recorder, the ‘AV7100 can process trick modes (decode and display I-frame only), with the limitation that the data must contain the entire frame as opposed to several intra slices. Random bits are allowed in between trick mode pictures. However, if the random bits emulate any start code, this will cause unpredictable decoding and display errors.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I-picture</li> <li>• Ignores the video buffer underflow error</li> <li>• Continuously displays the decoded I-frame” AV7100 Preview at 18.</li> </ul> <p>“The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder AP Is. Consult the TMS320AV7100 Software Guide for details.” AV7100 Preview at 20; see id. tbl. 8 (showing video decoder commands).</p> <p>“In recording mode, the 'AV7100 sends either encrypted or decrypted packets to the 1394 interface. The packet is transferred as it is received. When recording encrypted data, the TPP sends each byte directly to the 1394 interface and bypasses the DES module. In the case of recording decrypted data, the TPP sends that packet payload to the DES module, then forwards a block of packets to the 1394 interface. The 1394 interface transmits this block byte by byte. No processing is done to the packet during recording, except to set the encrypt bit to the proper state. The TPP does not remove the CWP from the auxiliary packet. During playback mode, the packet entering the 1394 interface is transferred directly into the TPP module. In record mode, the packet exiting the TPP may be transferred to the 1394 interface, to the RAM through the traffic controller, or to both places simultaneously. This allows the 'AV7100 to decode one program while recording from 1 to all 32 possible</p>

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	<p>services from a transponder. Figure 20 shows the functional block diagram of the data flow between the TPP, DES, and 1394 interface.” AV7100 Preview at 52; <i>see also id.</i> at 53-54 (showing read and write timing relationships on the 1394 interface).</p> <div> <pre> graph LR     In(( )) --&gt; MUX     In2(( )) --&gt; MUX     MUX --&gt; TPP     TPP &lt;--&gt; DES     TPP --&gt; TC[Traffic Controller]     TC &lt;--&gt; RAM     TC --&gt; I1394[1394 Interface]     I1394 --&gt; MUX     </pre> <p>The diagram illustrates a functional block diagram of data flow. It includes a Multiplexer (MUX) at the top left, a Transponder (TPP) in the center, a Data Encryption Service (DES) block to the right of the TPP, a Traffic Controller block below the TPP, and a Random Access Memory (RAM) block at the bottom. A 1394 Interface block is located to the left of the Traffic Controller. Data flow is indicated by arrows: an external input splits to feed the MUX and the 1394 Interface; the MUX outputs to the TPP; the TPP has bidirectional communication with the DES and sends data to the Traffic Controller; the Traffic Controller has bidirectional communication with the RAM and sends data to the 1394 Interface; the 1394 Interface also feeds back into the MUX.</p> </div> <p>AV7100 Preview at 52 fig. 20.</p> <p>“During recording, it is assumed that input data originates from the FEC device. An FEC error signal sets the DERROR pin at or before the first byte of input data. This DERROR value is sent to the PERROR output on the 1394 interface coincident with the first valid PDATA. The PERROR value remains active as long as the FEC device keeps DERROR active. Typically, the FEC device retains DERROR until the beginning of the following packet. In this case, the 1394 link device may check for record errors at the first data byte of the packet.</p> <p>During playback mode, an error signal can cause an interrupt only once per packet. For the case of an error between packets, the 1394 link device must ensure that the PERROR of the 'AV7100 is held active until the first byte at PDATA is entered. If an error occurs within a packet, the PERROR pin must complete the transition to</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>high before the last byte of the packet is clocked. PERROR must then be returned low before the first byte of the following good packet.” AV7100 Preview at 54.</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“Fully Functional Decoder Using a Single 16-MBit External Synchronous Dynamic Random-Access Memory (SDRAM)” AV7100 Preview at 1.</p> <p>“The ‘AV7100 provides chip select signals for up to two SDRAMs. The minimum SDRAM size required by the decoder is 16 Mbit. Other supported sizes and configurations are:  16 Mbit --7 one 16 Mbit SDRAM  20 Mbit --7 one 16 Mbit and one 4 Mbit SDRAM  32 Mbit --7 two 16 Mbit SDRAM  The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 20 macroblock. The interface also supports decrement mode for bitBLT block transfer.  The two chip selects correspond to the following address ranges:  SCS1 --7 0xCC00 0000 - 0xCC1 F FFFF  SCS2 --7 0xCC20 0000 - 0xCDFF FFFF” AV7100 Preview at 13.</p> <p>“During decoding, the ‘AV7100 allocates the first 16-Mbit SDRAM for NTSC mode, as shown in Figure 3.” AV7100 Preview at 14; see id. fig. 3 (showing memory allocation of 16-Mbit SDRAM).</p> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for</p>

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	<p>initialization and control of the video decoder. The output video is sent to the 'AV7100 on-screen display (OSD) module for further blending with OSD data." AV7100 Preview at 18.</p> <p>"The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The 'AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization." AV7100 Preview at 30.</p> <p>"extension bus read and write timing The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 16-bit data and 25-bit address. . . . Figure 11 and Figure 12 show the timing of a single read and write cycle on the extension bus. The user can program a single or multiple access pattern on the extension bus. Single access implies one access during each chip-select cycle. Multiple access mode allows multiple accesses during one chip select cycle. In this case, the data is latched based upon the programmed wait state." AV7100 Preview at 39.</p> <p><i>See also claim 1 at 1e, supra.</i></p>
Claim 6	
<p>6. The system of claim 1, the decoder subsystem further comprising a transport stream decoder/graphics subsystem.</p>	<p>AV7100 Preview discloses or at least renders obvious the decoder subsystem further comprising a transport stream decoder/graphics subsystem. For example:</p> <p>"Audio Output in Both Pulse Code Modulation (PCM) and SPDIF Formats On-Screen Display (OSD) Processor Enables Mixture of OSD and Video Data With Transparency" AV7100 Preview at 1.</p> <p>"On-Chip NTSC/PAL Encoder Incorporates Closed Caption and Video Aspect Ratio Identification Signal Encoding and the Macrovision® Logic for Anti-Taping Protection Analog Y, C, and Composite Video Outputs With 9-Bit Precision Internally or Externally Generated Video Synchronization Signals Digital Video Component Output That Also Contains Aspect Ratio Identification Code" AV7100 Preview at 1.</p>

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	<p>“Both the video and audio decoders synchronize their presentation using the transmitted PTS. For DSS the PTS is transmitted as picture user data in the video bit stream and as an MPEG-1 system packet bit stream for audio. Dedicated hardware decodes the PTS if it is in the MPEG-1 system packet and forwards it to the audio decoder. The video decoder decodes PTS from picture user data. Both the video and audio decoders compare PTS to the local system clock in order to synchronize presentation of reconstructed data. The local system clock is continuously updated by the ARM.</p> <p>When the PTS and local system clock do not match within tolerance, the video decoder either redisplay or skips a frame. At that time, the CC/EDS is handled as follows:</p> <ul style="list-style-type: none"> <li>• When the video decoder redisplay a frame, the second display does not contain CC/EDS.</li> <li>• When the video decoder skips a frame, the corresponding CC/EDS is also skipped.” AV7100 Preview at 20.</li> </ul> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending them with the video. The OSD module accepts video from the video decoder, reads OSD data from SDRAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces. OSD defaults to standby mode and simply routes video from the video decoder to both outputs. The ARM is responsible for turning on/off OSD operations and for setting specific window attributes of the OSD windows. Dedicated bitBLT hardware attached to the OSD module provides acceleration to memory block moves and graphics operations. OSD data may originate from the user data in the bit stream or may be generated by applications executed on the ARM. Regardless of the source, the OSD data is stored in the SDRAM and managed by the ARM. Memory space in the single 16 Mbits SDRAM is limited to approximately 241 kbytes for OSD, with capability to increase this to approximately 391 kbytes using the half resolution display mode. The OSD data may be represented in one of the following forms: bitmap, graphics 4:4:4 component, 4:2:2 component, or simply background color.” AV7100 Preview at 22; <i>see also id.</i> at 21, 22-24 (describing additional aspects of the OSD module).</p> <p>“The ‘AV7100 provides video output signals encoded for display on a video monitor. The encoded data may include video data or blended video and OSD data. The encoder supports the NTSC format and PAL B, D, G/H and I display formats. The NTSC/PAL pin selects between NTSC and PAL output. Changing between NTSC and PAL requires a hardware reset of the device.</p> <p>The encoder uses 9-bit D/A converters (DACs) to produce an analog S-video signal on separate luminance M and chrominance © channels. An analog composite (Comp) signal is also output. Output signals conform to the RS 170A standard. Application circuits for external connections to the DAG outputs are illustrated in Figure 24. With a single-ended 75 Q load, the output current for peak white is 20 mA.” AV7100 Preview at 26.</p>



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	<p>“The ‘AV7100 also supports various features for video display and control. Closed caption (CC) and Extended Data Services (EDS) information which has been extracted by the video decoder is passed to the ‘AV7100 encoder. The encoder then presents CC data at video line 21 and EDS at video line 284. The video decoder also extracts aspect ratio data from the bit stream and sends it to the ARM, which in turn prepares data according to the video aspect ratio identification signal (VARIS) standard, EIAJ CPX-1204. The ARM forwards VARIS codes to the ‘AV7100 NTSC/PAL module where the codes are inserted onto the 20<sup>th</sup> video line for NTSC and 23<sup>rd</sup> line for PAL.” AV7100 Preview at 26.</p> <p>“The ‘AV7100 provides a digital output interface for pure video or blended video and OSD. The digital output includes video in either 4:4:4 or 4:2:2 YCrCb format. VARIS coding for aspect ratio is also provided at the beginning of each video frame. The video output format is programmable by the user, but defaults to 4:2:2. The pin assignments for the digital video output signals are:  8-bit Cb/Y/Cr/Y and VARIS multiplexed data output  27-MHz or 40.5-MHz clock output  YCOOUT(8)  YCCLK(1)  YCCTRL(2) 2-bit control signals to distinguish between YCrCb components and VARIS code” AV7100 Preview at 26; <i>see also id.</i> at 26-29 (describing additional aspects of the digital video output interface).</p> <p>“PCM audio output  The 2s complement PCM data is output serially on the PCM OUT pin using the serial clock ASCLK. ASCLK is derived from the PCM clock, PCMCLK, according to the PCMSEL 1 :O bits in the control register. The PCM clock  must be the proper multiple of the sampling frequency of the bit stream. The PCMCLK may be input to the device or internally derived from an 36.864-MHz clock. The data on the PCMOUT pin alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7100 Preview at 31; <i>see id.</i> fig. 9 (showing timing for the PCM data).</p> <p>“SPDIF audio output  The SPDIF output conforms to a subset of the AES3 standard for serial transmission of digital audio data. The SPDIF format is a subset of the minimum implementation of AES3.” AV7100 Preview at 31.</p>

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	See claim 1 at 1c, <i>supra</i> , and claim 7, <i>infra</i> .
Claim 7	
7. The system of claim 6, wherein the transport stream decoder/graphics subsystem includes at least one of: a host bridge; a memory controller; an MPEG-3 transport demultiplexer; an MPEG-3 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller.	<p>AV7100 Preview discloses or at least renders obvious the transport stream decoder/graphics subsystem includes at least one of: a host bridge; a memory controller; an MPEG-3 transport demultiplexer; an MPEG-3 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller For example:</p> <p>“On-Chip SDRAM Controller for 16, 20, or 32-MBit SDRAM” AV7100 Preview at 1.</p> <p>“The SDRAM interface supports 16-bit data width SDRAM operating at minimum 81 MHz. The SDRAM selected for use with the ‘AV7100 should meet or exceed the timing requirements in Table 3 for proper operation. The TI TMS626162-12 is one example of a compatible 16 Mbit SDRAM.” AV7100 Preview at 13.</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending them with the video. The OSD module accepts video from the video decoder, reads OSD data from SDRAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces. OSD defaults to standby mode and simply routes video from the video decoder to both outputs. The ARM is responsible for turning on/off OSD operations and for setting specific window attributes of the OSD windows. Dedicated bitBLT hardware attached to the OSD module provides acceleration to memory block moves and graphics operations. OSD data may originate from the user data in the bit stream or may be generated by applications executed on the ARM. Regardless of the source, the OSD data is stored in the SDRAM and managed by the ARM. Memory space in the single 16 Mbits SDRAM is limited to approximately 241 kbytes for OSD, with capability to increase this to approximately 391 kbytes using the half resolution display mode. The OSD data may be represented in one of the following forms: bitmap, graphics 4:4:4 component, 4:2:2 component, or simply background color.” AV7100 Preview at 22; see also id. at 21, 22-24 (describing additional aspects of the OSD module).</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> </ul>

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	<ul style="list-style-type: none"> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware”</li> </ul> <p>AV7100 Preview at 15.</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“Video Decoder Decodes MPEG-1 (Moving Pictures Experts Group) and MPEG-2 Main Profile and Main Level Bit Stream</p> <ul style="list-style-type: none"> <li>• Audio Decoder Decodes MPEG-1 Layer I and II Bit Stream” AV7100 Preview at 1.</li> </ul> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Supports output data in both PCM and SPDIF formats</li> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for sychronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p>“extension bus interface</p> <p>The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus. Each CS has its own defined memory space and a programmable wait register. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. . . .</p> <p>The extension bus supports the connection of seven devices using the predefined chip selects. Additional devices may be used by externally decoding the address bus. Table 21 shows the name of the device, its chip select, address range, and programmable wait state. Table 22 and Table 23 show extension bus wait state and configuration registers. Each device on the extension bus is required to have data outputs in high-impedance state within one clock cycle following the removal of chip-select.” AV7100 Preview at 37.</p>

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	See claim 1 at 1c and claim 6, <i>supra</i> .
Claim 8	
8. The system of claim 7, the transport stream decoder/graphics subsystem further comprising at least one transport stream interface, wherein the transport stream interface receives the transport stream from the input section.	<p>AV7100 Preview discloses or at least renders obvious the transport stream decoder/graphics subsystem further comprising at least one transport stream interface, wherein the transport stream interface receives the transport stream from the input section. For example:</p> <p>“Accepts Transport Bit Stream Up to 40-MBits per Second” AV7100 Preview at 1.</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p> <p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> </ul>

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	<ul style="list-style-type: none"> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware” AV7100 Preview at 15.</li> </ul> <p>“input interface The transport packet data from the FEC device is input to the ‘AV7100 eight bits at a time, using the byte clock, DCLK. A high on PACCLK signals valid packet data. During satellite sourced decode, a DERROR signal is received from the FEC device to indicate that a packet has data errors. The DERROR pin is valid on the first byte or one data byte cycle before the first data byte. It does not change until the following packet.” AV7100 Preview at 16; see also id. at 17 fig. 5 (illustrating input interface timing).</p> <p>“Video Decoder Decodes MPEG-1 (Moving Pictures Experts Group) and MPEG-2 Main Profile and Main Level Bit Stream</p> <ul style="list-style-type: none"> <li>• Audio Decoder Decodes MPEG-1 Layer I and II Bit Stream” AV7100 Preview at 1.</li> </ul> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers 1 and 2</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies, except half frequency</li> <li>• Supports 48-kHz sampling frequency with 36.864 MHz external VCXO</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Supports output data in both PCM and SPDIF formats</li> </ul>

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	<ul style="list-style-type: none"> <li>• Generates the PCM clock or accepts an external clock source</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information” AV7100 Preview at 30.</li> </ul> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p><i>See also</i> claim 1 at 1c and claims 6-7, <i>supra</i>.</p>
Claim 9	
<p>9. The system of claim 7, wherein the transport stream is demultiplexed into audio and video packet streams, wherein the audio and video packet streams are stored and played back through an output side of the transport stream decoder/graphics subsystem.</p>	<p>AV7100 Preview discloses or at least renders obvious the transport stream is demultiplexed into audio and video packet streams, wherein the audio and video packet streams are stored and played back through an output side of the transport stream decoder/graphics subsystem. For example:</p> <p>“input interface The transport packet data from the FEC device is input to the ‘AV7100 eight bits at a time, using the byte clock, DCLK. A high on PACCLK signals valid packet data. During satellite sourced decode, a DERROR signal is received from the FEC device to indicate that a packet has data errors. The DERROR pin is valid on the first byte or one data byte cycle before the first data byte. It does not change until the following packet.” AV7100 Preview at 16; <i>see also id.</i> at 17 fig. 5 (illustrating input interface timing); <i>id.</i> at 54.</p> <p>“The ‘AV7100 accepts a transport bit stream from the output of a forward error correction (FEC) device with a maximum throughput of 40 Mbits/s or 5 Mbytes/s. The transport packet parser (TPP) in the ‘AV7100 processes the header of each packet and extracts only those packets having the specified SCIO numbers. The TPP identifies whether the extracted packet requires further processing by the ARM or whether the packet contains only relevant data and may be routed to SDRAM without ARM intervention. Following interrupt from the TPP, the ARM checks data RAM for packets that need further processing, performs necessary parsing, removes the header, and establishes DMA for transferring payload data from data RAM to SDRAM. The traffic controller repacks the data and removes voids created by the header removal.” AV7100 Preview at 15.</p>

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	<p>“transport packet parser features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream from either the front end device or the 1394 interface</li> <li>• Performs system clock reference recovery</li> <li>• Supports transport streams up to 40 Mbits-per-second</li> <li>• Accepts 8-bit parallel input data</li> <li>• Supports storage of 32 SCIDs (service channel IDs)</li> <li>• Provides lost-packet detection</li> <li>• Provides decrypted or encrypted packets directly to the 1394 interface</li> <li>• Implements internal descrambler for DSS with the Data Encryption Standard implemented in hardware” AV7100 Preview at 15.</li> </ul> <p>“The external SDRAM is used to store system level tables, video and audio bit streams, reconstructed video images, OSD data, and video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware. The traffic controller manages two physical DMA channels, but only one of them, the general purpose DMA, is visible to the user. The user has no knowledge of the DMAs initiated by the transport packet parser, the video and audio decoder, and the OSD module. The general purpose DMA includes ARM-generated and bitBLT-generated DMAs. The traffic controller can accept up to four general DMAs at any given time. Table 2 describes the allowable general purpose DMA transfers.” AV7100 Preview at 12.</p> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.</p> <p>In addition to normal bit stream decoding, the video decoder also extracts the following data fields from the picture layer user data: the closed caption (CC), the extended data services (EDS), the presentation time stamps (PTS) and decode time stamps, the pan_and_scan, the fields display flags, and the no_burst flag. These data fields are specified by the DSS. The CC and EDS are forwarded to the NTSC/PAL encoder module, and the PTS is used for presentation synchronization. The other data fields form DSS-specific constraints on the normal MPEG bit stream, and they are used to update information obtained from the bit stream.” AV7100 Preview at 18.</p>



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	<p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p> <p>“Both the video and audio decoders synchronize their presentation using the transmitted PTS. For DSS the PTS is transmitted as picture user data in the video bit stream and as an MPEG-1 system packet bit stream for audio. Dedicated hardware decodes the PTS if it is in the MPEG-1 system packet and forwards it to the audio decoder. The video decoder decodes PTS from picture user data. Both the video and audio decoders compare PTS to the local system clock in order to synchronize presentation of reconstructed data. The local system clock is continuously updated by the ARM.</p> <p>When the PTS and local system clock do not match within tolerance, the video decoder either redisplay or skips a frame. At that time, the CC/EDS is handled as follows:</p> <ul style="list-style-type: none"> <li>• When the video decoder redisplay a frame, the second display does not contain CC/EDS.</li> <li>• When the video decoder skips a frame, the corresponding CC/EDS is also skipped.” AV7100 Preview at 20.</li> </ul> <p>“The video decoder is capable of producing decimated pictures using <math>\frac{1}{2}</math> or <math>\frac{1}{4}</math> decimation per dimension, which results in reduced areas of <math>\frac{1}{4}</math> or <math>\frac{1}{16}</math>, respectively. The decimated picture can be viewed in real time. Decimation is achieved by using field data out of a frame, skipping lines, and performing vertical filtering to smooth the decimated image.” AV7100 Preview at 19.</p> <p><i>See</i> AV7100 Preview at 19 (describing (1) display formats supported by AV7100, (2) aspect ratio conversion supported by the AV7100).</p> <p>“Audio Output in Both Pulse Code Modulation (PCM) and SPDIF Formats On-Screen Display (OSD) Processor Enables Mixture of OSD and Video Data With Transparency” AV7100 Preview at 1.</p> <p>“On-Chip NTSC/PAL Encoder Incorporates Closed Caption and Video Aspect Ratio Identification Signal Encoding and the Macrovision® Logic for Anti-Taping Protection Analog Y, C, and Composite Video Outputs With 9-Bit Precision Internally or Externally Generated Video Synchronization Signals</p>

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	<p>Digital Video Component Output That Also Contains Aspect Ratio Identification Code” AV7100 Preview at 1.</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending them with the video. The OSD module accepts video from the video decoder, reads OSD data from SDRAM, and directs OSD and/or video output independently to the digital video and NTSC/PAL output interfaces. OSD defaults to standby mode and simply routes video from the video decoder to both outputs. The ARM is responsible for turning on/off OSD operations and for setting specific window attributes of the OSD windows. Dedicated bitBLT hardware attached to the OSD module provides acceleration to memory block moves and graphics operations. OSD data may originate from the user data in the bit stream or may be generated by applications executed on the ARM. Regardless of the source, the OSD data is stored in the SDRAM and managed by the ARM. Memory space in the single 16 Mbits SDRAM is limited to approximately 241 kbytes for OSD, with capability to increase this to approximately 391 kbytes using the half resolution display mode. The OSD data may be represented in one of the following forms: bitmap, graphics 4:4:4 component, 4:2:2 component, or simply background color.” AV7100 Preview at 22; see also id. at 21, 22-24 (describing additional aspects of the OSD module).</p> <p>“The ‘AV7100 provides video output signals encoded for display on a video monitor. The encoded data may include video data or blended video and OSD data. The encoder supports the NTSC format and PAL B, D, G/H and I display formats. The NTSC/PAL pin selects between NTSC and PAL output. Changing between NTSC and PAL requires a hardware reset of the device.</p> <p>The encoder uses 9-bit D/A converters (DACs) to produce an analog S-video signal on separate luminance M and chrominance © channels. An analog composite (Comp) signal is also output. Output signals conform to the RS 170A standard. Application circuits for external connections to the DAG outputs are illustrated in Figure 24. With a single-ended 75 Q load, the output current for peak white is 20 mA.” AV7100 Preview at 26.</p> <p>“The ‘AV7100 also supports various features for video display and control. Closed caption (CC) and Extended Data Services (EDS) information which has been extracted by the video decoder is passed to the ‘AV7100 encoder. The encoder then presents CC data at video line 21 and EDS at video line 284. The video decoder also extracts aspect ratio data from the bit stream and sends it to the ARM, which in turn prepares data according to the video aspect ratio identification signal (VARIS) standard, EIAJ CPX-1204. The ARM forwards VARIS codes to the ‘AV7100 NTSC/PAL module where the codes are inserted onto the 20th video line for NTSC and 23rd line for PAL.” AV7100 Preview at 26.</p>

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	<p>“The ‘AV7100 provides a digital output interface for pure video or blended video and OSD. The digital output includes video in either 4:4:4 or 4:2:2 YCrCb format. VARIS coding for aspect ratio is also provided at the beginning of each video frame. The video output format is programmable by the user, but defaults to 4:2:2. The pin assignments for the digital video output signals are:  8-bit Cb/Y/Cr/Y and VARIS multiplexed data output  27-MHz or 40.5-MHz clock output  YCOUT(8)  YCCLK(1)  YCCTRL(2) 2-bit control signals to distinguish between YCrCb components and VARIS code” AV7100 Preview at 26; see also id. at 26-29 (describing additional aspects of the digital video output interface).</p> <p>“PCM audio output  The 2s complement PCM data is output serially on the PCM OUT pin using the serial clock ASCLK. ASCLK is derived from the PCM clock, PCMCLK, according to the PCMSEL 1 :O bits in the control register. The PCM clock must be the proper multiple of the sampling frequency of the bit stream. The PCMCLK may be input to the device or internally derived from an 36.864-MHz clock. The data on the PCMOUT pin alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7100 Preview at 31; see id. fig. 9 (showing timing for the PCM data).</p> <p>“SPDIF audio output  The SPDIF output conforms to a subset of the AES3 standard for serial transmission of digital audio data. The SPDIF format is a subset of the minimum implementation of AES3.” AV7100 Preview at 31.</p> <p><i>See also</i> claim 1 at 1a, 1c-1i, and claims 6-8, <i>supra</i>.</p>
Claim 10	
10. The system of claim 7, further comprising a SDRAM connected to the transport stream decoder/graphics subsystem.	<p>AV7100 Preview discloses or at least renders obvious a SDRAM connected to the transport stream decoder/graphics subsystem. For example:</p> <p>“Fully Functional Decoder Using a Single 16-MBit External Synchronous Dynamic Random-Access Memory (SDRAM)” AV7100 Preview at 1.</p>

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	<p>“The ‘AV7100 provides chip select signals for up to two SDRAMs. The minimum SDRAM size required by the decoder is 16 Mbit. Other supported sizes and configurations are:  16 Mbit --7 one 16 Mbit SDRAM  20 Mbit --7 one 16 Mbit and one 4 Mbit SDRAM  32 Mbit --7 two 16 Mbit SDRAM  The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 20 macroblock. The interface also supports decrement mode for bitBLT block transfer.  The two chip selects correspond to the following address ranges:  SCS1 --7 0xCC00 0000 - 0xCC1 F FFFF  SCS2 --7 0xCC20 0000 - 0xCDF FFFF” AV7100 Preview at 13.</p> <p>“During decoding, the ‘AV7100 allocates the first 16-Mbit SDRAM for NTSC mode, as shown in Figure 3.” AV7100 Preview at 14; <i>see id.</i> fig. 3 (showing memory allocation of 16-Mbit SDRAM).</p> <p>“The video decoder reads the video bit stream from the external SDRAM and processes it according to ISO standards. The ‘AV7100 decodes MPEG-1 and MPEG-2 main profile at main level. The decoding process is controlled by a RISC engine that accepts high-level commands from the ARM. The ARM functions as a host for initialization and control of the video decoder. The output video is sent to the ‘AV7100 on-screen display (OSD) module for further blending with OSD data.” AV7100 Preview at 18.</p> <p>“The audio decoder reads audio packet data from the external SDRAM and processes the data according to ISO standards. The ‘AV7100 decodes Layer I and II MPEG-1 audio data and outputs audio in PCM and SPDIF formats. PTS information is extracted from audio packet headers and used for audio synchronization.” AV7100 Preview at 30.</p>

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	<p>AV7100 Preview at 9 fig. 1.</p> <p>See claim 1 at 1c and 1i, and claims 6-9, <i>supra</i>.</p>
Claim 11	
11. The system of claim 1, wherein the processor is	AV7100 Preview discloses or at least renders obvious the processor is operative to run system software, middleware, and application software. For example:

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operative to run system software, middleware, and application software.	<p>“The ARM is responsible for managing all hardware and software resources in the ‘AV7100. At powerup the ARM verifies the size of external memory. It then initializes all ‘AV7100 hardware modules by setting up control registers and tables and by resetting data pointers. The ARM then executes the default firmware. All firmware is stored in on-chip ROM, except the OSD graphics and some generic run-time support. The run-time support library (RTSL) and all user application software are stored outside the ‘AV7100 in external memory attached to the extension bus. Details of the firmware, RTSL, and application program interface (API) are provided in the companion software document, TMS320AV7100 Software Guide.</p> <p>Based on programmable priority, the ARM responds to interrupt requests generated by internal modules and external devices on the extension bus. Some of the requests are for data transfers to internal RAM, whereas others are true interrupts to the ARM. The 'AV7100s traffic controller handles data transfers, and the ARM provides services to true interrupts. Interrupts are grouped into FIQ and IRQ categories. The system software uses FIQ; the application software uses IRQ. The priorities for FIQs and IRQs are managed by the firmware.” AV7100 Preview at 11.</p> <p>“The ARM initializes and controls the audio decoder via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and oversampling ratio, and choose the output format for dual channel mode. The ARM also reads status information from the audio decoder via a 32-bit status register which provides the MPEG header information and sync, CRC, and PCM status.” AV7100 Preview at 30.</p> <p><i>See</i> AV7100 Preview at 20 tbl. 8 (listing use of OSD API).</p> <p>“The audio module has two registers: a read/write control register and a read-only status register. Both registers are read or written to through user software and 'AV7100 API routines.” AV7100 Preview at 31.</p> <p>“The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder APIs. . . .” AV7100 Preview at 20.</p> <p>“The 'AV7100 includes an interface to the smart card access control system. The interface consists of a high-speed UART and logic to comply with the News Datacom specification (Document #HU-T052, Release E, dated November 1994, and Release F, dated January 1996) ‘DirecTV Project: Decoder-Smart Card Interface Requirements.’ Applicable software drivers that control the interface are also included, and detailed in the companion software document for the 'AV7100.” AV7100 Preview at 33.</p>

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	<p>“The conditional access is triggered by the arrival of a control word packet (CWP). The ARM firmware recognizes that a CWP has been received and passes it to the verifier, which is the user-implemented News Datacom application software running on the ARM. The verifier reads the CWP and communicates with the external smart card through a UART I/O interface. After verification, it passes the pointer to an 8-byte key back to the firmware, which then loads the key for the DES to decrypt succeeding packets.” AV7100 Preview at 33.</p> <p>“To put the device in slave mode the application program must set the slave mode select and a 7-bit address for the 'AV7100. The application must also send a software reset to the 12C to complete the transition to slave mode.” AV7100 Preview at 37.</p> <p>“The initialization software should specify the data size of the device connected to the CS2 to CS6. CS1 and DRAM are always size 16, but CS2 to CS6 (including the parallel data port) can be programmed as a size 8 or size 16 interface. The extension bus interface does the routing between the internal 32-bit data and the 8-bit or 16-bit data on the extension bus. For example, the user program can write a word to an 8-bit device on the extension bus, and the extension bus interface performs four consecutive byte writes.” AV7100 Preview at 43.</p> <p>“device control interfaces reset The 'AV7100 requires a hardware reset on powerup. Reset of the device is initiated by pulling the RESET pin low for at least 100 ns while the clock is running. The following actions will then occur:</p> <ul style="list-style-type: none"> <li>• Input data on all ports is ignored.</li> <li>• External memory is sized.</li> <li>• Data pointers are reset.</li> <li>• All modules are initialized and set to a default state.</li> </ul> <p>TPP tables are initialized. Audio decoder is set for 16 bit output with 256 x oversampling. OSD background color is set to blue and video data is selected for the analog and digital outputs. Macrovision is disabled. The 12C port is set to master mode. When the reset sequence completes, the device will begin to accept data. All data input prior to the end of the reset sequence is ignored.” AV7100 Preview at 55.</p>

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	<p>“Firmware Controls Device Operation and Provides Application Access to Hardware Resources” AV7100 Preview at 1.</p> <p><i>See claim 1 at 1b, supra.</i></p>
Claim 14	
<p>14. The system of claim 11, wherein the system software includes at least: an operating system kernel and device drivers, the system software operative to initialize and control hardware components.</p>	<p>AV7100 Preview discloses or at least renders obvious the system software includes at least: an operating system kernel and device drivers, the system software operative to initialize and control hardware components. For example:</p> <p>“The ARM is responsible for managing all hardware and software resources in the ‘AV7100. At powerup the ARM verifies the size of external memory. It then initializes all ‘AV7100 hardware modules by setting up control registers and tables and by resetting data pointers. The ARM then executes the default firmware. All firmware is stored in on-chip ROM, except the OSD graphics and some generic run-time support. The run-time support library (RTSL) and all user application software are stored outside the ‘AV7100 in external memory attached to the extension bus. Details of the firmware, RTSL, and application program interface (API) are provided in the companion software document, TMS320AV7100 Software Guide. Based on programmable priority, the ARM responds to interrupt requests generated by internal modules and external devices on the extension bus. Some of the requests are for data transfers to internal RAM, whereas others are true interrupts to the ARM. The 'AV7100s traffic controller handles data transfers, and the ARM provides services to true interrupts. Interrupts are grouped into FIQ and I RQ categories. The system software uses FIQ; the application software uses IRQ. The priorities for FIQs and IRQs are managed by the firmware.” AV7100 Preview at 11.</p> <p>“The ARM initializes and controls the audio decoder via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and oversampling ratio, and choose the output format for dual channel mode. The ARM also reads status information from the audio decoder via a 32-bit status register which provides the MPEG header information and sync, CRC, and PCM status.” AV7100 Preview at 30.</p> <p><i>See AV7100 Preview at 20 tbl. 8 (listing use of OSD API).</i></p>



'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The audio module has two registers: a read/write control register and a read-only status register. Both registers are read or written to through user software and 'AV7100 API routines.” AV7100 Preview at 31.</p> <p>“The video decoder accepts the high-level commands detailed in Table 8. Commands are executed via the user software and its implementation of the video decoder APIs. . . .</p> <p>The half resolution display mode stores and displays only one field of B frame. The same field is displayed twice for the interlaced frame. The same field is repeatedly displayed during the 3:2 pulldown case. The user controls this mode via software using the video decoder commands HalfResOn and HalfResOff.” AV7100 Preview at 20.</p> <p>“The 'AV7100 includes an interface to the smart card access control system. The interface consists of a high-speed UART and logic to comply with the News Datacom specification (Document #HU-T052, Release E, dated November 1994, and Release F, dated January 1996) ‘DirecTV Project: Decoder-Smart Card Interface Requirements.’ Applicable software drivers that control the interface are also included, and detailed in the companion software document for the 'AV7100.” AV7100 Preview at 33.</p> <p>“The conditional access is triggered by the arrival of a control word packet (CWP). The ARM firmware recognizes that a CWP has been received and passes it to the verifier, which is the user-implemented News Datacom application software running on the ARM. The verifier reads the CWP and communicates with the external smart card through a UART 1/0 interface. After verification, it passes the pointer to an 8-byte key back to the firmware, which then loads the key for the DES to decrypt succeeding packets.” AV7100 Preview at 33.</p> <p>“To put the device in slave mode the application program must set the slave mode select and a 7-bit address for the 'AV7100. The application must also send a software reset to the 12C to complete the transition to slave mode.” AV7100 Preview at 37.</p> <p>“The initialization software should specify the data size of the device connected to the CS2 to CS6. CS1 and DRAM are always size 16, but CS2 to CS6 (including the parallel data port) can be programmed as a size 8 or size 16 interface. The extension bus interface does the routing between the internal 32-bit data and the 8-bit or 16-bit data on the extension bus. For example, the user program can write a word to an 8-bit device on the extension bus, and the extension bus interface performs four consecutive byte writes.” AV7100 Preview at 43.</p> <p>“device control interfaces reset</p>

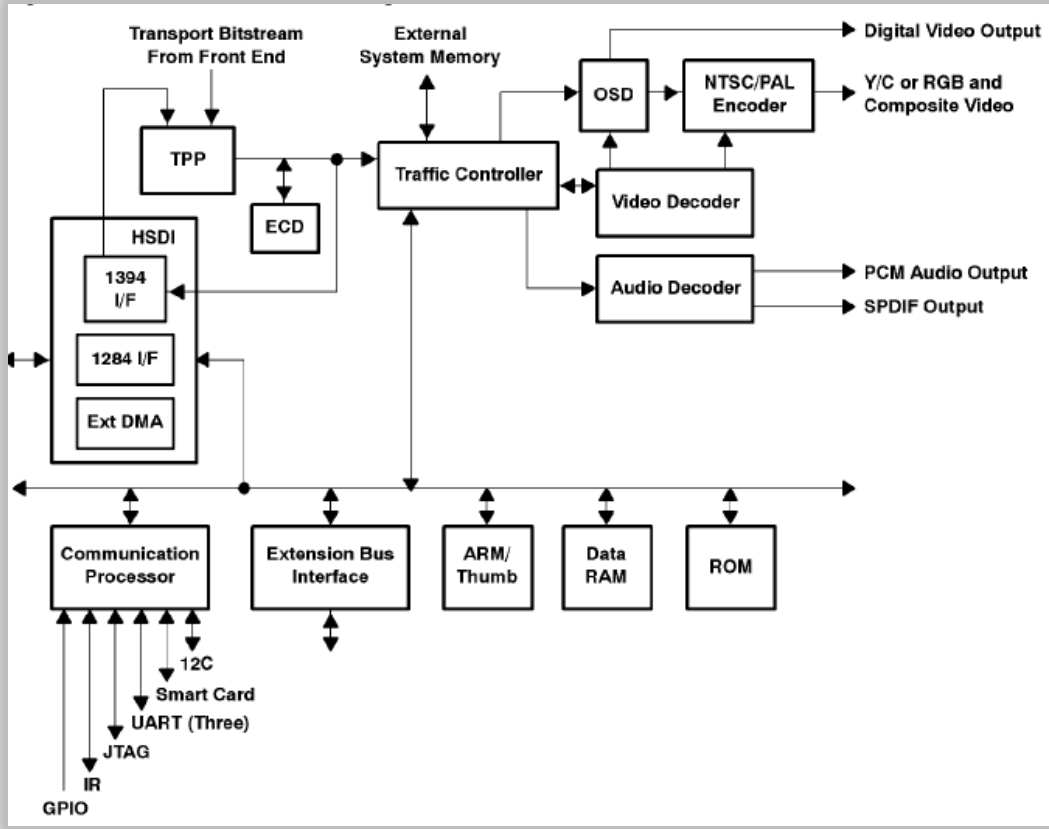
'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>The 'AV7100 requires a hardware reset on powerup. Reset of the device is initiated by pulling the RESET pin low for at least 100 ns while the clock is running. The following actions will then occur:</p> <ul style="list-style-type: none"> <li>• Input data on all ports is ignored.</li> <li>• External memory is sized.</li> <li>• Data pointers are reset.</li> <li>• All modules are initialized and set to a default state.</li> </ul> <p>TPP tables are initialized.  Audio decoder is set for 16 bit output with 256 x oversampling.  OSD background color is set to blue and video data is selected for the analog and digital outputs.  Macrovision is disabled.  The 12C port is set to master mode.  When the reset sequence completes, the device will begin to accept data. All data input prior to the end of the reset sequence is ignored.” AV7100 Preview at 55.</p> <p><i>See claim 1 at 1b and claim 11, supra.</i></p>
Claim 13	
<p>13. The system of claim 1, further comprising a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in the media switch.</p>	<p>AV7100 Preview discloses or at least renders obvious a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in the media switch. For example:</p> <p>“extension bus interface  The extension bus interface is a 16-bit bidirectional data bus with a 25-bit address for byte access. It also provides a wait line and three external interrupts, each with its own acknowledge signal. All the external memories or input/output devices are mapped to the 32-bit address space of the ARM. There are seven internally generated chip selects (CS) which may be used to select EEPROM memory, DRAM, modem, front panel, front end control, parallel output port, and 1394 link device or other devices that reside on the extension bus. Each CS has its own defined memory space and a programmable wait register. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space.” AV7100 Preview at 37.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure																																
	<div><p><b>Table 21. Extension Bus Chip Selects</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 MBytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 32 MBytes)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7100 Preview at 37 tbl. 21.</p> <p><i>See also</i> claim 1 at 1d, <i>supra</i>.</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 MBytes)	N/A	2E00 0000 – 2FFF FFFF	N/A	DRAM (up to 32 MBytes)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE																														
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CS2	3000 0000 – 31FF FFFF	1 – 7	Modem																														
CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel																														
CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device																														
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device																														
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port																														

**Invalidity Contentions for U.S. Patent No. 8,457,476****Based on “Product Preview: TMS320AV7110 Integrated Digital Set-top Box Decoder” (“AV7110 Preview”)**

Based upon TiVo’s Complaint, Infringement Contentions, and apparent claim constructions and application of the claims to Samsung’s accused products, as best as they can be deciphered, the reference charted below anticipates or at least renders obvious the asserted claims. These invalidity contentions are not an admission by Samsung that the accused products are covered by, or infringe the asserted claims, particularly when these claims are properly construed and applied. These invalidity contentions are not an admission that Samsung concedes or acquiesces to any claim construction implied or suggested by TiVo’s Complaint or Infringement Contentions. Nor is Samsung asserting any claim construction positions through these charts, including whether the preamble is a limitation. The portions of the prior art reference cited below are not exhaustive but are exemplary in nature.

<b>’476 Patent Claim</b>	<b>Exemplary Prior Art Disclosure</b>
<b>Claim 1</b>	
[1p] A system for the simultaneous storage and retrieval of multimedia data, comprising:	<p>To the extent that the preamble is limiting, the AV7110 Preview discloses or at least renders obvious a system for the simultaneous storage and retrieval of multimedia data. For example:</p> <p>“The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO), and MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infra-red (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.” AV7110 Preview at 1.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	 <p>The diagram illustrates the AV7110 system architecture. A 'Transport Bitstream From Front End' enters a 'TPP' (Transport Processing Processor) block. The TPP is connected to an 'HSDI' (High-Speed Data Interface) block, which contains '1394 I/F', '1284 I/F', and 'Ext DMA' components. The HSDI is connected to a 'Traffic Controller' block. The Traffic Controller is also connected to 'External System Memory' and an 'OSD' (On-Screen Display) block. The Traffic Controller outputs to a 'Video Decoder' and an 'Audio Decoder'. The Video Decoder outputs to the OSD, which then feeds into an 'NTSC/PAL Encoder'. The NTSC/PAL Encoder produces 'Digital Video Output' and 'Y/C or RGB and Composite Video'. The Audio Decoder produces 'PCM Audio Output' and 'SPDIF Output'. The Traffic Controller is also connected to a 'Communication Processor' block, which interfaces with 'GPIO', 'IR', 'JTAG', 'UART (Three)', 'Smart Card', and '12C'. The Communication Processor is connected to an 'Extension Bus Interface' block, which in turn connects to 'ARM/Thumb', 'Data RAM', and 'ROM' blocks.</p> <p>AV7110 Preview at 12 fig. 1.</p> <p>“After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards.” AV7110 Preview at 13.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PIO table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.</p> <p>The only difference between the two scenarios is that in the case where there is no TPP traffic, the TPP buffer pool can be used. In the case where there is active TPP data, a general purpose buffer needs to be used. Additionally, when TPP data traffic is active, the end of packet (EOP) interrupt generation will require an indication data type configured in the header, which describes where the data to be processed is to be found.” AV7110 Preview at 21.</p> <p>“trick mode</p> <p>When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error</li> <li>• Continuously displays the decoded I frame.” AV7110 Preview at 26; <i>see id.</i> tbl. 6 (showing video decoder commands enabling trick mode functionality).</li> </ul> <p>“The HSDI supports the following concurrent data transfers.</p> <ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/program to 1394 (using dedicated I/F - see NOTE XXXX of Table 29)</li> <li>• TPP/program to decoder; 1394/OMA to/from memory</li> </ul>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• TPP/program to decoder; memory/DMA to/from HSDI</li> <li>• TPP/program to decoder; TPP/DMA to HSDI</li> <li>• TPP/program to decoder; TPP/program to 1394; memory/DMA to/from 1394</li> <li>• TPP/program to decoder; 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; TPP/DMA to 1394” AV7110 Preview at 61.</li> </ul> <p>AV7110 Preview at 61 (showing the functional blocks of the HSDI); <i>see also id.</i> at 62-65 (showing describing AV7110's reading and writing of data from/to the 1394 interface).</p> <p>“AV7110 internal data path for 1394</p> <p>In recording mode, the 'AV7110 sends either encrypted or clean packets to the 1394 interface. The packet will be transferred as soon as it arrives. When recording encrypted data, the ECO module is bypassed. In the case of recording decrypted byte, the TPP sends the encrypted part of the payload to the ECD module, and then forwards each byte to the 1394 interface. No CPU processing is done to the packet during recording. The TPP automatically modifies the header if the packet is decrypted.</p> <p>Note that the same team cannot be sent to the 1394 interface twice (such as, once after decryption, and twice as part of a full transport stream with the by-pass capability). Both Timon and the 'AV7110 support only one MPEG-2 transport stream channel on the bulky data interface.</p> <p>During playback mode, MPEG-2 transport packets coming from the 1394 interface go directly to the TPP module.</p> <p>Figure 29 shows the functional block diagram of the data flow between the TPP, ECD, and 1394 interface. Note that the major portion of the 1394 interface function is implemented in the HSDI module. Dedicated data lines are used for the 1394 interface that allows the 'AV7110 to work in different modes.</p> <ul style="list-style-type: none"> <li>• Decode/decrypt/display one channel and record it</li> <li>• Decode/decrypt/display one channel and record it encrypted (pay-per-view)</li> <li>• Decode/display one channel while recording all or part of 32 PIDs from a transponder, with each selected PIDs either encrypted or decrypted. In addition non selected PIDs can also be recorded in their original format (decryption is not possible for non selected PIDs).</li> <li>• While the TPP is receiving MPEG-2 data from the 1394 port, the 'AV7110 can also record part of the bit stream it is receiving to the 1394 port</li> </ul>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Send the whole transport stream from the FEC to the 1394 port without any filtering or decryption and, at the same time, decode/decrypt/display a program from either the same transport stream or from another transport stream received through the 1394 port.” AV7110 Preview at 65.</li> </ul> <p>AV7110 Preview at 65 fig. 29 (showing functional block diagram of data flow between TPP, ECD, and 1394 interface).</p> <p>“When configured for EDMA operation (HSDI_ STATUS[1 LO] = 01), the HSDI is capable of a glue less connection to an external enhanced SCSI controller (ESC) device such as the NCR 53CF94-1 /53CF96-1. Figure 30 shows the connections for this example configuration.</p> <p>....</p> <p>Since there is only an 8-bit bus on the HSDI, the ESC is limited to an 8-bit, single bus architecture so its mode selection inputs should be set to mode 0. The upper data bits can be left floating since they have internal pullups on the ESC. Likewise, the AD?-0 inputs of the ESC will not be used for this mode and can be left unconnected. The ESC requires an external clock source from 10 MHz to 40 MHz. Since the CLK40 signal of the 'AV7110 is actually a 40.5 MHz clock it cannot be used directly for this controller without violating its specification. Table 32 shows the signals needed for the EDMA interface.</p> <p>....</p> <p>All data transfers (using the HSDI DMA unit) as well as external controller communications (using the A[3:0] output signals), are controlled by the firmware. Firmware will handle MPEG-2 program stream and MPEG-1 system stream input. This firmware will not be available with the initial samples of the 'AV7110. The other input data formats will be handled by user application software. This includes specific interfaces such as the ESC. Table 33 details the EDMA register which allows the user to configure the wait states and other factors of the EDMA port.” AV7110 Preview at 66-67.</p>

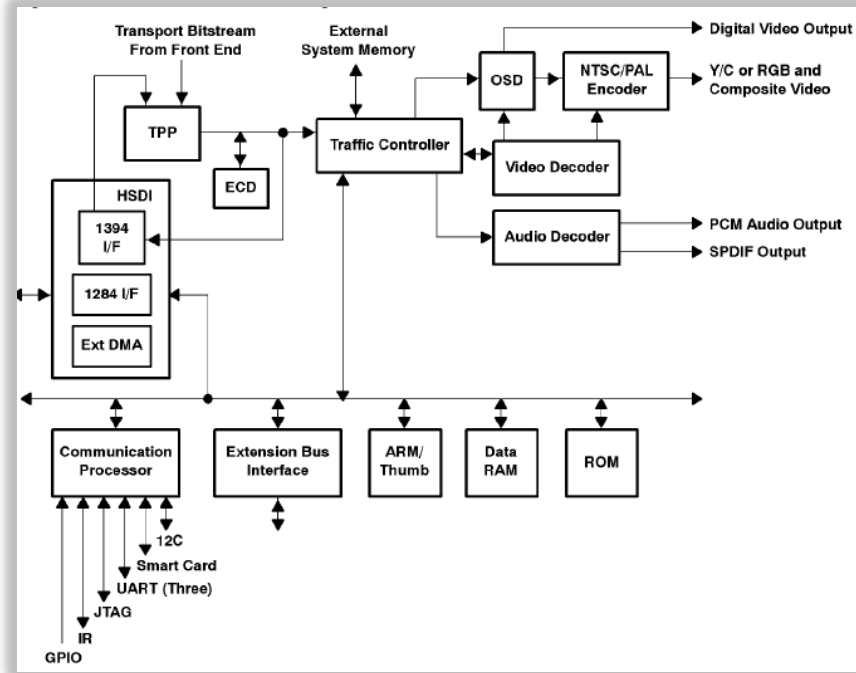


'476 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p>The diagram, labeled 'Figure 26. 1394 Interface', shows a block diagram of the AV7100 system. At the top is a large rectangle labeled 'AV7100'. Below it, on the left, is a vertical line labeled 'External Bus'. To the right of this bus is a vertical stack of three boxes: 'DVCR Packetizer' at the top, 'LINK Interface' in the middle, and 'PHY Interface' at the bottom. A line connects the 'External Bus' to the 'LINK Interface'. To the right of the 'DVCR Packetizer' is a box labeled 'Data BD Port'. A line connects the 'Data BD Port' to the 'DVCR Packetizer'. Below the 'LINK Interface' is a box labeled 'TIMON (TSB12LV41)'. A line connects the 'LINK Interface' to the 'TIMON' box. Below the 'PHY Interface' is a box labeled '1394 Port 1', '1394 Port 2', and '1394 Port 3'. A line connects the 'PHY Interface' to this box.</p> </div> <p>AV7110 Preview at 62 fig. 26 (showing connection between AV7110 and external packetizer, link layer controller, and physical layer device); <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) packets to and from the internal data RAM. This data can then be processed by the user software as needed.”).</p> <p>“The application software interfaces with the peripheral interface controller via RTSL API calls. To send data to the host the application software will issue an API call to transfer the data from memory to the peripheral interface via a DMA. To receive data from the host, the application software will issue an API to transfer a predetermined number of bytes from the peripheral interface to internal data memory via the HSDI DMA unit. The user application software must have a way to determine the number of bytes of data that is expected from the host.” AV7110 Preview at 70.</p> <p><i>See claim 1 at 1j, infra.</i></p>

'476 Patent Claim	Exemplary Prior Art Disclosure
<p>[1a] an input section that acquires an input signal, the input section creates a transport stream from the input signal;</p>	<p>AV7110 Preview discloses or at least renders obvious an input section that acquires an input signal, the input section creates a transport stream from the input signal. For example:</p> <p>“The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO), and MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infra-red (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.” AV7110 Preview at 1.</p> <p>“transport parser input interface The ‘AV7110 accepts DVB transport packet data from a front end such as a Forward Error Correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB Conditional Access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23; <i>see also id.</i> at 24 tbl. 4 (describing transport packet input interface pin description).</p>

## '476 Patent Claim

## Exemplary Prior Art Disclosure



AV7110 Preview at 12 fig. 1.

“The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.” AV7110 Preview at 13.

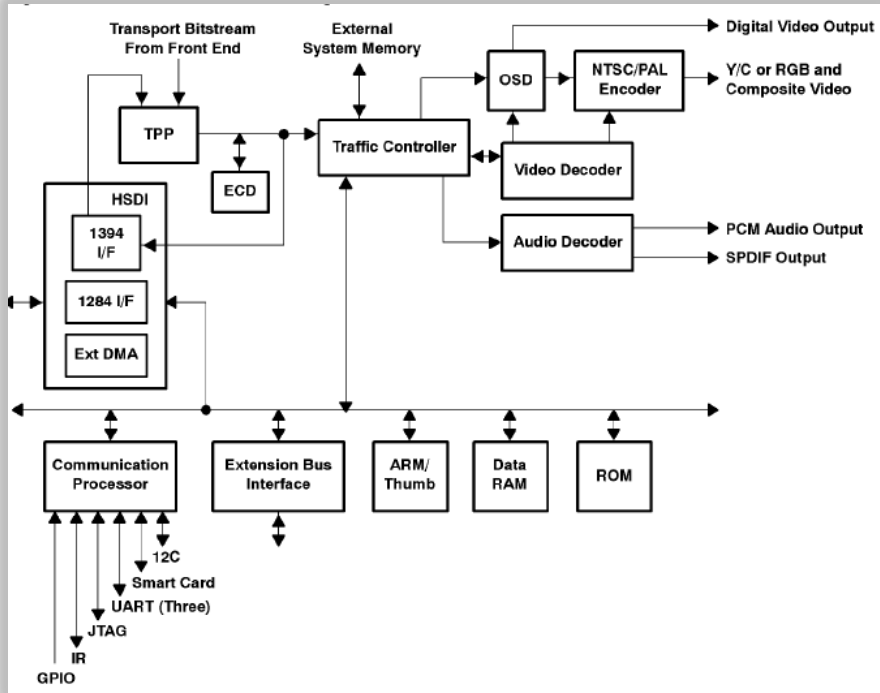
“The TPP hardware is capable of detecting packets lost from the transport stream. With error concealment by the audio and the video decoders the 'AV7110 minimizes the effect of lost data.” AV7110 Preview at 13.

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM  Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PIO table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.” AV7110 Preview at 21.</p> <p>“MPEG transport decoder (TPP)  TPP module  features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15  Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>Maximum number of pairs of keys for the descrambler ..... 16</p> <p>Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination.</p> <p>The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p>
[1b] a processor;	<p>AV7110 Preview discloses or at least renders obvious a processor. For example:</p> <p>AV7110 Preview at 1 (listing a “32/16 Bit ARM/Thumb Processor” as one of the components present in the TMS320AV7110 decoder chip).</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“ARM CPU features</p> <ul style="list-style-type: none"> <li>• Runs at 40.5 MHz</li> <li>• Supports byte (8-bit), half-word (16-bit), and word (32-bit) data types</li> <li>• Reads instructions from on-chip ROM or from the extension bus</li> <li>• Can switch between ARM (32-bit) or Thumb (16-bit) instruction mode</li> <li>• 32-bit data and 32-bit address lines</li> <li>• 7 processing modes</li> <li>• Two interrupts, FIQ and IRO</li> </ul> <p>The 32-bit ARM processor running at 40.5 MHz and its associated firmware provide the following:</p> <ul style="list-style-type: none"> <li>• Initialization and management of all hardware modules</li> <li>• Service for selected interrupt generated by hardware modules and I/O ports</li> <li>• Application program interface (API) for users to develop their own applications”</li> </ul> <p>AV7110 Preview at 15.</p> <p>“The CPU in the 'AV7110 is a 32-bit RISC processor, the ARM7TDM I/Thumb, which has the capability to execute instructions in 16- or 32-bit format at a clock frequency of 40.5 MHz. The regular ARM instructions are exactly one word (32-bit) long, and the data operations are only performed on word quantities. The LOAD and STORE instructions however, can transfer either byte, half-word or word quantities.</p> <p>The Thumb uses the same 32-bit architecture with an 16-bit instruction set. That is, it retains the 32-bit performance but reduces the code size with 16-bit instructions. With 16-bit instruction, the Thumb still gives 70-80% of the performance of the ARM when running ARM instructions from 32-bit memory.” AV7110 Preview at 15; <i>see also id.</i> (stating that ARM and Thumb are used interchangeably in the AV7110 Preview’s disclosure).</p> <p>“ARM uses a LOAD and STORE architecture, that is, all operations are on the registers. ARM has 7 different processing modes with 16, 32-bit registers visible in user mode. In the Thumb state, there are only 8 registers available in user mode. The high registers may still be accessed through special instructions in this case. The instruction pipeline is three stage, fetch ~ decode ~ execute, and most instructions only take one cycle to execute. Figure 3 shows the data path of ARM processor core.” AV7110 Preview at 16.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p>The diagram illustrates the ARM Core Data Path. It features a Register Bank on the left, a Barrel Shifter in the upper middle, a Booth Multiplier in the lower middle, and an ALU on the right. The Register Bank is connected to the Barrel Shifter via a B-Bus. The Register Bank is also connected to the ALU via an A-Bus. The Barrel Shifter is connected to the ALU. The Booth Multiplier is connected to the ALU. The ALU is connected to the Register Bank via an ALU-Bus. The ALU-Bus is also connected to the Booth Multiplier.</p> <p style="text-align: center;"><b>Figure 3. ARM Core Data Path</b></p> </div> <p>AV7110 Preview at 16 fig. 3 (figure showing data path of the ARM Core); <i>see id.</i> (describing ARM CPU's performance of hardware and software resource management).</p>
[1c] a decoder subsystem that decodes the transport stream, the decoder subsystem is communicatively connected to the processor;	<p>AV7110 Preview discloses or at least renders obvious a decoder subsystem that decodes the transport stream, the decoder subsystem is communicatively connected to the processor. For example:</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	 <p>The diagram illustrates the AV7110 system architecture. A 'Transport Bitstream From Front End' enters a 'TPP' (Transport Packet Processor) block. The TPP is connected to an 'HSDI' block containing '1394 I/F', '1284 I/F', and 'Ext DMA'. The HSDI block is connected to a 'Traffic Controller' block. The Traffic Controller is also connected to 'External System Memory' and an 'ECD' (Error Correction Decoder) block. The Traffic Controller outputs to a 'Video Decoder' and an 'Audio Decoder'. The Video Decoder is connected to an 'OSD' (On-Screen Display) block and an 'NTSC/PAL Encoder'. The Audio Decoder outputs to 'PCM Audio Output' and 'SPDIF Output'. The Video Decoder also outputs to 'Digital Video Output' and 'Y/C or RGB and Composite Video'. The Traffic Controller is connected to a 'Communication Processor' block, which is further connected to 'GPIO', 'IR', 'JTAG', 'UART (Three)', 'Smart Card', and '12C'. The Communication Processor is also connected to an 'Extension Bus Interface' block, which is connected to 'ARM/Thumb', 'Data RAM', and 'ROM'.</p> <p>AV7110 Preview at 12 fig. 1.</p> <p>“After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards. The chip decodes MPEG-1 and MPEG-2 main profile at main level for video and Layer I and II MPEG-1 and MPEG-2 stereo for audio. Both video and audio decoders synchronize their presentation of reconstructed data using the transmitted presentation time stamps (PTS) and their local system clock. The local system clock is continuously updated by the ARM.” AV7110 Preview at 13.</p> <p>“video decoder features</p> <ul style="list-style-type: none"> <li>• Real-time decoding of MPEG-2 Main Profile@Main level and MPEG-1 video bit-streams</li> <li>• Error detection and concealment</li> </ul>



'476 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Internal 90 kHz/27 MHz system time clock</li> <li>• Sustained input rate of 15 Mbps</li> <li>• Supports trick mode with full size trick mode picture</li> <li>• Provides 1/4 and 1/16 decimated size picture</li> <li>• Extracts closed caption and other picture user data from the bit-stream</li> <li>• 3:2 pulldown in NTSC mode</li> <li>• Provides read access to video input buffer's read/write pointers</li> <li>• Pan-and-scan for 16:9 and 20:9 source material according to MPEG syntax</li> <li>• Letterbox support</li> <li>• High level command interface</li> <li>• Synchronization using presentation time stamps (PTS); also supports VBV delay based and free run (no synchronization) video playback</li> <li>• Supports the following display format with polyphase horizontal resampling and vertical chrominance filtering.” AV7110 Preview at 25.</li> </ul> <p>“The video decoder module receives a video bit-stream from the SDRAM. It also uses the SDRAM as its working memory to store tables, buffers, and reconstructed images. The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.</p> <p>The 'AV7110 synchronizes the presentation of video with the audio using the transmitted PTS which are extracted by the ARM from the PES packets. it compares the PTS with the local system time clock (STC) and performs synchronization recovery if the difference is outside of a user programmable threshold range given as follows:</p> $STC - \text{threshold} < PTS < STC + \text{threshold}$ <p>If synchronization recovery is needed, the video decoder will either redisplay or skip a frame, depending on the PTS value. If the PTS lags, that is, the time for displaying the current picture has already passed, the video decoder discards the following B pictures without decoding them until the PTS catches up with the STC. If the PTS leads, that is, the time for displaying the current picture has not arrived yet, the video decoder pauses the decoding and continuously displays the last picture (see Synchronization for more details).” AV7110 Product Preview at 25-26.</p> <p>“trick mode</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur.</p> <p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error</li> <li>• Continuously displays the decoded I frame.” AV7110 Preview at 26; <i>see id.</i> tbl. 6 (showing video decoder commands enabling trick mode functionality).</li> </ul> <p>“The video decoder contains a polyphase filter and a vertical interpolation filter for performing horizontal resampling and luma/chroma vertical interpolation to support decimation and scaling of pictures. In operation, the firmware first loads picture data from the video storage space in the SDRAM to the internal buffer of the video decoder.” AV7110 Preview at 27; <i>see id.</i> (describing additional aspects).</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers I and II</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Outputs in both PCM and SPDIF formats</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information</li> <li>• Supports half-frequency modes</li> <li>• Supports playback of 16-bit PCM data (PCM bypass), audio elementary stream, and audio PES</li> <li>• Provides read/write accesses to audio input buffers read/write pointers</li> </ul> <p>The audio module receives MPEG compressed audio data from the TC, decodes it, and outputs audio samples in PCM format. APIs are provided for the ARM CPU to initialize/control the audio decoder via a control register and to read status information from the decoder's status register.</p> <p>Audio frame data and PTS information are stored in the SDRAM in packet form. The audio module decodes the packets to extract the PTS and audio data. The audio decoder uses this PTS value to perform playback synchronization (see Synchronization for more details). It is application software's responsibility to determine and</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>enable the PIO of the MPEG-1 compliant bit-stream in a MPEG-2 audio program which contains both the MPEG-1 compliant bit-stream and the MPEG-2 extension bit-stream.</p> <p>The ARM can control the operation of the audio module via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and over-sampling ratio, and choose the output format for dual channel mode. The ARM will also be able to read status information from the audio module. One 32-bit register provides the MPEG header information and sync, CRC, and PCM status.” AV7110 Preview at 44; <i>see also id.</i> at 45-46 (listing registers used by the audio module).</p> <p>“MPEG transport decoder (TPP)  TPP module  features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15  Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32  Maximum number of pairs of keys for the descrambler ..... 16  Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination. The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“transport parser input interface</p> <p>The 'AV7110 accepts DVB transport packet data from a front end such as a Forward Error Correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB Conditional Access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23; <i>see also id.</i> at 24 tbl. 4 (describing transport packet input interface pin description).</p> <p>“The 'AV7110 uses the STC and PTS to determine the play back time of the decoded audio and video data. The relationship between STC and PTS is determined at the time of the generation of the generation of the respective elementary streams (ES). Upon reception, the demultiplexing software in the 'AV7110 extracts the video PTS and inserts it in an array of PTS and byte-count information maintained for the video decoder. For the audio the PTS information is extracted by the audio decoder front end from the PES. The video decoder contains an STC counter that is clocked by the system clock (27 MHz) and normalized to a 90 kHz reference. The</p>

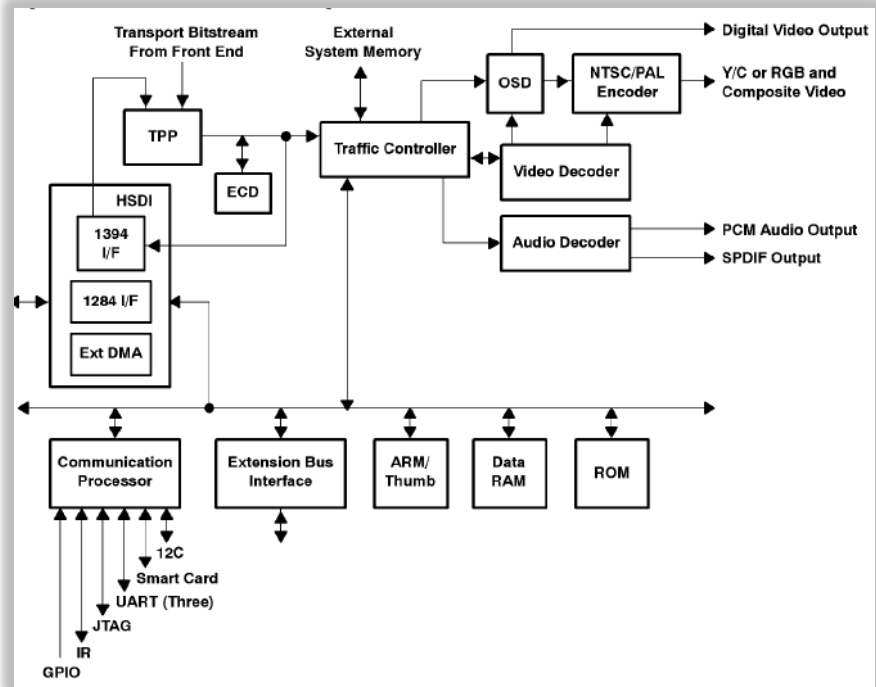
'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>audio decoder does not contain a counter. Instead, it gets updated from the system time reference counter every 1 .4 ms.” AV7110 Preview at 48.</p> <p>“elementary stream playback In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.” AV7110 Preview at 48.</p> <p>“extension bus interface (EBI) The extension bus interface is a 32-bit or 16-bit bidirectional data bus with a 25-bit address. It also provides 3 external interrupts and a wait line. All the external memories or I/O devices are mapped to the 32-bit address space of the ARM. There are six internally generated chips selects (CSx) for devices such as EEPROM memory, modem, front panel, front panel, front end control, parallel output port, and 1394 link device. Each CS has its own defined memory space and a programmable wait register which has a default of maximum allowable values as defined in Table 27. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. These are all programmable by user application software using APIs.” AV7110 Preview at 50.</p> <p>“CS1 is intended for ARM application code, but writes will not be prevented. CS2, CS3, CS4, and CS5 all have the same characteristics. The ARM performs reads and writes to these devices through the extension bus. CS6 is read and write accessible by the ARM. It is also accessed by the TC for TPP DMAs, and it is write only. User C application software selects the PIO of the packets to be sent through this port, the TPP will then send the data Q via DMAs. The parallel port is one byte wide and it is accessed via the least significant byte.” AV7110 Preview at 51.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure																																				
	<div><p>Table 27. An Example of Extension Bus Chip Select Assignment</p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 Mbytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2EFF FFFF</td><td>N/A</td><td>DRAM (up to 16 Mbytes, on RAS1)</td></tr><tr><td>N/A</td><td>2F00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 16 Mbytes, on RAS3)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7110 Preview at 51 tbl. 27.</p> <p>“The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it has to become active before the programmable wait cycle expires. If the combined total wait states exceeds its maximum, the decoder is not guaranteed to function properly. The EXTWAIT signal is synchronized internally with the on-chip 81 MHz clock. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT signal should be at least 24.7 ns. Since the EXTWAIT signal has the potential to stall the whole decoding process, the ARM will cap its wait to 500 ns. Afterwards, the ARM assumes the device that generated the EXTWAIT has failed and will ignore EXTWAIT from then on. Only a software or hardware reset can activate the EXTWAIT signal again. The timing diagram shown in Figure 19 is an example of a read using the EXTWAIT signal.”</p> <p>AV7110 Preview at 53.</p> <p>“The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 32-bit or 16-bit data and 25-bit address. It also supports DMA transfers to/from the extension bus. DMA transfers within the extension bus are not supported directly. They may be accomplished from user application software by using one DMA to the internal data RAM, followed by a second DMA to transfer back to the EBI. Extension bus single read and write cycle timings are shown in Figure 17 and Figure 18 respectively.” AV7110 Preview at 51; <i>see also id.</i> at 52 figs. 17 and 18.</p> <p>“traffic controller (TC)</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)	N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)	N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE																																		
CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)																																		
N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)																																		
N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)																																		
CS2	3000 0000 – 31FF FFFF	1 – 7	Modem																																		
CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel																																		
CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device																																		
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device																																		
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port																																		

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>features</p> <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>• Authorizes and manages DMA transfers</li> <li>• Provides SDRAM interface</li> <li>• Manages extension bus</li> <li>• Provides memory access protection</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> <li>- Audio/video decoder to/from SDRAM</li> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> </ul> </li> <li>• Generates chip selects (CS) for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus</li> <li>• Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.</li> </ul>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p>Figure 4. Traffic Controller Data Flow</p> </div> <p>AV7110 Preview at 18 fig. 4.</p> <p>See AV7110 Preview at 7 (stating that the TMS320AV7110 includes “an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory.”).</p> <p>“The ARM can control the operation of the audio module via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and over-sampling ratio, and choose the output format for dual channel mode. The ARM will also be able to read status information from the audio module. One 32-bit register provides the MPEG header information and sync, CRC, and PCM status.” AV7110 Preview at 44.</p> <p>See AV7110 Preview at 58 fig. 23 (showing examples of DRAM Connections to 16-Bit and 32-Bit Extension buses).</p>



'476 Patent Claim	Exemplary Prior Art Disclosure
<p>[1d] a media switch communicatively connected to the decoder subsystem, the media switch operative to interface a plurality of system components and operates asynchronously from the processor, wherein the media switch includes:</p>	<p>AV7110 Preview discloses or at least renders obvious a media switch communicatively connected to the decoder subsystem, the media switch operative to interface a plurality of system components and operates asynchronously from the processor. For example:</p>  <p>The diagram illustrates the system architecture of the AV7110 Preview. A central <b>Traffic Controller</b> is connected to several key components:</p> <ul style="list-style-type: none"> <li><b>Input/Output and Processing Blocks:</b> <ul style="list-style-type: none"> <li><b>TPP</b> (Transport Processing Processor) receives a <b>Transport Bitstream From Front End</b> and connects to the Traffic Controller.</li> <li><b>ECD</b> (Error Correction Decoder) connects to the Traffic Controller.</li> <li><b>Video Decoder</b> and <b>Audio Decoder</b> receive data from the Traffic Controller. The Video Decoder outputs to an <b>OSD</b> (On-Screen Display) and an <b>NTSC/PAL Encoder</b>, which produces <b>Digital Video Output</b> and <b>Y/C or RGB and Composite Video</b>.</li> <li>The Audio Decoder produces <b>PCM Audio Output</b> and <b>SPDIF Output</b>.</li> </ul> </li> <li><b>System Components:</b> <ul style="list-style-type: none"> <li><b>External System Memory</b> is connected to the Traffic Controller.</li> <li><b>Communication Processor</b> is connected to the Traffic Controller and interfaces with <b>GPIO</b>, <b>IR</b>, <b>JTAG</b>, <b>UART (Three)</b>, <b>Smart Card</b>, and <b>12C</b>.</li> <li><b>Extension Bus Interface</b> connects the Traffic Controller to <b>ARM/Thumb</b>, <b>Data RAM</b>, and <b>ROM</b>.</li> <li>A block containing <b>HSDI</b>, <b>1394 I/F</b>, <b>1284 I/F</b>, and <b>Ext DMA</b> is connected to the Traffic Controller.</li> </ul> </li> </ul> <p>AV7110 Preview at 12 fig. 1.</p> <p>“traffic controller (TC) features</p> <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> </ul>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Authorizes and manages DMA transfers</li> <li>• Provides SDRAM interface</li> <li>• Manages extension bus</li> <li>• Provides memory access protection</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> <li>- Audio/video decoder to/from SDRAM</li> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> </ul> </li> <li>• Generates chip selects (CS) for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus</li> <li>• Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.</li> </ul>

## '476 Patent Claim

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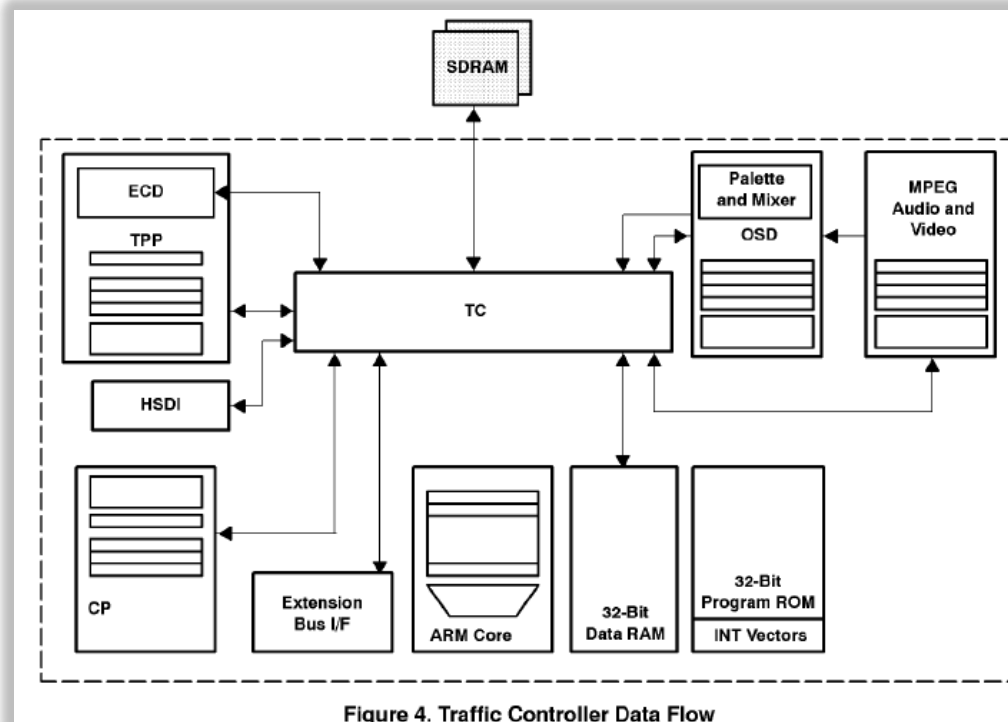


Figure 4. Traffic Controller Data Flow

AV7110 Preview at 18 fig. 4.

“extension bus interface (EBI)

The extension bus interface is a 32-bit or 16-bit bidirectional data bus with a 25-bit address. It also provides 3 external interrupts and a wait line. All the external memories or I/O devices are mapped to the 32-bit address space of the ARM. There are six internally generated chips selects (CSx) for devices such as EEPROM memory, modem, front panel, front panel, front end control, parallel output port, and 1394 link device. Each CS has its own defined memory space and a programmable wait register which has a default of maximum allowable values as defined in Table 27. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. These are all programmable by user application software using APIs.” AV7110 Preview at 50.

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	<p>“CS1 is intended for ARM application code, but writes will not be prevented. CS2, CS3, CS4, and CS5 all have the same characteristics. The ARM performs reads and writes to these devices through the extension bus. CS6 is read and write accessible by the ARM. It is also accessed by the TC for TPP DMAs, and it is write only. User C application software selects the PIO of the packets to be sent through this port, the TPP will then send the data Q via DMAs. The parallel port is one byte wide and it is accessed via the least significant byte.” AV7110 Preview at 51.</p> <div><p><b>Table 27. An Example of Extension Bus Chip Select Assignment</b></p><table><tr><th>CHIP SELECT</th><th>BYTE ADDRESS RANGE</th><th>WAIT STATE</th><th>DEVICE</th></tr><tr><td>CS1</td><td>2C00 0000 – 2DFF FFFF</td><td>1 – 5</td><td>EEPROM (up to 32 Mbytes)</td></tr><tr><td>N/A</td><td>2E00 0000 – 2EFF FFFF</td><td>N/A</td><td>DRAM (up to 16 Mbytes, on RAS1)</td></tr><tr><td>N/A</td><td>2F00 0000 – 2FFF FFFF</td><td>N/A</td><td>DRAM (up to 16 Mbytes, on RAS3)</td></tr><tr><td>CS2</td><td>3000 0000 – 31FF FFFF</td><td>1 – 7</td><td>Modem</td></tr><tr><td>CS3</td><td>3200 0000 – 33FF FFFF</td><td>1 – 7</td><td>Front panel</td></tr><tr><td>CS4</td><td>3400 0000 – 35FF FFFF</td><td>1 – 7</td><td>Front end device</td></tr><tr><td>CS5</td><td>3600 0000 – 37FF FFFF</td><td>1 – 7</td><td>1394 Link device</td></tr><tr><td>CS6</td><td>3800 0000 – 39FF FFFF</td><td>1 – 4</td><td>Parallel data port</td></tr></table></div> <p>AV7110 Preview at 51 tbl. 27.</p> <p>“The EXTWAIT signal is an alternative way for the ARM to communicate with slower devices. It can be used together with the programmable wait state, but it has to become active before the programmable wait cycle expires. If the combined total wait states exceeds its maximum, the decoder is not guaranteed to function properly. The EXTWAIT signal is synchronized internally with the on-chip 81 MHz clock. When a device needs to use the EXTWAIT signal, it should set the programmable wait state to at least 3. The duration of EXTWAIT signal should be at least 24.7 ns. Since the EXTWAIT signal has the potential to stall the whole decoding process, the ARM will cap its wait to 500 ns. Afterwards, the ARM assumes the device that generated the EXTWAIT has failed and will ignore EXTWAIT from then on. Only a software or hardware reset can activate the EXTWAIT signal again. The timing diagram shown in Figure 19 is an example of a read using the EXTWAIT signal.” AV7110 Preview at 53.</p>	CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE	CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)	N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)	N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)	CS2	3000 0000 – 31FF FFFF	1 – 7	Modem	CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel	CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device	CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device	CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port
CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE																																		
CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)																																		
N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)																																		
N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)																																		
CS2	3000 0000 – 31FF FFFF	1 – 7	Modem																																		
CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel																																		
CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device																																		
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device																																		
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port																																		

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 32-bit or 16-bit data and 25-bit address. It also supports DMA transfers to/from the extension bus. DMA transfers within the extension bus are not supported directly. They may be accomplished from user application software by using one DMA to the internal data RAM, followed by a second DMA to transfer back to the EBI. Extension bus single read and write cycle timings are shown in Figure 17 and Figure 18 respectively.” AV7110 Preview at 51; <i>see also id.</i> at 52 figs. 17 and 18.</p> <p>“The descrambling of the incoming data is performed automatically with minimum intervention by the CPU. The TPP module detects which transport packets are scrambled, at either the program elementary stream (PES) or the transport stream level, and routes the data through the ECD as necessary. The ECD stores the descrambler keys locally and automatically selects the correct key of a specific PID. Up to 16 sets of keys are stored in the key table for use by the ECD. It is possible for more than one PIO to use the same key. The descrambler keys are derived by the conditional access software using the command packet from the bit-stream.” AV7110 Preview at 23.</p> <p>“The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.</p> <p>Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM, and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.” AV7110 Preview at 13.</p> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start</p>

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	<p>up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.” AV7110 Preview at 22.</p> <p>Together with the ARM, the TPP also handles program clock reference (PCR) recovery with an external VCXO. The TPP will latch and transfer to the ARM its internal system clock upon the arrival of any packet which contains a PCR. After further processing on the packet and identifying the system clock, the ARM calculates the difference between the system clock from a bit-stream and the actual system clock at the time the packet arrives. Then, the ARM filters the difference and sends it through an 8-bit sigma-delta DAC to control the external VCXO. The ARM will drive the VCXO to its center frequency during start-up or, if enabled by an API, after channel change when there is no incoming PCR.” AV7110 Preview at 13.</p> <p>“At startup the hardware STC counter is free running and the increments to the software extension of the system STC take place every 1 .4 ms. Both audio and video decoders are initialized to free-run. This condition is identical for system startup as well as for re-synchronization after a channel change. Once a PCR channel is activated by user software through an API, the on-chip software will monitor the incoming data in the PCR designated channel and reset the system common reference counter STCs<sub>sys</sub> to the first PCR that arrives in the designated stream (full 42 bits). At the same time, the video and audio STC are initialized to the same value, if they are enabled via the appropriate API calls.” AV7110 Preview at 48.</p> <p>“Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PC Rs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“The video synchronization of STC and PTS can be enabled/disabled via an API. The STC for the video decoder</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>is clocked by the 27 MHz system clock. The initial value of the video STC (STCvid) is written to the video decoder from the firmware. This happens at the time that the first PCR from the designated PCR channel arrives at the AF. In some cases the PTS can consistently be off by a certain amount, causing the video buffer to eventually over- or under-run. If this occurs, the firmware will detect the under/over-runs via FIQ-s and adjust the video STC with an offset, such that the under/over-run ceases.” AV7110 Preview at 50.</p> <p>“Command communication from the 'AV7110 to the ESC is done using the 4-bit EDMA A bus which is mapped into the ARM addressing space of the 'AV7110 when the EDMA port is selected. This will allow user software to write directly to the registers of the ESC. For details of these registers, refer to the appropriate external controller documentation. The 'AV7110 does not process this data and thus places no restriction on its function. An access to this memory space while the EDMA is selected will automatically generate a read or write cycle on the HSDI using the EDMA_RO and EDMA_WR signals and the EDMA_CS signal. Timing for these accesses is shown in Figure 31.” AV7110 Preview at 67.</p> <p>“communication processor features</p> <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> <li>• Provides 3 general purpose UARTs - two at up to 115.2 Kbps and one at up to 9.6 Kbps</li> <li>• Accepts IR input signals</li> <li>• Generates IR output signals</li> <li>• Provides up to nine general purpose I/Os</li> <li>• Manages I2C and JTAG interfaces</li> </ul> <p>This module contains a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR, and I2C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM CPU. Interrupts are used to communicate between these interface modules and the ARM CPU.” AV7110 Preview at 72; <i>see generally id.</i> at 72-78 (describing different functions and functional blocks of the communication processor).</p> <p>“Together with the ARM, the TPP also handles program clock reference (PCR) recovery with an external VCXO. The TPP will latch and transfer to the ARM its internal system clock upon the arrival of any packet which contains a PCR. After further processing on the packet and identifying the system clock, the ARM calculates the difference between the system clock from a bit-stream and the actual system clock at the time the packet arrives. Then, the ARM filters the difference and sends it through an 8-bit sigma-delta DAC to control the external</p>

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	<p>VCXO. The ARM will drive the VCXO to its center frequency during start-up or, if enabled by an API, after channel change when there is no incoming PCR.” AV7110 Preview at 13; <i>see also id.</i> at 22-23.</p> <p>“The 'AV7110 uses the STC and PTS to determine the play back time of the decoded audio and video data. The relationship between STC and PTS is determined at the time of the generation of the generation of the respective elementary streams (ES). Upon reception, the demultiplexing software in the 'AV7110 extracts the video PTS and inserts it in an array of PTS and byte-count information maintained for the video decoder. For the audio the PTS information is extracted by the audio decoder front end from the PES. The video decoder contains an STC counter that is clocked by the system clock (27 MHz) and normalized to a 90 kHz reference. The audio decoder does not contain a counter. Instead, it gets updated from the system time reference counter every 1 .4 ms.” AV7110 Preview at 48.</p> <p>“The audio synchronization of STC and PTS can be enabled/disabled through an API. The STC for the audio decoder time reference is loaded by the firmware every time the system reference counter (STCs<sub>sys</sub>) rolls over. This roll over will occur every 26 ticks of the 90 kHz portion of the hardware system clock counter in the AV7110. This is approximately every 1 .4 ms. The firmware will receive an FIQ from the counter and write STCs<sub>sys</sub> + aud_offset to the STC register in the audio decoder. The value for aud_offset is 0 by default after initialization and after audio channel change.” AV7110 Preview at 49.</p> <p>“IEEE 1394 interface On power-up the IEEE 1394 interface is enabled on the HSDI. An API call can be used to configure the HSDI for another mode or to return to the 1394 interface if necessary. To complete the 1394 implementation, the 'AV7110 requires an external packetizer and link layer controller, and a physical layer device. Figure 26 shows the connection between the 'AV7110 and these devices.” AV7110 Preview at 62; <i>see id.</i> at fig. 26.</p> <p>“IEEE 1284 interface The IEEE 1284 interface on the 'AV7110 has the following characteristics:</p> <ul style="list-style-type: none"> <li>• Supports transfer of up to 10 Mbits/sec</li> <li>• Supports the compatibility, nibble and byte mode</li> <li>• Supports the ECP mode except for run length coding compression</li> <li>• Does not support the EPP mode</li> <li>• Peripheral mode only</li> </ul> <p>The IEEE 1284 interface is used to connect the 'AV7110 to an external host. The 'AV7110 side of the protocol</p>



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	<p>can be handled by an IEEE 1284 peripheral interface controller on the chip such as the SN54ACT1284/SN? 4ACT1284. Since the signals on the HSDI are 5-V-tolerant, they can be connected directly to this external 1284 driver.” AV7110 Preview at 69; <i>see id.</i> fig.33; <i>see also id.</i> at 69-70.</p> <p>“high speed data interface (HSDI)  The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device. Logic for these three interfaces share signal pins and hence only one can be active at any given time. Table 28 shows the pin definitions for the HSDI in its various configurations. Switching from one interface to another will require a predefined sequence of API calls. Two signal pins (HSDI_ STATUS[1 :OJ) indicate which of the three interfaces is active. They can be used to control external logic for interface arbitration. The definition of these signals is shown at the bottom of Table 28.” AV7110 Preview at 60.</p> <p>“The 32-bit ARM processor running at 40.5 MHz and its associated firmware provide the following:</p> <ul style="list-style-type: none"> <li>• Initialization and management of all hardware modules</li> <li>• Service for selected interrupt generated by hardware modules and I/O ports</li> <li>• Application program interface (API) for users to develop their own applications” AV7110 Preview at 15.</li> </ul> <p>“The CPU in the 'AV7110 is a 32-bit RISC processor, the ARM7TDM I/Thumb, which has the capability to execute instructions in 16- or 32-bit format at a clock frequency of 40.5 MHz. The regular ARM instructions are exactly one word (32-bit) long, and the data operations are only performed on word quantities. The LOAD and STORE instructions however, can transfer either byte, half-word or word quantities.  The Thumb uses the same 32-bit architecture with an 16-bit instruction set. That is, it retains the 32-bit performance but reduces the code size with 16-bit instructions. With 16-bit instruction, the Thumb still gives 70-80% of the performance of the ARM when running ARM instructions from 32-bit memory.” AV7110 Preview at 15; <i>see also id.</i> (stating that ARM and Thumb are used interchangeably in the AV7110 Preview’s disclosure).</p> <p>“The 'AV7110 includes three general purpose UARTs that are memory mapped and fully accessible by user application programs. A set of APIs exists to assist in programming them. The output of the UARTs are digital and require external level shifters for RS232 compliance. These UARTs support full duplex mode and are double buffered with sufficient FIFO space to minimize the interrupt frequency to the ARM even when they are operating at their maximum transmission speeds.” AV7110 Preview at 75.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“IR input port Hardware is provided to capture and deliver IR data bits to user software for command decoding. Sample IR command decoding driver software for several commonly used IR formats are provided with the 'AV7110. API software is provided to configure the hardware to recognize IR format with different parameter settings:</p> <ul style="list-style-type: none"> <li>• data frame length (up to 32 bits)</li> <li>• maximum time between frame (a 13-bit count equals one period of CLK40)</li> <li>• LSB/MSB first</li> <li>• repeat pattern present</li> <li>• stop pattern present</li> <li>• compare enable (ignore repeated frames if this bit is set)</li> </ul> <p>At start up, user application software sets up the parameters above and defines the encoding pattern of the preamble, stop, repeat, data zero, and data one by storing the duration of the high and low levels of each pattern in the IR-input-RAM. The IR hardware will then look for IR input (assumed demodulated) which matches the pattern” AV7110 Preview at 75.</p> <p>“general purpose I/Os The 'AV7110 has four dedicated (101, 102, 104, and 105) and five multiplexed general purpose I/O pins (103 and 106 to 109) which are user configurable. Each I/O port has its own 32-bit control/status register, IOCSR<sub>n</sub>, where n ranges from 1 to 9.</p> <p>If an I/O is configured as an input and the delta interrupt mask is cleared, an IRQ is generated whenever an input changes state. If the delta interrupt mask is set, interrupts to the ARM are disabled. If no other device drives the I/O pin while it is configured as an input, it will be held high by an internal pullup resistor.</p> <p>If an I/O is configured as an output (by setting the cio bit in the corresponding control/status register), the value contained in the io_out) bit of the control/status register is output. Interrupt generation is disabled when an I/O is configured as an output.” AV7110 Preview at 77; <i>see also id.</i> tbl. 37.</p> <p>“Hardware is provided on the 'AV7110 to generate drive signal on the output pin according to input data bit and format control signals provided by user software or to just retransmit the input signal received at the IR input port. External buffering is required to drive an IR LED.</p> <p>In order to communicate with IR receivers of different IR formats, the 'AV7110s IR output encoder supports a very flexible IR frame format. The format of the frame is specified through APIs and can be changed as frequently as per IR command transmission.” AV7110 Preview at 75.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“The smart card interface on the 'AV7110 supports clock frequencies of: 2.025, 3.375, 4.05, 4.5, 6.0, 6.75, 8.1, and 13.5 MHz. All these clock frequencies are generated internally from the 81 MHz clock.” AV7110 Preview at 72.</p> <p>“Since there is only an 8-bit bus on the HSDI, the ESC is limited to an 8-bit, single bus architecture so its mode selection inputs should be set to mode 0. The upper data bits can be left floating since they have internal pullups on the ESC. Likewise, the AD-0 inputs of the ESC will not be used for this mode and can be left unconnected. The ESC requires an external clock source from 10 MHz to 40 MHz. Since the CLK40 signal of the 'AV7110 is actually a 40.5 MHz clock it cannot be used directly for this controller without violating its specification. Table 2 shows the signals needed for the EDMA interface.” AV7110 Preview at 66; <i>see id.</i> tbl. 32 (listing DMA interface signals).</p> <p><i>See</i> AV7110 Preview at 58 fig. 23 (showing examples of DRAM Connections to 16-Bit and 32-Bit Extension buses).</p> <p><i>See</i> AV7110 Preview at 60, table 29 (“Types of DMA Transfers Allowed for Data Ports”).</p> <p><i>See</i> claim 1 at 1e-1h, <i>infra</i>.</p>
[1e] a host controller;	<p>AV7110 Preview discloses or at least renders obvious a host controller. For example:</p> <p>“high speed data interface (HSDI)  The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device. Logic for these three interfaces share signal pins and hence only one can be active at any given time. Table 28 shows the pin definitions for the HSDI in its various configurations. Switching from one interface to another will require a predefined sequence of API calls. Two signal pins (HSDI_ STATUS[1:0]) indicate which of the three interfaces is active. They can be used to control external logic for interface arbitration. The definition of these signals is shown at the bottom of Table 28.” AV7110 Preview at 60.</p>

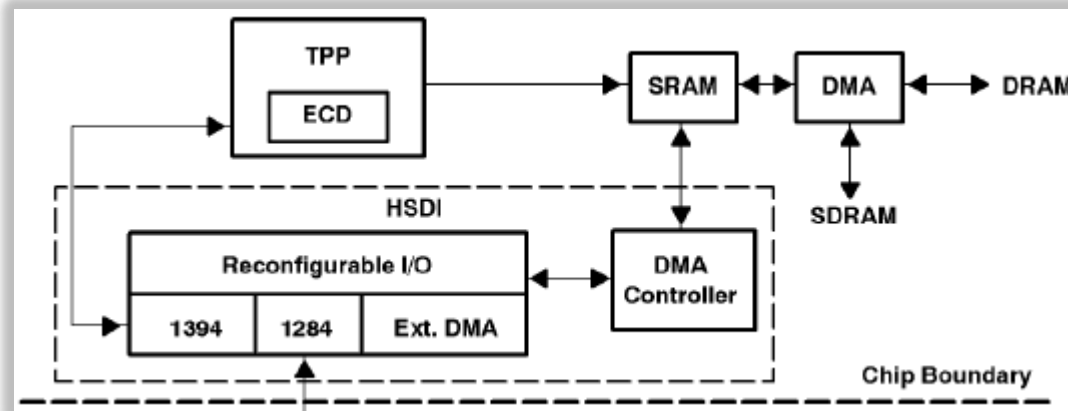
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Table 28. High Speed Data Interface Signal Pin Assignment

PIN NAME	I/O	IEEE 1394 I/F	IEEE 1284 I/F	EXTERNAL DMA
HSDI_DATA[7:0]	I/O	BDI[7:0] (In/Out)	1284_D[7:0] (In/Out)	EDMA_DB[7:0] (In/Out)
HSDI_SIG1	O	BDIRW (Out)	1284_ERROR (Out)	EDMA_RD (Out)
HSDI_SIG2	O	BDIEN (Out)	1284_ACK (Out)	EDMA_DACK (Out) <sup>†</sup>
HSDI_SIG3	I or O	BDAVAIL (In)	1284_STROBE (In)	EDMA_A[3] (Out)
HSDI_SIG4	I/O, I or O	BDIF[2] (In/Out)	1284_SLCTIN (In)	EDMA_A[2] (Out)
HSDI_SIG5	I/O, I or O	BDIF[1] (In/Out)	1284_AF (In)	EDMA_A[1] (Out)
HSDI_SIG6	I/O or O	BDIF[0] (In/Out)	1284_SLT (Out)	EDMA_A[0] (Out)
HSDI_SIG7	I	BDIRQ (In)	1284_INIT (In)	EDMA_DREQ (In) <sup>†</sup>
HSDI_SIG8	O	N/A (drives high)	1284_PEND (Out)	EDMA_CS (Out)
HSDI_SIG9	O	N/A (drives high)	1284_BUSY (Out)	EDMA_WR (Out)
HSDI_STATUS[1:0]	O	00	1x (see IEEE 1284 Interface)	01

AV7110 Preview at 60 tbl. 28; *see also id.* tbl. 29 (listing different types of DMA transfers allowed for data ports).



AV7110 Preview at 61 fig. 25 (showing functional block diagram of HSDI).

“IEEE 1394 interface

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	<p>On power-up the IEEE 1394 interface is enabled on the HSDI. An API call can be used to configure the HSDI for another mode or to return to the 1394 interface if necessary. To complete the 1394 implementation, the 'AV7110 requires an external packetizer and link layer controller, and a physical layer device. Figure 26 shows the connection between the 'AV7110 and these devices.” AV7110 Preview at 62; see id. at fig. 26.</p> <p>“IEEE 1284 interface  The IEEE 1284 interface on the 'AV7110 has the following characteristics:</p> <ul style="list-style-type: none"> <li>• Supports transfer of up to 10 Mbits/sec</li> <li>• Supports the compatibility, nibble and byte mode</li> <li>• Supports the ECP mode except for run length coding compression</li> <li>• Does not support the EPP mode</li> <li>• Peripheral mode only</li> </ul> <p>The IEEE 1284 interface is used to connect the 'AV7110 to an external host. The 'AV7110 side of the protocol can be handled by an IEEE 1284 peripheral interface controller on the chip such as the SN54ACT1284/SN? 4ACT1284. Since the signals on the HSDI are 5-V-tolerant, they can be connected directly to this external 1284 driver.” AV7110 Preview at 69; see id. fig.33; see also id. at 69-70.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p style="text-align: center;"><b>Figure 26. 1394 Interface</b></p> </div> <p>AV7110 Preview at 62; <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) C packets to and from the internal data RAM. This data can then be processed by the user software as needed.”); <i>see also id.</i> at 63 (listing signals associated with the 1394 interface).</p> <p>“external DMA interface (EDMA) When configured for EDMA operation (HSDI_STATUS[1 LO] = 01), the HSDI is capable of a glue less connection to an external enhanced SCSI controller (ESC) device such as the NCR 53CF94-1 /53CF96-1. Figure 30 shows the connections for this example configuration.” AV7110 Preview at 66.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<div><p>Figure 30. Interfacing the 'AV7110 to a SCSI Chip</p></div> <p>AV7110 Preview at 66 fig. 30.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<div> </div> <p>AV7110 Preview at 71 fig. 34; <i>see id.</i> (“In this example, the logic is grouped into a single programmable logic device, For simplicity, some of the HSDI signal names have been shorted (i.e., ST1 and ST0 to represent HSDI_STATUS[1 :0], etc.). Note that the 1284 interface block is completely disabled (tri-stated) when it is not selected and so can be directly connected to the HSDI bus.”).</p> <p><i>See</i> AV7110 Preview at 1 (stating that the AV7110 includes a “[c]onfigurabe High Speed Data Interface to Connect to Either an IEEE 1394 Link Device, an IEEE 1284 Interface, or an External DMA Device Like SCSI that Supports Up to 16 Mbps Data Rate “).</p>



'476 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p>The diagram illustrates the AV7110 HSDI interface. At the top, a block labeled 'AV7110 HSDI' has several output lines: 1284_BUSY, 1284_PEND, 1284_D[7:0], 1284_SLT, 1284_ACK, 1284_ERROR, 1284_STROBE, 1284_SLCTIN, 1284_AF, 1284_INIT, HSDI_STATUS[1], and HSDI_STATUS[0]. Below this, two identical blocks labeled '74ACT1284' are shown, each with inputs A, B, HD, and DIR. The first 74ACT1284 block is connected to the AV7110 HSDI block via 1284_BUSY, 1284_PEND, and 1284_D[7:0]. The second 74ACT1284 block is connected to the AV7110 HSDI block via 1284_SLT, 1284_ACK, 1284_ERROR, 1284_STROBE, 1284_SLCTIN, 1284_AF, 1284_INIT, HSDI_STATUS[1], and HSDI_STATUS[0]. Both 74ACT1284 blocks are connected to an 'IEEE 1284 Bus Connector' at the bottom. The connector has multiple input/output lines for each block. A third block, containing a triangle symbol, is also connected to the IEEE 1284 Bus Connector and the AV7110 HSDI block via 1284_STROBE, 1284_SLCTIN, 1284_AF, and 1284_INIT.</p> </div> <p>AV7110 Preview at 69; <i>see also id.</i> at 70 tbl. 34 (listing signals associated with IEEE 1284 interface).</p> <p>“The application software interfaces with the peripheral interface controller via RTSL API calls. To send data to the host the application software will issue an API call to transfer the data from memory to the peripheral interface via a DMA. To receive data from the host, the application software will issue an API to transfer a predetermined number of bytes from the peripheral interface to internal data memory via the HSDI DMA unit. The user application software must have a way to determine the number of bytes of data that is expected from the host.” AV7110 Preview at 70.</p> <p>“combining the 1394, 1284 and external controller interfaces With additional external logic it is possible to combine the three HSDI interfaces within a single design. Note that performing the API call to switch between interfaces will involve resetting the HSDI and so transfers between interfaces are not practical (i.e., 1394 to 1284). Switching between HSDI modes should be detected by external logic and proper care should be taken to prevent contention between the external devices and the HSDI interface.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>Figure 34 shows the block diagram of an example of this configuration based on the devices used previously.” AV7110 Preview at 70.</p>
<p>[1f] a DMA controller;</p>	<p>AV7110 Preview discloses or at least renders obvious a DMA controller. For example:</p> <p>“The data transfer from TPP to the data RAM is done via DMA. Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM, and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.” AV7110 Preview at 13.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PIO table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.</p> <p>The only difference between the two scenarios is that in the case where there is no TPP traffic, the TPP buffer pool can be used. In the case where there is active TPP data, a general purpose buffer needs to be used.</p>

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	<p>Additionally, when TPP data traffic is active, the end of packet (EOP) interrupt generation will require an indication data type configured in the header, which describes where the data to be processed is to be found.” AV7110 Preview at 21.</p> <p>“managing DMA transfer</p> <p>The TC in the 'AV7110 provides DMA capability to facilitate large block transfers between memories and buffers. The burst length (in multiple of 4 bytes) of the DMAs are independently selectable via 6-bit registers with an API. This provides a burst value from 4 to 188 bytes.</p> <p>The SDRAM is used to store system level tables, video and audio bit-streams, reconstructed video images, OSD data, video decoding codes, tables, and FIFOs. The internal data RAM stores temporary buffers, OSD window attributes, keys for conditional access, and other tables and buffers for firmware.</p> <p>The TC manages two types of DMA transfers, but only one of them, the general purpose DMA (GPDMA), is accessible to the user. The user has no knowledge of the other type of DMAs which are initiated by the TPP, the video decoder, the audio decoder, and the OSD module. The GPDMA includes ARM-generated and bitBLT-generated DMAs. The TC can accept up to 4 GPDMA at any given time. DMA from the data RAM to the extension bus (and vice versa) is byte aligned. Table 3 describes the allowable GPDMA transfers.</p> <p>....</p> <p>Note that there is no direct DMA transfer between the extension bus memories and the SDRAM. the user can use the bitBLT hardware which uses the internal data RAM as an intermediate step for this process. Alternatively, an API is provided to transfer data from the extension bus memories to the SDRAM (and vice versa). This is accomplished using this internal data RAM and two DMAs. One from the extension bus to the internal data RAM and the second from the internal data RAM to the SDRAM.” AV7110 Preview at 20; <i>see also id.</i> tbl. 3 (showing allowed DMA transfers between different functional blocks).</p> <p>“The extension bus supports connection to external EEPROM, SRAM, or ROM memory and DRAM with its 32-bit or 16-bit data and 25-bit address. It also supports DMA transfers to/from the extension bus. DMA transfers within the extension bus are not supported directly. They may be accomplished from user application software by using one DMA to the internal data RAM, followed by a second DMA to transfer back to the EBI. Extension bus single read and write cycle timings are shown in Figure 17 and Figure 18 respectively.” AV7110 Preview at 51; <i>see also id.</i> at 52 figs. 17 and 18.</p> <p>“An internal DMA unit is dedicated for the HSDI port and is under user level API control. There are some restrictions to the source, destinations and data types of this DMA unit. These are detailed in Table 29. The</p>

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	<p>firmware available in the first samples will not support I/A packets, multiple I packet channels or the Program Map Table insertion for IEEE 1394. In any event, a DMA write from the TPP to the HSDI in any of its configurations, only sends the payload. It is impossible to view and perform a DMA transfer to the HSDI from the same program source..” AV7110 Preview at 60.</p> <div><p><b>Table 29. Types of DMA Transfers Allowed for Data Ports</b></p><table><tr><th>INTERFACE CONFIGURATION</th><th>SOURCE DATA TYPES</th><th>POSSIBLE DESTINATION FOR DMA INPUT</th><th>POSSIBLE SOURCES FOR DMA OUTPUT</th></tr><tr><td>IEEE 1394/TPP (Dedicated I/F<sup>†</sup>)</td><td>M Packets</td><td>TPP</td><td>TPP</td></tr><tr><td>IEEE 1394 I/F</td><td>M Packets<sup>‡</sup></td><td>DRAM or SDRAM<sup>§</sup></td><td>TPP, DRAM or SDRAM</td></tr><tr><td>IEEE 1284 I/F</td><td>Elementary Stream or Data<sup>‡</sup></td><td>DRAM or SDRAM</td><td>TPP, DRAM or SDRAM</td></tr><tr><td>External DMA</td><td>Elementary Stream or Data<sup>‡</sup></td><td>DRAM or SDRAM</td><td>TPP, DRAM or SDRAM</td></tr></table><p><sup>†</sup> This is a dedicated data path which is separate from the DMA channel. <sup>‡</sup> Other data types or support like I/A packets, MPEG1 system and MPEG2 program require versions of the firmware which will not be available in the first samples. <sup>§</sup> The source or destination between DRAM and SDRAM is a two-stage process using the on chip SRAM as an intermediate step.</p></div> <p>AV7110 Preview at 60 fig. 29.</p> <p>“external DMA Interface (EDMA)</p> <p>When configured for EDMA operation (HSDI_ STATUS[1 LO] = 01), the HSDI is capable of a glue less connection to an external enhanced SCSI controller (ESC) device such as the NCR 53CF94-1 /53CF96-1. Figure 30 shows the connections for this example configuration.” AV7110 Preview at 66.</p> <p>“Command communication from the 'AV7110 to the ESC is done using the 4-bit EDMA A bus which is mapped into the ARM addressing space of the 'AV7110 when the EDMA port is selected. This will allow user software to write directly tot he registers of the ESC. For details of these registers, refer to the appropriate external controller documentation. The 'AV7110 does not processing of this data and thus places no restriction on its function. An access to this memory space while the EDMA is selected will automatically generate a read or write cycle on the HSDI using the EDMA_RO and EDMA_WR signals and the EDMA_CS signal. Timing for these access is shown in Figure 31.” AV7110 Preview at 67.</p> <p>“The EDMA DREQ signal should be used by the external controller to initiate an external DMA ('AV7110 DMA between the HSDI and the external device). EDMA_DREQ will be ignored until the DMA has been properly</p>	INTERFACE CONFIGURATION	SOURCE DATA TYPES	POSSIBLE DESTINATION FOR DMA INPUT	POSSIBLE SOURCES FOR DMA OUTPUT	IEEE 1394/TPP (Dedicated I/F <sup>†</sup> )	M Packets	TPP	TPP	IEEE 1394 I/F	M Packets <sup>‡</sup>	DRAM or SDRAM <sup>§</sup>	TPP, DRAM or SDRAM	IEEE 1284 I/F	Elementary Stream or Data <sup>‡</sup>	DRAM or SDRAM	TPP, DRAM or SDRAM	External DMA	Elementary Stream or Data <sup>‡</sup>	DRAM or SDRAM	TPP, DRAM or SDRAM
INTERFACE CONFIGURATION	SOURCE DATA TYPES	POSSIBLE DESTINATION FOR DMA INPUT	POSSIBLE SOURCES FOR DMA OUTPUT																		
IEEE 1394/TPP (Dedicated I/F <sup>†</sup> )	M Packets	TPP	TPP																		
IEEE 1394 I/F	M Packets <sup>‡</sup>	DRAM or SDRAM <sup>§</sup>	TPP, DRAM or SDRAM																		
IEEE 1284 I/F	Elementary Stream or Data <sup>‡</sup>	DRAM or SDRAM	TPP, DRAM or SDRAM																		
External DMA	Elementary Stream or Data <sup>‡</sup>	DRAM or SDRAM	TPP, DRAM or SDRAM																		

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>configured using the appropriate API calls. The source/destination addresses, the DMA size and the burst are under user software control via this API. Once asserted, the 'AV7110 will respond by transferring the data one byte at a time between the external device and the internal data RAM using the EDMA_RD and EDMA_WR signals and the EDMA_DACK signal as shown in Figure 32.” AV7110 Preview at 67.</p> <p>“When the 'AV7110 is transferring data to/from the DRAM via DMA, it makes full use of the page mode read/write cycle and will read/write a byte/half-word/word every 50 ns (2 clock cycles). When 16-bit wide DRAM is accessed from the ARM, the DRAM controller will make use of page mode read cycle to transfer each 32 bit word. Each new 32-bit write/read is addressed independently to the DRAM.” AV7110 Preview at 57.</p> <p>“The HSDI supports the following concurrent data transfers.</p> <ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/program to 1394 (using dedicated I/F - see NOTE XXXX of Table 29)</li> <li>• TPP/program to decoder; 1394/DMA to/from memory</li> <li>• TPP/program to decoder; memory/DMA to/from HSDI</li> <li>• TPP/program to decoder; TPP/DMA to HSDI</li> <li>• TPP/program to decoder; TPP/program to 1394; memory/DMA to/from 1394</li> <li>• TPP/program to decoder; 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; TPP/DMA to 1394” AV7110 Preview at 61.</li> </ul> <div> </div> <p>AV7110 Preview at 61 fig. 25 (showing the functional blocks of the HSDI); <i>see also id.</i> at 62-65 (showing describing AV7110’s reading and writing of data from/to the 1394 interface).</p>

'476 Patent Claim	Exemplary Prior Art Disclosure																																																												
	<p>“high speed data interface (HSDI) The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device. Logic for these three interfaces share signal pins and hence only one can be active at any given time. Table 28 shows the pin definitions for the HSDI in its various configurations. Switching from one interface to another will require a predefined sequence of API calls. Two signal pins (HSDI_ STATUS[1:0]) indicate which of the three interfaces is active. They can be used to control external logic for interface arbitration. The definition of these signals is shown at the bottom of Table 28.” AV7110 Preview at 60.</p> <div><p><b>Table 28. High Speed Data Interface Signal Pin Assignment</b></p><table><tr><th>PIN NAME</th><th>I/O</th><th>IEEE 1394 I/F</th><th>IEEE 1284 I/F</th><th>EXTERNAL DMA</th></tr><tr><td>HSDI_DATA[7:0]</td><td>I/O</td><td>BDI[7:0] (In/Out)</td><td>1284_D[7:0] (In/Out)</td><td>EDMA_DB[7:0] (In/Out)</td></tr><tr><td>HSDI_SIG1</td><td>O</td><td>BDIRW (Out)</td><td>1284_ERROR (Out)</td><td>EDMA_RD (Out)</td></tr><tr><td>HSDI_SIG2</td><td>O</td><td>BDIEN (Out)</td><td>1284_ACK (Out)</td><td>EDMA_DACK (Out)<sup>†</sup></td></tr><tr><td>HSDI_SIG3</td><td>I or O</td><td>BDAVAIL (In)</td><td>1284_STROBE (In)</td><td>EDMA_A[3] (Out)</td></tr><tr><td>HSDI_SIG4</td><td>I/O, I or O</td><td>BDIF[2] (In/Out)</td><td>1284_SLCTIN (In)</td><td>EDMA_A[2] (Out)</td></tr><tr><td>HSDI_SIG5</td><td>I/O, I or O</td><td>BDIF[1] (In/Out)</td><td>1284_AF (In)</td><td>EDMA_A[1] (Out)</td></tr><tr><td>HSDI_SIG6</td><td>I/O or O</td><td>BDIF[0] (In/Out)</td><td>1284_SLT (Out)</td><td>EDMA_A[0] (Out)</td></tr><tr><td>HSDI_SIG7</td><td>I</td><td>BDIRQ (In)</td><td>1284_INIT (In)</td><td>EDMA_DREQ (In)<sup>†</sup></td></tr><tr><td>HSDI_SIG8</td><td>O</td><td>N/A (drives high)</td><td>1284_PEND (Out)</td><td>EDMA_CS (Out)</td></tr><tr><td>HSDI_SIG9</td><td>O</td><td>N/A (drives high)</td><td>1284_BUSY (Out)</td><td>EDMA_WR (Out)</td></tr><tr><td>HSDI_STATUS[1:0]</td><td>O</td><td>00</td><td>1x (see IEEE 1284 Interface)</td><td>01</td></tr></table></div> <p>AV7110 Preview at 60 tbl. 28; <i>see also id.</i> tbl. 29 (listing different types of DMA transfers allowed for data ports).</p>	PIN NAME	I/O	IEEE 1394 I/F	IEEE 1284 I/F	EXTERNAL DMA	HSDI_DATA[7:0]	I/O	BDI[7:0] (In/Out)	1284_D[7:0] (In/Out)	EDMA_DB[7:0] (In/Out)	HSDI_SIG1	O	BDIRW (Out)	1284_ERROR (Out)	EDMA_RD (Out)	HSDI_SIG2	O	BDIEN (Out)	1284_ACK (Out)	EDMA_DACK (Out) <sup>†</sup>	HSDI_SIG3	I or O	BDAVAIL (In)	1284_STROBE (In)	EDMA_A[3] (Out)	HSDI_SIG4	I/O, I or O	BDIF[2] (In/Out)	1284_SLCTIN (In)	EDMA_A[2] (Out)	HSDI_SIG5	I/O, I or O	BDIF[1] (In/Out)	1284_AF (In)	EDMA_A[1] (Out)	HSDI_SIG6	I/O or O	BDIF[0] (In/Out)	1284_SLT (Out)	EDMA_A[0] (Out)	HSDI_SIG7	I	BDIRQ (In)	1284_INIT (In)	EDMA_DREQ (In) <sup>†</sup>	HSDI_SIG8	O	N/A (drives high)	1284_PEND (Out)	EDMA_CS (Out)	HSDI_SIG9	O	N/A (drives high)	1284_BUSY (Out)	EDMA_WR (Out)	HSDI_STATUS[1:0]	O	00	1x (see IEEE 1284 Interface)	01
PIN NAME	I/O	IEEE 1394 I/F	IEEE 1284 I/F	EXTERNAL DMA																																																									
HSDI_DATA[7:0]	I/O	BDI[7:0] (In/Out)	1284_D[7:0] (In/Out)	EDMA_DB[7:0] (In/Out)																																																									
HSDI_SIG1	O	BDIRW (Out)	1284_ERROR (Out)	EDMA_RD (Out)																																																									
HSDI_SIG2	O	BDIEN (Out)	1284_ACK (Out)	EDMA_DACK (Out) <sup>†</sup>																																																									
HSDI_SIG3	I or O	BDAVAIL (In)	1284_STROBE (In)	EDMA_A[3] (Out)																																																									
HSDI_SIG4	I/O, I or O	BDIF[2] (In/Out)	1284_SLCTIN (In)	EDMA_A[2] (Out)																																																									
HSDI_SIG5	I/O, I or O	BDIF[1] (In/Out)	1284_AF (In)	EDMA_A[1] (Out)																																																									
HSDI_SIG6	I/O or O	BDIF[0] (In/Out)	1284_SLT (Out)	EDMA_A[0] (Out)																																																									
HSDI_SIG7	I	BDIRQ (In)	1284_INIT (In)	EDMA_DREQ (In) <sup>†</sup>																																																									
HSDI_SIG8	O	N/A (drives high)	1284_PEND (Out)	EDMA_CS (Out)																																																									
HSDI_SIG9	O	N/A (drives high)	1284_BUSY (Out)	EDMA_WR (Out)																																																									
HSDI_STATUS[1:0]	O	00	1x (see IEEE 1284 Interface)	01																																																									
[1g] a bus arbiter; and	<p>AV7110 Preview discloses or at least renders obvious a bus arbiter. For example:</p> <p>“prioritized interrupt Interrupt requests are generated from internal modules like the TPP, OSD, A/V decoder, communication processor, and devices on the extension bus. Some of the requests are for data transfers to internal RAM, while others are true interrupts to the ARM CPU. The TC handles data transfers to internal RAM, while others are true interrupts to the ARM CPU. The TC handles data transfers, and the ARM provides services to true interrupts. The</p>																																																												

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>interrupts are grouped into FIQs and IRQs. The firmware will use FIQs, while the application software will use IRQs. The priorities for FIQs are managed by the firmware while those of IRQ are managed by the application software.” AV7110 Preview at 19.</p> <p>“video/audio buffer monitoring support The TC continuously monitors the fullness of the video and audio input buffers. If overflow or underflow occurs, a maskable FIQ interrupt will be used to alert the firmware so that corrective action can be taken in a timely manner. Alternatively, user software can periodically inspect (read access) the read/write pointers of the circular video and audio input buffers and take preemptive actions if overflow/underflow is deemed imminent. Moreover, the TC also keeps the number of bytes of video data being sent to the video decoder in a wrap-around counter. This byte-count is used by the firmware for accurate video PTS synchronization.” AV7110 Preview at 20.</p> <p>“interrupts There are three external interrupt lines on the extension bus of the 'AV7110. Each interrupt has a dedicated acknowledge pin (EXTACK[2:0]). One additional interrupt, BDIRQ (HSDI_ SIG7), is dedicated to the 1394 interface and it has no associated acknowledge signal. All the interrupts generate IRQ to the ARM and user application software needs to provide their service routine. These interrupts are handled by a centralized interrupt controller. The interrupt mask and priority are managed by the firmware. The BDIRQ and three extension bus interrupts are connected to a total of four different IRQs. When the interrupt handler on the ARM begins servicing one of the extension bus IRQs, it should first issue the corresponding acknowledge signal. At the completion of the IRQ, the ARM should reset the acknowledge signal.” AV7110 Preview at 53.</p> <p>“high speed data interface (HSDI) The 'AV7110 provides a high speed data interface. This allows the user to select between an external connection to an IEEE 1284 parallel peripheral, an IEEE 1394 device or an external DMA device. Logic for these three interfaces share signal pins and hence only one can be active at any given time. Table 28 shows the pin definitions for the HSDI in its various configurations. Switching from one interface to another will require a predefined sequence of API calls. Two signal pins (HSOI_ STATUS[1 :0]) indicate which of the three interfaces is active. They can be used to control external logic for interface arbitration. The definition of these signals is shown at the bottom of Table 28.” AV7110 Preview at 60.</p>

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	<div><p>Table 28. High Speed Data Interface Signal Pin Assignment</p><table><tr><th>PIN NAME</th><th>I/O</th><th>IEEE 1394 I/F</th><th>IEEE 1284 I/F</th><th>EXTERNAL DMA</th></tr><tr><td>HSDI_DATA[7:0]</td><td>I/O</td><td>BDI[7:0] (In/Out)</td><td>1284_D[7:0] (In/Out)</td><td>EDMA_DB[7:0] (In/Out)</td></tr><tr><td>HSDI_SIG1</td><td>O</td><td>BDIRW (Out)</td><td>1284_ERROR (Out)</td><td>EDMA_RD (Out)</td></tr><tr><td>HSDI_SIG2</td><td>O</td><td>BDIEN (Out)</td><td>1284_ACK (Out)</td><td>EDMA_DACK (Out)<sup>†</sup></td></tr><tr><td>HSDI_SIG3</td><td>I or O</td><td>BDAVAIL (In)</td><td>1284_STROBE (In)</td><td>EDMA_A[3] (Out)</td></tr><tr><td>HSDI_SIG4</td><td>I/O, I or O</td><td>BDIF[2] (In/Out)</td><td>1284_SLCTIN (In)</td><td>EDMA_A[2] (Out)</td></tr><tr><td>HSDI_SIG5</td><td>I/O, I or O</td><td>BDIF[1] (In/Out)</td><td>1284_AF (In)</td><td>EDMA_A[1] (Out)</td></tr><tr><td>HSDI_SIG6</td><td>I/O or O</td><td>BDIF[0] (In/Out)</td><td>1284_SLT (Out)</td><td>EDMA_A[0] (Out)</td></tr><tr><td>HSDI_SIG7</td><td>I</td><td>BDIRQ (In)</td><td>1284_INIT (In)</td><td>EDMA_DREQ (In)<sup>†</sup></td></tr><tr><td>HSDI_SIG8</td><td>O</td><td>N/A (drives high)</td><td>1284_PEND (Out)</td><td>EDMA_CS (Out)</td></tr><tr><td>HSDI_SIG9</td><td>O</td><td>N/A (drives high)</td><td>1284_BUSY (Out)</td><td>EDMA_WR (Out)</td></tr><tr><td>HSDI_STATUS[1:0]</td><td>O</td><td>00</td><td>1x (see IEEE 1284 Interface)</td><td>01</td></tr></table></div> <p>AV7110 Preview at 60 tbl. 28; <i>see also id.</i> tbl. 29 (listing different types of DMA transfers allowed for data ports).</p> <p>“IEEE 1394 interface</p> <p>On power-up the IEEE 1394 interface is enabled on the HSDI. An API call can be used to configure the HSDI for another mode or to return to the 1394 interface if necessary. To complete the 1394 implementation, the 'AV7110 requires an external packetizer and link layer controller, and a physical layer device. Figure 26 shows the connection between the 'AV7110 and these devices.” AV7110 Preview at 62; <i>see id.</i> at fig. 26.</p> <p>“IEEE 1284 interface</p> <p>The IEEE 1284 interface on the 'AV7110 has the following characteristics:</p> <ul style="list-style-type: none"><li>• Supports transfer of up to 10 Mbits/sec</li><li>• Supports the compatibility, nibble and byte mode</li><li>• Supports the ECP mode except for run length coding compression</li><li>• Does not support the EPP mode</li><li>• Peripheral mode only</li></ul> <p>The IEEE 1284 interface is used to connect the 'AV7110 to an external host. The 'AV7110 side of the protocol</p>	PIN NAME	I/O	IEEE 1394 I/F	IEEE 1284 I/F	EXTERNAL DMA	HSDI_DATA[7:0]	I/O	BDI[7:0] (In/Out)	1284_D[7:0] (In/Out)	EDMA_DB[7:0] (In/Out)	HSDI_SIG1	O	BDIRW (Out)	1284_ERROR (Out)	EDMA_RD (Out)	HSDI_SIG2	O	BDIEN (Out)	1284_ACK (Out)	EDMA_DACK (Out) <sup>†</sup>	HSDI_SIG3	I or O	BDAVAIL (In)	1284_STROBE (In)	EDMA_A[3] (Out)	HSDI_SIG4	I/O, I or O	BDIF[2] (In/Out)	1284_SLCTIN (In)	EDMA_A[2] (Out)	HSDI_SIG5	I/O, I or O	BDIF[1] (In/Out)	1284_AF (In)	EDMA_A[1] (Out)	HSDI_SIG6	I/O or O	BDIF[0] (In/Out)	1284_SLT (Out)	EDMA_A[0] (Out)	HSDI_SIG7	I	BDIRQ (In)	1284_INIT (In)	EDMA_DREQ (In) <sup>†</sup>	HSDI_SIG8	O	N/A (drives high)	1284_PEND (Out)	EDMA_CS (Out)	HSDI_SIG9	O	N/A (drives high)	1284_BUSY (Out)	EDMA_WR (Out)	HSDI_STATUS[1:0]	O	00	1x (see IEEE 1284 Interface)	01
PIN NAME	I/O	IEEE 1394 I/F	IEEE 1284 I/F	EXTERNAL DMA																																																									
HSDI_DATA[7:0]	I/O	BDI[7:0] (In/Out)	1284_D[7:0] (In/Out)	EDMA_DB[7:0] (In/Out)																																																									
HSDI_SIG1	O	BDIRW (Out)	1284_ERROR (Out)	EDMA_RD (Out)																																																									
HSDI_SIG2	O	BDIEN (Out)	1284_ACK (Out)	EDMA_DACK (Out) <sup>†</sup>																																																									
HSDI_SIG3	I or O	BDAVAIL (In)	1284_STROBE (In)	EDMA_A[3] (Out)																																																									
HSDI_SIG4	I/O, I or O	BDIF[2] (In/Out)	1284_SLCTIN (In)	EDMA_A[2] (Out)																																																									
HSDI_SIG5	I/O, I or O	BDIF[1] (In/Out)	1284_AF (In)	EDMA_A[1] (Out)																																																									
HSDI_SIG6	I/O or O	BDIF[0] (In/Out)	1284_SLT (Out)	EDMA_A[0] (Out)																																																									
HSDI_SIG7	I	BDIRQ (In)	1284_INIT (In)	EDMA_DREQ (In) <sup>†</sup>																																																									
HSDI_SIG8	O	N/A (drives high)	1284_PEND (Out)	EDMA_CS (Out)																																																									
HSDI_SIG9	O	N/A (drives high)	1284_BUSY (Out)	EDMA_WR (Out)																																																									
HSDI_STATUS[1:0]	O	00	1x (see IEEE 1284 Interface)	01																																																									



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	<p>can be handled by an IEEE 1284 peripheral interface controller on the chip such as the SN54ACT1284/SN? 4ACT1284. Since the signals on the HSDI are 5-V-tolerant, they can be connected directly to this external 1284 driver.” AV7110 Preview at 69; see id. fig.33; see also id. at 69-70.</p> <div> <p>Figure 26. 1394 Interface</p> </div> <p>AV7110 Preview at 62; <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) C packets to and from the internal data RAM. This data can then be processed by the user software as needed.”); <i>see also id.</i> at 63 (listing signals associated with the 1394 interface).</p>
[1h] a multimedia data stream processor; and	<p>AV7110 Preview discloses or at least renders obvious a multimedia data stream processor. For example:</p> <p>“The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or</p>

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	<p>containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.” AV7110 Preview at 13.</p> <p>“Together with the ARM, the TPP also handles program clock reference (PCR) recovery with an external VCXO. The TPP will latch and transfer to the ARM its internal system clock upon the arrival of any packet which contains a PCR. After further processing on the packet and identifying the system clock, the ARM calculates the difference between the system clock from a bit-stream and the actual system clock at the time the packet arrives. Then, the ARM filters the difference and sends it through an 8-bit sigma-delta DAC to control the external VCXO. The ARM will drive the VCXO to its center frequency during start-up or, if enabled by an API, after channel change when there is no incoming PCR.” AV7110 Preview at 13; see also id. at 22-23.</p> <div> <p>The diagram illustrates a system architecture. At the top left, a 'Transport Bitstream From Front End' enters a 'TPP' (Traffic Processing Processor) block. The TPP is connected to an 'HSDI' block containing '1394 I/F', '1284 I/F', and 'Ext DMA'. The TPP also connects to an 'ECD' (Error Correction Decoder) block. Both the TPP and ECD connect to a central 'Traffic Controller' block. The Traffic Controller is bidirectionally connected to 'External System Memory'. It also connects to a 'Video Decoder' block, which in turn connects to an 'OSD' (On-Screen Display) block and an 'NTSC/PAL Encoder' block. The 'Audio Decoder' block connects to the Traffic Controller and outputs 'PCM Audio Output' and 'SPDIF Output'. The 'OSD' and 'NTSC/PAL Encoder' output 'Digital Video Output' and 'Y/C or RGB and Composite Video'. At the bottom, a 'Communication Processor' block is connected to the Traffic Controller and has multiple interfaces: '12C', 'Smart Card', 'UART (Three)', 'JTAG', 'IR', and 'GPIO'. It is also connected to an 'Extension Bus Interface' block. To the right of the Communication Processor are 'ARM/Thumb', 'Data RAM', and 'ROM' blocks, all connected to a common system bus.</p> </div> <p>AV7110 Preview at 12 fig. 1.</p>

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	<p>“MPEG transport decoder (TPP)  TPP module  features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15  Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32  Maximum number of pairs of keys for the descrambler ..... 16  Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the</p>

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	<p>CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination. The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“conditional access and descrambling processing  The 'AV7110 contains a full implementation of the ECD hardware.  The descrambling of the incoming data is performed automatically with minimum intervention by the CPU. The TPP module detects which transport packets are scrambled, at either the program elementary stream (PES) or the transport stream level, and routes the data through the ECD as necessary. The ECD stores the descrambler keys locally and automatically selects the correct key of a specific PID. Up to 16 sets of keys are stored in the key table for use by the ECD. It is possible for more than one PIO to use the same key. The descrambler keys are derived by the conditional access software using the command packet from the bit-stream.” AV7110 Preview at 23.</p>

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	<div> <p style="text-align: center;"><b>Figure 26. 1394 Interface</b></p> </div> <p>AV7110 Preview at 62; <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) C packets to and from the internal data RAM. This data can then be processed by the user software as needed.”); <i>see also id.</i> at 63 (listing signals associated with the 1394 interface).</p> <p>“communication processor features</p> <ul style="list-style-type: none"> <li>• Provides two programmable timers</li> <li>• Provides 3 general purpose UARTs - two at up to 115.2 Kbps and one at up to 9.6 Kbps</li> <li>• Accepts IR input signals</li> <li>• Generates IR output signals</li> <li>• Provides up to nine general purpose I/Os</li> <li>• Manages I2C and JTAG interfaces</li> </ul> <p>This module contains a collection of buffers, control registers, and control logic for various interfaces, such as UARTs, IR, and I2C, and JTAG. All the buffers and registers are memory mapped and individually managed by the ARM CPU. Interrupts are used to communicate between these interface modules and the ARM CPU.”</p>

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	<p>AV7110 Preview at 72; <i>see generally id.</i> at 72-78 (describing different functions and functional blocks of the communication processor).</p> <p>“UARTs The 'AV7110 includes three general purpose UARTs that are memory mapped and fully accessible by user application programs. A set of APIs exists to assist in programming them. The output of the UARTs are digital and require external level shifters for RS232 compliance. These UARTs support full duplex mode and are double buffered with sufficient FIFO space to minimize the interrupt frequency to the ARM even when they are operating at their maximum transmission speeds. UART 1 and 2 support handshaking through RTS and CTS signals. They work with baud rates of 1200, 2400, 4800, 9600, 14,400, 19,200, 28,800, 57,600 and 115,200 bps. These two UARTs transmit/receive 1 start bit, 7 or 8 data bits, optional parity, and 1 or 2 stop bits. UART 3 has no support for hardware handshaking, it works with baud rates of 1200, 2400, 4800, 9600 bps. It is possible for the user application software to implement software handshaking with any of the UARTs. The UARTs are fully accessible using the API and can generate interrupts when data is received or the transmit buffer is empty. The CPU also has access to a status register for each UART that contains flags for such errors as data overrun or framing errors.” AV7110 Preview at 75.</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SDRAM, and produces three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs. After being configured and activated by the ARM CPU, the OSD module reads OSD data and mixes it with the video output. The CPU is responsible for turning on and off OSD operations. The bitBLT hardware which is attached to the OSD module provides acceleration for memory block moves and graphics operations.” AV7110 Preview at 33; <i>see id.</i> (showing block diagram of the OSD module).</p>
[1i] a storage subsystem communicatively connected to the media switch, wherein multimedia data are stored on the storage subsystem and	<p>AV7110 Preview discloses or at least renders obvious a storage subsystem communicatively connected to the media switch, wherein multimedia data are stored on the storage subsystem and retrieved from the storage subsystem essentially simultaneously. For example:</p> <p>“After removing packet headers and other system related information, both audio and video data is stored in the</p>

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retrieved from the storage subsystem essentially simultaneously.	<p>external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards. The chip decodes MPEG-1 and MPEG-2 main profile at main level for video and Layer I and II MPEG-1 and MPEG-2 stereo for audio. Both video and audio decoders synchronize their presentation of reconstructed data using the transmitted presentation time stamps (PTS) and their local system clock. The local system clock is continuously updated by the ARM.” AV7110 Preview at 13.</p> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PIO table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.</p> <p>The only difference between the two scenarios is that in the case where there is no TPP traffic, the TPP buffer pool can be used. In the case where there is active TPP data, a general purpose buffer needs to be used. Additionally, when TPP data traffic is active, the end of packet (EOP) interrupt generation will require an indication data type configured in the header, which describes where the data to be processed is to be found.” AV7110 Preview at 21.</p> <p>“trick mode When decoding a picture from a digital recorder, the decoder can handle trick modes (decode and display I frame only). The limitation is that the data has to be a whole picture instead of several intra-slices. Random bits are allowed in between trick mode pictures. It is important to note that if the random bits emulate a start code, unpredictable decoding and display errors will like occur.</p>

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	<p>During trick mode decoding, the video decoder repeats the following steps:</p> <ul style="list-style-type: none"> <li>• Searches for a sequence header followed by an I picture</li> <li>• Ignores the video buffer under-flow error <ul style="list-style-type: none"> <li>• Continuously displays the decoded I frame.”</li> </ul> </li> </ul> <p>AV7110 Preview at 26; <i>see id.</i> tbl. 6 (showing video decoder commands enabling trick mode functionality).</p> <p>“The HSDI supports the following concurrent data transfers.</p> <ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/program to 1394 (using dedicated I/F - see NOTE XXXX of Table 29)</li> <li>• TPP/program to decoder; 1394/DMA to/from memory</li> <li>• TPP/program to decoder; memory/DMA to/from HSDI</li> <li>• TPP/program to decoder; TPP/DMA to HSDI</li> <li>• TPP/program to decoder; TPP/program to 1394; memory/DMA to/from 1394</li> <li>• TPP/program to decoder; 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; TPP/DMA to 1394” AV7110 Preview at 61.</li> </ul> <div> <p><b>Figure 25. Functional Block Diagram of High Speed Data Interface</b></p> </div> <p>AV7110 Preview at 61 (showing the functional blocks of the HSDI); <i>see also id.</i> at 62-65 (showing describing AV7110’s reading and writing of data from/to the 1394 interface).</p> <p>“AV7110 internal data path for 1394</p>



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	<p>In recording mode, the 'AV7110 sends either encrypted or clean packets to the 1394 interface. The packet will be transferred as soon as it arrives. When recording encrypted data, the ECD module is bypassed. In the case of recording decrypted byte, the TPP sends the encrypted part of the payload to the ECD module, and then forwards each byte to the 1394 interface. No CPU processing is done to the packet during recording. The TPP automatically modifies the header if the packet is decrypted.</p> <p>Note that the same bit stream cannot be sent to the 1394 interface twice (such as, once after decryption, and twice as part of a full transport stream with the by-pass capability). Both Timon and the 'AV7110 support only one MPEG-2 transport stream channel on the bulky data interface.</p> <p>During playback mode, MPEG-2 transport packets coming from the 1394 interface go directly to the TPP module. Figure 29 shows the functional block diagram of the data flow between the TPP, ECD, and 1394 interface. Note that the major portion of the 1394 interface function is implemented in the HSDI module. Dedicated data lines are used for the 1394 interface that allows the 'AV7110 to work in different modes.</p> <ul style="list-style-type: none"> <li>• Decode/decrypt/display one channel and record it</li> <li>• Decode/decrypt/display one channel and record it encrypted (pay-per-view)</li> <li>• Decode/display one channel while recording all or part of 32 PIDs from a transponder, with each selected PIDs either encrypted or decrypted. In addition non selected PIDs can also be recorded in their original format (decryption is not possible for non selected PIDs).</li> <li>• While the TPP is receiving MPEG-2 data from the 1394 port, the 'AV7110 can also record part of the bit stream it is receiving to the 1394 port</li> <li>• Send the whole transport stream from the FEC to the 1394 port without any filtering or decryption and, at the same time, decode/decrypt/display a program from either the same transport stream or from another transport stream received through the 1394 port..” AV7110 Preview at 65.</li> </ul>

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	<div> <p><b>Figure 25. 1394 Data Flow Block Diagram</b></p> </div> <p>AV7110 Preview at 69 fig. 25 (showing functional block diagram of data flow between TPP, ECD, and 1394 interface).</p> <p>“Since there is only an 8-bit bus on the HSDI, the ESC is limited to an 8-bit, single bus architecture so its mode selection inputs should be set to mode 0. The upper data bits can be left floating since they have internal pullups on the ESC. Likewise, the AD<sup>?</sup>-0 inputs of the ESC will not be used for this mode and can be left unconnected. The ESC requires an external clock source from 10 MHz to 40 MHz. Since the CLK40 signal of the 'AV7110 is actually a 40.5 MHz clock it cannot be used directly for this controller without violating its specification. Table 32 shows the signals needed for the EDMA interface.” AV7110 Preview at 66; <i>see id.</i> tbl. 32 (listing EDMA interface signals).</p> <p>“When configured for EDMA operation (HSDI_ STATUS[1 LO] = 01), the HSDI is capable of a glue less connection to an external enhanced SCSI controller (ESC) device such as the NCR 53CF94-1 /53CF96-1. Figure 30 shows the connections for this example configuration.</p> <p>. . . .</p> <p>All data transfers (using the HSDI DMA unit) as well as external controller communications (using the A[3:0] output signals), are controlled by the firmware. Firmware will handle MPEG-2 program stream and MPEG-1 system stream input. This firmware will not be available with the initial samples of the 'AV7110. The other input data formats will be handled by user application software. This includes specific interfaces such as the ESC. Table 33 details the EDMA register which allows the user to configure the wait states and other factors of the EDMA port.” AV7110 Preview at 66, 67.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<div> <p style="text-align: center;">Figure 26. 1394 Interface</p> </div> <p>AV7110 Preview at 62; <i>see id.</i> (“The command and control between the packetizer or the link layer interface device and the CPU is transmitted via the extension bus. The MPEG packet data from the bulk 1394 is transferred via dedicated pins on the 1394 interface from/to the TPP. The HSDI DMA channel is used for transferring isochronous (I) or asynchronous (A) C packets to and from the internal data RAM. This data can then be processed by the user software as needed.”); <i>see also id.</i> at 63 (listing signals associated with the 1394 interface).</p> <p>“The application software interfaces with the peripheral interface controller via RTSL API calls. To send data to the host the application software will issue an API call to transfer the data from memory to the peripheral interface via a DMA. To receive data from the host, the application software will issue an API to transfer a predetermined number of bytes from the peripheral interface to internal data memory via the HSDI DMA unit. The user application software must have a way to determine the number of bytes of data that is expected from the host.” AV7110 Preview at 70.</p> <p>“Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM, and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.</p> <p>....</p> <p>After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards. The chip decodes MPEG-1 and MPEG-2 main profile at main level for video and Layer I and II MPEG-1 and MPEG-2 stereo for audio. Both video and audio decoders synchronize their presentation of reconstructed data using the transmitted presentation time stamps (PTS) and their local system clock. The local system clock is continuously updated by the ARM.” AV7110 Preview at 13.</p> <p>“The SDRAM must be 16-bits wide. The 'AV7110 provides control signals for up to two SDRAMs. Any combination of 4 or 16 Mbit SDRAMs may be used, provided they total at least 16 Mbits. The SDRAM must operate at an 81 MHz clock frequency and have the same timing parameters as the TI TMS626162, a 16 Mbit SDRAM. Other supported sizes and configurations are:</p> <p>16 Mbit → one 16 Mbit SDRAM  20 Mbit → one 16 Mbit and one 4 Mbit SDRAM  32 Mbit → two 16 Mbit SDRAM</p> <p>The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 2D macroblock. The interface also supports decrement mode for bitBLT block transfers.</p> <p>....</p> <p>During DVB decoding, the 'AV7110 allocates the 16 Mbit SDRAM for PAL mode according to the default layout shown in Table 2. All the address pointers of the SDRAM partitioning are user programmable and hence the actual layout can be customized according to needs.” AV7110 Preview at 19.</p> <p>“memory usage reduction</p> <p>In the minimum memory configuration, the 'AV7110 is designed to work with two memory devices: a single 16 Mbit SDRAM device for system data storage (audio, video data, etc.) and a 4 Mbit DRAM for local data storage (private data, SI information, etc.). Table 11 shows what the two memories are used for, in bytes. The amount of memory available for OSD applications depends upon the mode of operation of the 'AV7110. For example, if the letterbox display format is used, more memory is required to store B frames and hence less OSD space will be available.” AV7110 Preview at 30.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“Figure 27 shows the functionality of the interface signals when the 'AV7110 reads data from Timon. The maximum input rate of MPEG-2 data coming from Timon and routed through the transport stream hardware demultiplexer block (TPP) is approximately 64.8 Mbits/second. The maximum input bit rate over one transport packet is 60 Mbits/second.</p> <p>....</p> <p>When the 'AV7110 writes data to Timon (record mode), it drives BDIF, BDIEN, and BDIRW for one clock (system) period. BDIEN is driven low for only one byte and must be driven high between two byte transmissions. This is shown in Figure 28.” AV7110 Preview at 64; <i>see also id.</i> figs. 27-28.</p> <p><i>See also</i> claim 1 at 1e, <i>supra</i>.</p>
Claim 6	
6. The system of claim 1, the decoder subsystem further comprising a transport stream decoder/graphics subsystem.	AV7110 Preview discloses or at least renders obvious the decoder subsystem further comprising a transport stream decoder/graphics subsystem. For example:

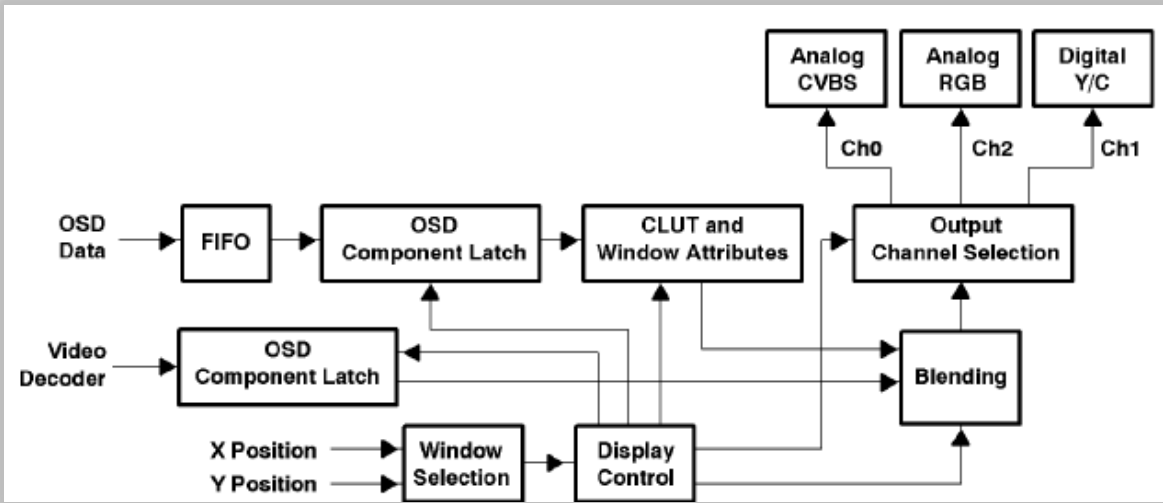
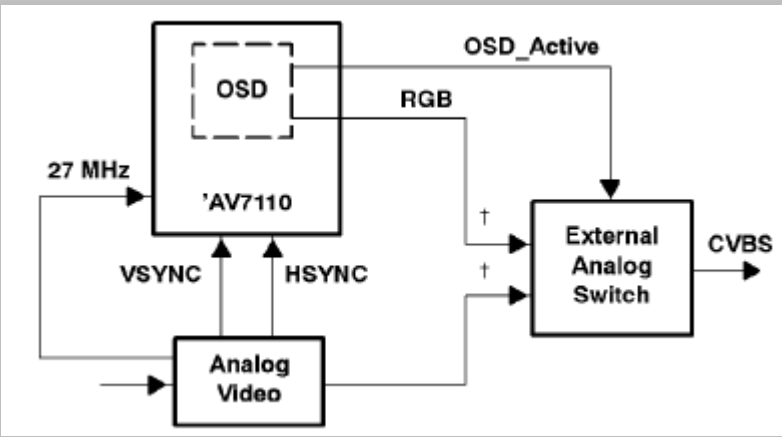
'476 Patent Claim	Exemplary Prior Art Disclosure
	<div><p>The diagram illustrates a system architecture. At the top left, a 'Transport Bitstream From Front End' feeds into a 'TPP' (MPEG transport decoder) block. The 'TPP' is connected to a '1394 I/F' block, which is part of a larger block containing '1284 I/F' and 'Ext DMA'. This block is connected to a 'Communication Processor' at the bottom left. The 'Communication Processor' has multiple external interfaces: 'GPIO', 'IR', 'JTAG', 'UART (Three)', 'Smart Card', and '12C'. A 'Traffic Controller' is connected to the 'TPP', '1394 I/F', 'External System Memory', 'Video Decoder', and 'Audio Decoder'. The 'Video Decoder' is connected to an 'OSD' block, which then feeds into an 'NTSC/PAL Encoder'. The 'Audio Decoder' outputs 'PCM Audio Output' and 'SPDIF Output'. The 'NTSC/PAL Encoder' outputs 'Y/C or RGB and Composite Video'. The 'OSD' outputs 'Digital Video Output'. The 'Traffic Controller' is also connected to 'External System Memory'. At the bottom, a horizontal bus connects the 'Communication Processor', 'Extension Bus Interface', 'ARM/Thumb', 'Data RAM', and 'ROM'.</p></div> <p>AV7110 Preview at 12 fig. 1.</p> <p>“MPEG transport decoder (TPP) TPP module features</p> <ul style="list-style-type: none"><li>• Parses transport bit streams</li><li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li><li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li></ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps Maximum input bit rate through the 1394 interface ..... 64.8 Mbps Maximum video bit rate ..... 15 Mbps Maximum audio bit rate ..... 1.13 Mbps</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec</p> <p>Maximum number of PIDs that can be filtered ..... 32</p> <p>Maximum number of PIDs that can be descrambled ..... 32</p> <p>Maximum number of pairs of keys for the descrambler ..... 16</p> <p>Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination. The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“video output interfaces</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>analog video output - NTSC/PAL encoder module</p> <ul style="list-style-type: none"> <li>• Supports NTSC and PAL B, D, G/H, and I display formats</li> <li>• Outputs Y/C or RGB, and composite video with 9-bit DACs</li> <li>• Generates 100/75 format color bar for PAL mode testing</li> <li>• Complies to the RS170A standard</li> <li>• Composite and RGB signals comply with ITU-R BT.470-3 and ITUR BT.471-1</li> <li>• Supports Macro Vision anti-taping function on composite video</li> <li>• Provides sync signals with option to accept external sync signals</li> </ul> <p>The composite video output can be either PAL or NTSC format. The default output format is PAL at powerup. Changing between NTSC and PAL mode can be done via an API which selects the output mode of the NTSC/PAL encoder. Note that the video decoder microcode ROM is specific to NTSC or PAL and required for proper operation.</p> <p>The sync signal pins Vsync and Hsync on the 'AV7110 are defaulted to 3-state mode at powerup, where internally generated sync signals will be used by the NTSC/PAL encoder. The user can then select the source of video sync signals via an API. If internal source is selected then the Vsync and Hsync pins will be configured as output pins. In addition to composite video, the 'AV7110 also provides either an analog S-video (Y - luminance , C - chrominance) signal or an analog RGB output with 720 pixel resolution. All outputs conform to the RS170A standard. Selection of RGB or S-video output is done via API software. Macro Vision version 7 is enabled via an API; the default state is off. A version of the 'AV7110 where the MacroVision anti-taping circuitry is permanently disabled is also available.” AV7110 Preview at 39.</p> <p>“digital video output (not supported when 32-bit EBI is used)</p> <p>PAL mode digital video output</p> <p>The digital output is in 4:2:2 component format. The content of the video could be either pure video or the blended combination of video and OSD. The pin assignments for the digital video output signals are:</p> <p style="padding-left: 40px;">YCOUT(8) 8-bit Cb/Y/Cr/Y data output</p> <p style="padding-left: 40px;">YCCLK(1) 27 MHz clock output</p> <p>The timing of 4:2:2 digital video output is shown in Figure 12.</p> <p>...</p> <p>NTSC mode digital video output</p> <p>The digital output includes video in either 4:4:4 or 4:2:2 component format, plus the aspect ratio VARIS code at the beginning of each video frame. The video output format is programmable by the user but defaults to 4:2:2. The content of the video could be either pure video or the blended combination of video and OSD.</p>



'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>The pin assignments for the digital video output signals are:</p> <p>YCOUT(8) 8-bit Cb/Y/Cr/Y and VARIS multiplexed data output</p> <p>YCCLK(1) 27 MHz clock output</p> <p>YCCTRL(2) 2-bit control signals to distinguish between Y/Cb/Cr components and VARIS code</p> <p>The interpretation of YCCTRL is defined in Table 20.</p> <p>...” AV7110 Preview at 41.</p> <p>“PCM audio output</p> <p>The PCM audio output from the 'AV7110 is a serial PCM data line, with associated bit clock (ASCLK) and left/right clock (LRCLK). PCM data is output serially on PCM OUT using the serial clock ASCLK as shown in Figure 15. The data output of PCM OUT alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7110 Preview at 46; <i>see generally id.</i> at 46-47 (describing additional aspects of PCM audio output).</p> <p>“elementary stream playback</p> <p>In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.</p> <p>SPDIF audio output</p> <p>The SPDIF output conforms to the consumer format of the AES3 standard for serial transmission of digital audio data. When using an external PLL (PCMSRC=1), SPDIF is supported only if Bx over-sampled PCMCLK is supplied (that is, PCMSEL[0]=1).” AV7110 Preview at 48.</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SDRAM, and produces three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs. After being configured and activated by the ARM CPU, the OSD module reads OSD data and mixes it with the video output. The CPU is responsible for</p>

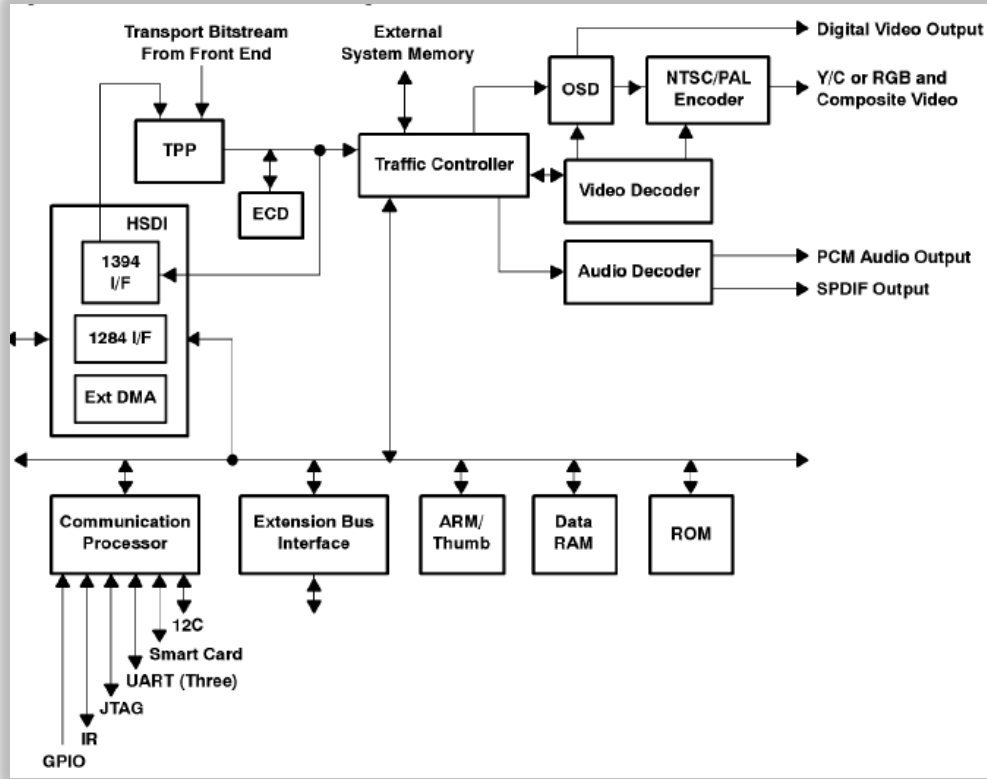
'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>turning on and off OSD operations. The bitBLT hardware which is attached to the OSD module provides acceleration for memory block moves and graphics operations.” AV7110 Preview at 33.</p> <div>  <p>The diagram illustrates the internal architecture of the OSD module. It features two input paths: 'OSD Data' and 'Video Decoder'. 'OSD Data' passes through a 'FIFO' and an 'OSD Component Latch' before entering the 'CLUT and Window Attributes' block. The 'Video Decoder' also passes through an 'OSD Component Latch'. Both 'OSD Component Latch' blocks feed into the 'CLUT and Window Attributes' block. Additionally, 'X Position' and 'Y Position' inputs feed into a 'Window Selection' block, which also feeds into the 'CLUT and Window Attributes' block. The 'CLUT and Window Attributes' block outputs to an 'Output Channel Selection' block. A 'Blending' block receives inputs from the 'CLUT and Window Attributes' block and the 'Output Channel Selection' block. The 'Blending' block outputs to the 'Output Channel Selection' block, which then routes the signal to three output channels: 'Analog CVBS' (labeled Ch0), 'Analog RGB' (labeled Ch2), and 'Digital Y/C' (labeled Ch1). A 'Display Control' block receives inputs from the 'Window Selection' block and the 'CLUT and Window Attributes' block, and it also feeds into the 'Blending' block.</p> </div> <p>AV7110 Preview at 33 fig. 8 (showing block diagram of the OSD module).</p> <div>  <p>This diagram shows the AV7110 chip and its external connections. The 'Analog Video' block provides 'VSYNC' and 'HSYNC' signals to the AV7110 chip. A '27 MHz' clock signal is also input to the chip. Inside the AV7110 chip, there is a dashed box labeled 'OSD'. The chip outputs an 'RGB' signal and an 'OSD_Active' signal to an 'External Analog Switch'. The 'Analog Video' block also outputs a signal to the 'External Analog Switch'. The 'External Analog Switch' combines these signals and outputs a 'CVBS' signal.</p> </div>

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	<p>AV7110 Preview at 36 fig. 9.</p> <p><i>See claim 1 at 1c, supra.</i></p>
Claim 7	
<p>7. The system of claim 6, wherein the transport stream decoder/graphics subsystem includes at least one of: a host bridge; a memory controller; an MPEG-3 transport demultiplexer; an MPEG-3 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller.</p>	<p>AV7110 Preview discloses or at least renders obvious the transport stream decoder/graphics subsystem includes at least one of: a host bridge; a memory controller; an MPEG-3 transport demultiplexer; an MPEG-3 decoder; an audio/video decoder; a graphics processor; a bus bridge; or a bus controller For example:</p> <p><i>See AV7110 Preview at 1 (stating that the AV7110 includes an “On-Chip SDRAM Controller for 16, 20, or 32 Mbit SDRAM”).</i></p> <p>“The SDRAM must be 16-bits wide. The 'AV7110 provides control signals for up to two SDRAMs. Any combination of 4 or 16 Mbit SDRAMs may be used, provided they total at least 16 Mbits. The SDRAM must operate at an 81 MHz clock frequency and have the same timing parameters as the TI TMS626162, a 16 Mbit SDRAM. Other supported sizes and configurations are:</p> <p>16 Mbit → one 16 Mbit SDRAM  20 Mbit → one 16 Mbit and one 4 Mbit SDRAM  32 Mbit → two 16 Mbit SDRAM</p> <p>The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 2D macroblock. The interface also supports decrement mode for bitBLT block transfers.</p> <p>....</p> <p>During DVB decoding, the 'AV7110 allocates the 16 Mbit SDRAM for PAL mode according to the default layout shown in Table 2. All the address pointers of the SDRAM partitioning are user programmable and hence the actual layout can be customized according to needs.” AV7110 Preview at 19.</p> <p>“traffic controller (TC) features</p> <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>• Authorizes and manages DMA transfers</li> <li>• Provides SDRAM interface</li> <li>• Manages extension bus</li> </ul>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• Provides memory access protection</li> <li>• Manages the data flow between processors and memories <ul style="list-style-type: none"> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> <li>- Audio/video decoder to/from SDRAM</li> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> </ul> </li> <li>• Generates chip selects (CS) for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus</li> <li>• Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.</li> </ul> <p>“Software on the 'AV7110 is divided into three sections: firmware, API, and user software. Firmware is masked into the internal ROM of the 'AV7110. This software is supplied by Texas Instruments (TI™) and is used for low level control of the hardware and bit-stream demultiplexing in the 'AV7110. The user software is resident in external memory and contains all the software written by the user. The user software communicates with the firmware through application programming interfaces (AP Is). These AP Is are contained in external ROM. APIs are written by TI and provided in the form of run time support library (RTSL).” AV7110 Preview at 13.</p> <p>“The 'AV7110 uses the STC and PTS to determine the play back time of the decoded audio and video data. The relationship between STC and PTS is determined at the time of the generation of the generation of the respective elementary streams (ES). Upon reception, the demultiplexing software in the 'AV7110 extracts the video PTS and inserts it in an array of PTS and byte-count information maintained for the video decoder. For the audio the PTS information is extracted by the audio decoder front end from the PES. The video decoder contains an STC counter that is clocked by the system clock (27 MHz) and normalized to a 90 kHz reference. The audio decoder does not contain a counter. Instead, it gets updated from the system time reference counter every 1 .4 ms.” AV7110 Preview at 48.</p> <p>“Figure 27 shows the functionality of the interface signals when the 'AV7110 reads data from Timon. The maximum input rate of MPEG-2 data coming from Timon and routed through the transport stream hardware demultiplexer block (TPP) is approximately 64.8 Mbits/second. The maximum input bit rate over one transport packet is 60 Mbits/second.” AV7110 Preview at 64; <i>see also id.</i> fig. 27.</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“MPEG transport decoder (TPP)  TPP module  features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15  Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32  Maximum number of pairs of keys for the descrambler ..... 16  Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the</p>

'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination. The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p>

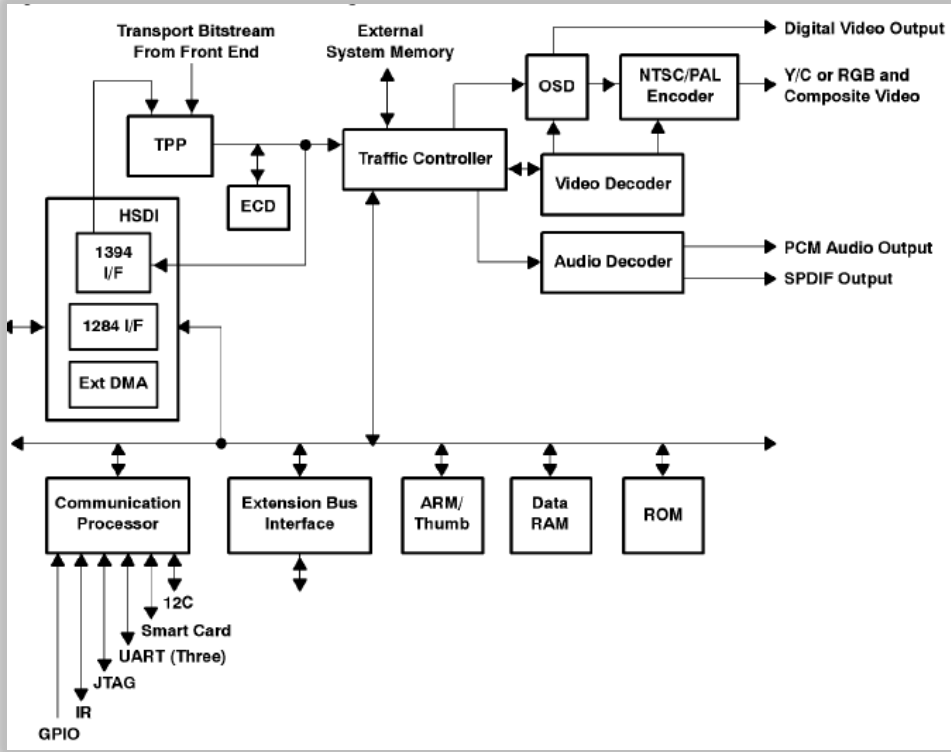
'476 Patent Claim	Exemplary Prior Art Disclosure
	 <p>The diagram illustrates the AV7110 system architecture. A 'Transport Bitstream From Front End' enters a 'TPP' (Transport Processing Processor) block. The TPP is connected to an 'HSDI' block containing '1394 I/F', '1284 I/F', and 'Ext DMA'. The HSDI block is connected to a 'Traffic Controller' block. The Traffic Controller is also connected to 'External System Memory' and an 'OSD' (On-Screen Display) block. The OSD block is connected to an 'NTSC/PAL Encoder' block, which produces 'Digital Video Output' and 'Y/C or RGB and Composite Video'. The Traffic Controller is also connected to a 'Video Decoder' block, which produces 'PCM Audio Output' and 'SPDIF Output'. The Traffic Controller is connected to a 'Communication Processor' block, which is connected to an 'Extension Bus Interface' block. The Communication Processor is also connected to 'ARM/Thumb', 'Data RAM', and 'ROM' blocks. The Communication Processor is connected to various external interfaces: 'GPIO', 'IR', 'JTAG', 'UART (Three)', 'Smart Card', and '12C'.</p> <p>AV7110 Preview at 12 fig. 1.</p> <p>“The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SDRAM, and produces three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs. After being configured and activated by the ARM CPU, the OSD module reads OSD data and mixes it with the video output. The CPU is responsible for turning on and off OSD operations. The bitBLT hardware which is attached to the OSD module provides acceleration for memory block moves and graphics operations.” AV7110 Preview at 33; <i>see also id.</i> fig. 8</p>

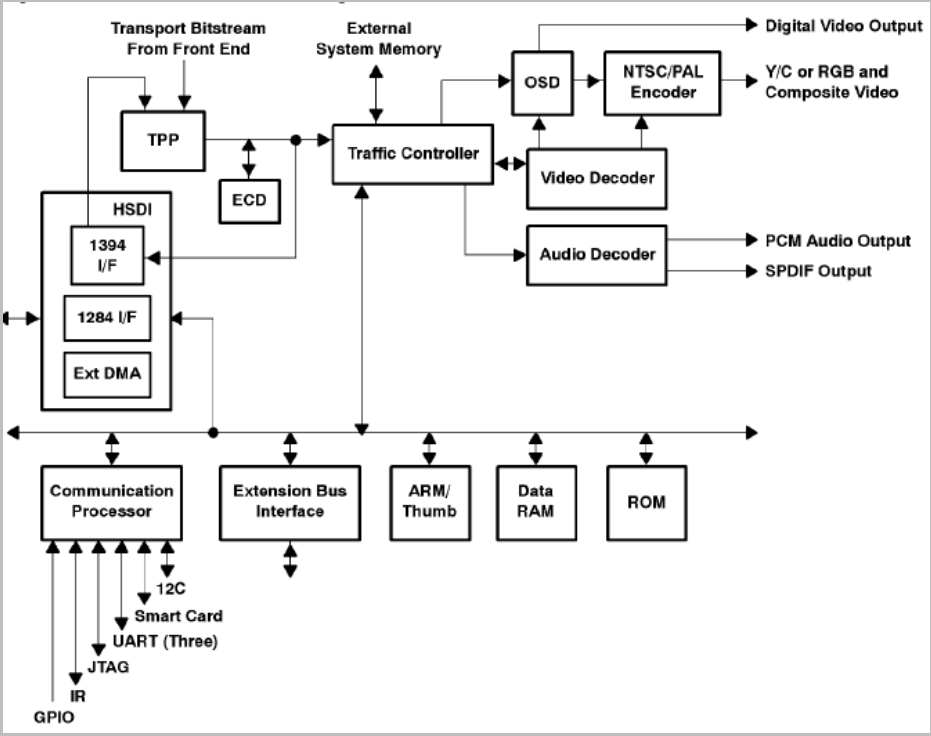
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	<p>(showing block diagram of the OSD module); <i>id.</i> at 36 fig. 9 (showing use of OSD_ACTIVE signal for external analog video).</p> <p>“The video decoder module receives a video bit-stream from the SDRAM. It also uses the SDRAM as its working memory to store tables, buffers, and reconstructed images. The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.” AV7110 Preview at 25-26.</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers I and II</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Outputs in both PCM and SPDIF formats</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information</li> <li>• Supports half-frequency modes</li> <li>• Supports playback of 16-bit PCM data (PCM bypass), audio elementary stream, and audio PES</li> <li>• Provides read/write accesses to audio input buffers read/write pointers</li> </ul> <p>The audio module receives MPEG compressed audio data from the TC, decodes it, and outputs audio samples in PCM format. APIs are provided for the ARM CPU to initialize/control the audio decoder via a control register and to read status information from the decoder's status register.</p> <p>Audio frame data and PTS information are stored in the SDRAM in packet form. The audio module decodes the packets to extract the PTS and audio data. The audio decoder uses this PTS value to perform playback synchronization (see Synchronization for more details). It is application software's responsibility to determine and enable the PIO of the MPEG-1 compliant bit-stream in a MPEG-2 audio program which contains both the MPEG-1 compliant bit-stream and the MPEG-2 extension bit-stream.</p> <p>The ARM can control the operation of the audio module via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and over-sampling ratio, and choose the output format for dual channel mode. The ARM will also be able to read status information from the audio module. One 32-bit register</p>



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	<p>provides the MPEG header information and sync, CRC, and PCM status.” AV7110 Preview at 44; see also id. at 45-46 (listing registers used by the audio module).</p> <p><i>See</i> claim 1 at 1c and claim 6, <i>supra</i>.</p>
Claim 8	
<p>8. The system of claim 7, the transport stream decoder/graphics subsystem further comprising at least one transport stream interface, wherein the transport stream interface receives the transport stream from the input section.</p>	<p>AV7110 Preview discloses or at least renders obvious the transport stream decoder/graphics subsystem further comprising at least one transport stream interface, wherein the transport stream interface receives the transport stream from the input section. For example:</p> <p>“MPEG transport decoder (TPP) TPP module features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15 Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32  Maximum number of pairs of keys for the descrambler ..... 16  Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet</p>

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	<p>should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination. The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“transport parser input interface The ‘AV7110 accepts DVB transport packet data from a front end such as a Forward Error Correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB Conditional Access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23; see also id. at 24 tbl. 4 (describing transport packet input interface pin description).</p> <p>See AV7110 Preview at 1 (“[TMS320AV7110] [a]ccepts Transport bit-streams of Up to 72.8Mbps Burst Rate (60 Mbps average Over One Transport Packet.”).</p>

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	 <p>AV7110 Preview at 12 fig. 1.</p> <p>See also claim 1 at 1c, and claims 6-7, <i>supra</i>.</p>
Claim 9	
<p>9. The system of claim 7, wherein the transport stream is demultiplexed into audio and video packet streams, wherein the audio and video packet</p>	<p>AV7110 Preview discloses or at least renders obvious the transport stream is demultiplexed into audio and video packet streams, wherein the audio and video packet streams are stored and played back through an output side of the transport stream decoder/graphics subsystem. For example:</p>

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<p>streams are stored and played back through an output side of the transport stream decoder/graphics subsystem.</p>	 <p>AV7110 Preview at 12 fig. 1.</p> <p>“The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO), and MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infra-red (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.” AV7110 Preview at 1.</p> <p>“transport parser input interface</p>

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	<p>The 'AV7110 accepts DVB transport packet data from a front end such as a Forward Error Correction (FEC) unit. Data is input one byte at a time using DCLK. PACCLK indicates when the data is valid. BYTE_START signals the first byte of a 188 byte packet. The interface is compatible with the common DVB Conditional Access. The diagram in Figure 6 shows the input timing for this interface.” AV7110 Preview at 23; see also id. at 24 tbl. 4 (describing transport packet input interface pin description).</p> <p>“The 'AV7110 accepts a DVB transport bit-stream from the output of a forward error correction (FEC) device with a maximum (burst) throughput of 72.8 Mbits/s or 9.1 Mbytes/s (60Mbps average over one transport packet). The transport packet parser (TPP) in the 'AV7110 processes the header of each packet and decides whether the packet should be discarded, further processed by ARM CPU, or if the packet only contains relevant data and needs to be stored without intervention from the ARM. The TPP sends all packets requiring further processing or containing relevant data through the traffic controller (TC), to the internal RAM. The TPP also activates or deactivates the decryption engine (ECO) based on the content of individual packet. The conditional access keys are stored in a local key table and managed by special firmware running on the ARM CPU. The data transfer from TPP to the data RAM is done via DMA.” AV7110 Preview at 13.</p> <p>“MPEG transport decoder (TPP)  TPP module  features</p> <ul style="list-style-type: none"> <li>• Parses transport bit streams</li> <li>• Accepts bit stream either from the transport parser input or from the 1394 interface</li> <li>• Provides filtered decrypted or encrypted packets directly to the 1394 interface</li> </ul> <p>Maximum input bit rate (peak) transport parser input ..... 72.8 Mbps  Maximum input bit rate (average over one transport packet) transport parser input ..... 60 Mbps  Maximum input bit rate through the 1394 interface ..... 64.8 Mbps  Maximum video bit rate ..... 15 Mbps  Maximum audio bit rate ..... 1.13 Mbps  Minimum time between two transport packets (providing input rate is less than average rate) ..... 0 Sec  Maximum number of PIDs that can be filtered ..... 32  Maximum number of PIDs that can be descrambled ..... 32  Maximum number of pairs of keys for the descrambler ..... 16  Recording mode through 1394 interface</p> <ul style="list-style-type: none"> <li>• full transport stream without descrambling</li> </ul>

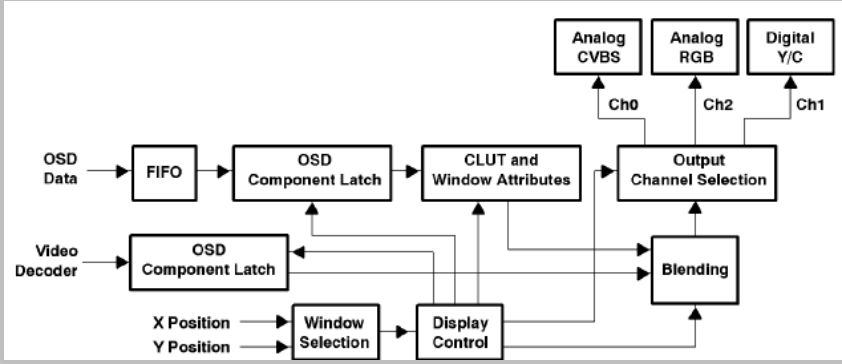
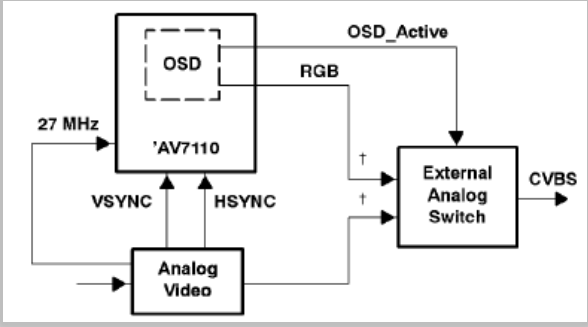
'476 Patent Claim	Exemplary Prior Art Disclosure
	<ul style="list-style-type: none"> <li>• full transport stream with up to 32 PIDs descrambled</li> <li>• up to 32 descrambled PIDs” AV7110 Preview at 22.</li> </ul> <p>“The TPP in the 'AV7110 filters the header of each packet according to the PIO and decides whether the packet should be discarded, further processed by the ARM CPU, or stored without intervention from the CPU. At start up, the TPP will discard all data until the firmware enables reception. Individual channel data will then be ignored until the first control word is received or until the firmware indicates that data is acceptable. The TPP can filter up to 32 different PIO at any one time. All packets requiring further processing or containing relevant data are sent by the TPP to the internal data RAM. The TPP also activates or deactivates the European Common Descrambler (ECO) hardware based on the content of individual packets or under the CPU control. Up to 16 pairs of conditional access (CA) keys are stored in the TPP. The data transfer from TPP to the internal data RAM is done via DMA automatically.</p> <p>Transport packets containing only audio or video payloads are automatically transferred to the proper external SDRAM memory buffer space via DMA. Other packets that require further processing are transferred to the CPU buffer, and an FIQ is issued to the CPU. Within the interrupt service routine the CPU checks the FIFO that contains packets for further processing. It then performs the necessary parsing, removes the header portion, and establishes a DMA for transferring payload data from internal data RAM to the appropriate destination.</p> <p>The TPP also detects packets lost from the transport stream. Together with error concealment by the audio/video decoder, the TPP minimizes the effect of lost data.</p> <p>Along with the CPU, the TPP handles program clock reference (PCR) recovery to control the external VCXO. The TPP latches and transfers to the CPU its internal system clock upon the arrival of any packet containing a PCR. Firmware, through an interrupt handling routine (FIQ), performs minimal filtering of the PCRs to control the external 27 MHz VCXO. More extensive filtering can be performed by the user application software. Figure 5 shows an example circuit for the external VCXO. The output from the 'AV7110 is a pulse width modulated signal with a resolution of 256 levels.” AV7110 Preview at 22.</p> <p>“After removing packet headers and other system related information, both audio and video data is stored in the external SDRAM. The video and audio decoders then read the bit-streams from the SDRAM and process them according to the ISO standards. The chip decodes MPEG-1 and MPEG-2 main profile at main level for video and Layer I and II MPEG-1 and MPEG-2 stereo for audio. Both video and audio decoders synchronize their presentation of reconstructed data using the transmitted presentation time stamps (PTS) and their local system clock. The local system clock is continuously updated by the ARM.” AV7110 Preview at 13.</p>

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	<p>“video/audio buffer monitoring support The TC continuously monitors the fullness of the video and audio input buffers. If overflow or underflow occurs, a maskable FIQ interrupt will be used to alert the firmware so that corrective action can be taken in a timely manner. Alternatively, user software can periodically inspect (read access) the read/write pointers of the circular video and audio input buffers and take preemptive actions if overflow/underflow is deemed imminent. Moreover, the TC also keeps the number of bytes of video data being sent to the video decoder in a wrap-around counter. This byte-count is used by the firmware for accurate video PTS synchronization.” AV7110 Preview at 20.</p> <p>“Software on the 'AV7110 is divided into three sections: firmware, API, and user software. Firmware is masked into the internal ROM of the 'AV7110. This software is supplied by Texas Instruments (TI™) and is used for low level control of the hardware and bit-stream demultiplexing in the 'AV7110. The user software is resident in external memory and contains all the software written by the user. The user software communicates with the firmware through application programming interfaces (AP Is). These AP Is are contained in external ROM. APIs are written by TI and provided in the form of run time support library (RTSL).” AV7110 Preview at 13.</p> <p>“The interrupt priorities determine the processing sequence, and the demultiplexed input stream packet information determines the data path through the system. There is only minimal inter-process dependency, which eliminates the need for a software control-flow process. Any inter-process dependencies can be handled by proper structuring of the interrupt process in terms of priorities and multi-level processing.” AV7110 Preview at 14.</p> <p>“traffic controller (TC) features</p> <ul style="list-style-type: none"> <li>• Manages interrupt requests</li> <li>• Authorizes and manages DMA transfers</li> <li>• Provides SDRAM interface</li> <li>• Manages extension bus</li> <li>• Provides memory access protection</li> <li>• Manages the data flow between processors and memories</li> <li>- TPP to/from internal data RAM</li> <li>- Data RAM to/from extension bus</li> <li>- SDRAM to OSD</li> <li>- OSD to/from internal data RAM</li> <li>- Audio/video decoder to/from SDRAM</li> </ul>

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	<ul style="list-style-type: none"> <li>- SDRAM to/from internal data RAM</li> <li>- High speed data interface to/from internal data RAM</li> <li>• Generates chip selects (CS) for all internal modules and devices on the extension bus</li> <li>• Generates programmable wait states for devices on the extension bus</li> <li>• Provides 3 breakpoint registers and a 64 x 32-bit patch RAM space” AV7110 Preview at 17.</li> </ul> <p>“The video decoder module receives a video bit-stream from the SDRAM. It also uses the SDRAM as its working memory to store tables, buffers, and reconstructed images. The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.</p> <p>The 'AV7110 synchronizes the presentation of video with the audio using the transmitted PTS which are extracted by the ARM from the PES packets. it compares the PTS with the local system time clock (STC) and performs synchronization recovery if the difference is outside of a user programmable threshold range given as follows:</p> $STC - threshold < PTS < STC + threshold$ <p>If synchronization recovery is needed, the video decoder will either redisplay or skip a frame, depending on the PTS value. If the PTS lags, that is, the time for displaying the current picture has already passed, the video decoder discards the following B pictures without decoding them until the PTS catches up with the STC. If the PTS leads, that is, the time for displaying the current picture has not arrived yet, the video decoder pauses the decoding and continuously displays the last picture (see Synchronization for more details).” AV7110 Preview at 25-26.</p> <p>“audio decoder features</p> <ul style="list-style-type: none"> <li>• Decodes MPEG audio layers I and II</li> <li>• Supports all MPEG-1 and MPEG-2 data rates and sampling frequencies</li> <li>• Provides automatic audio synchronization</li> <li>• Supports 16- and 18-bit PCM data</li> <li>• Outputs in both PCM and SPDIF formats</li> <li>• Provides error concealment (by muting) for synchronization or bit errors</li> <li>• Provides frame-by-frame status information</li> <li>• Supports half-frequency modes</li> </ul>



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	<ul style="list-style-type: none"> <li>• Supports playback of 16-bit PCM data (PCM bypass), audio elementary stream, and audio PES</li> <li>• Provides read/write accesses to audio input buffers read/write pointers</li> </ul> <p>The audio module receives MPEG compressed audio data from the TC, decodes it, and outputs audio samples in PCM format. APIs are provided for the ARM CPU to initialize/control the audio decoder via a control register and to read status information from the decoder's status register.</p> <p>Audio frame data and PTS information are stored in the SDRAM in packet form. The audio module decodes the packets to extract the PTS and audio data. The audio decoder uses this PTS value to perform playback synchronization (see Synchronization for more details). It is application software's responsibility to determine and enable the PIO of the MPEG-1 compliant bit-stream in a MPEG-2 audio program which contains both the MPEG-1 compliant bit-stream and the MPEG-2 extension bit-stream.</p> <p>The ARM can control the operation of the audio module via a 32-bit control register. The ARM may reset or mute the audio decoder, select the output precision and over-sampling ratio, and choose the output format for dual channel mode. The ARM will also be able to read status information from the audio module. One 32-bit register provides the MPEG header information and sync, CRC, and PCM status.” AV7110 Preview at 44; see also id. at 45-46 (listing registers used by the audio module).</p> <p>“The 'AV7110 uses the STC and PTS to determine the play back time of the decoded audio and video data. The relationship between STC and PTS is determined at the time of the generation of the generation of the respective elementary streams (ES). Upon reception, the demultiplexing software in the 'AV7110 extracts the video PTS and inserts it in an array of PTS and byte-count information maintained for the video decoder. For the audio the PTS information is extracted by the audio decoder front end from the PES. The video decoder contains an STC counter that is clocked by the system clock (27 MHz) and normalized to a 90 kHz reference. The audio decoder does not contain a counter. Instead, it gets updated from the system time reference counter every 1 .4 ms.” AV7110 Preview at 48.</p> <p>“elementary stream playback</p> <p>In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.” AV7110 Preview at 48.</p>

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	<p>“The OSD module is responsible for managing OSD data from different OSD windows and blending it with the video. It accept video from the video decoder, reads OSD data from SDRAM, and produces three sets of video output: two go to the on-chip PAL/NTSC encoder and another set to the digital output that goes off chip. Contents on these three sets of video output can be individually chosen. The OSD module defaults to standby mode, in which it simply sends video from the video decoder to all outputs. After being configured and activated by the ARM CPU, the OSD module reads OSD data and mixes it with the video output. The CPU is responsible for turning on and off OSD operations. The bitBLT hardware which is attached to the OSD module provides acceleration for memory block moves and graphics operations.” AV7110 Preview at 33.</p>  <p>AV7110 Preview at 33 fig. 8 (showing block diagram of the OSD module).</p>  <p>AV7110 Preview at 36 fig. 9.</p>

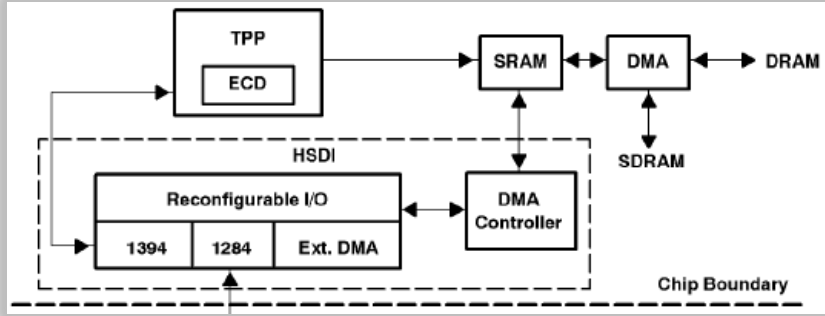
'476 Patent Claim	Exemplary Prior Art Disclosure
	<p>“video output interfaces  analog video output - NTSC/PAL encoder module</p> <ul style="list-style-type: none"> <li>• Supports NTSC and PAL B, D, G/H, and I display formats</li> <li>• Outputs Y/C or RGB, and composite video with 9-bit DACs</li> <li>• Generates 100/75 format color bar for PAL mode testing</li> <li>• Complies to the RS170A standard</li> <li>• Composite and RGB signals comply with ITU-R BT.470-3 and ITUR BT.471-1</li> <li>• Supports Macro Vision anti-taping function on composite video</li> <li>• Provides sync signals with option to accept external sync signals</li> </ul> <p>The composite video output can be either PAL or NTSC format. The default output format is PAL at powerup. Changing between NTSC and PAL mode can be done via an API which selects the output mode of the NTSC/PAL encoder. Note that the video decoder microcode ROM is specific to NTSC or PAL and required for proper operation.</p> <p>The sync signal pins Vsync and Hsync on the 'AV7110 are defaulted to 3-state mode at powerup, where internally generated sync signals will be used by the NTSC/PAL encoder. The user can then select the source of video sync signals via an API. If internal source is selected then the Vsync and Hsync pins will be configured as output pins. In addition to composite video, the 'AV7110 also provides either an analog S-video (Y - luminance , C - chrominance) signal or an analog RGB output with 720 pixel resolution. All outputs conform to the RS170A standard. Selection of RGB or S-video output is done via API software. Macro Vision version 7 is enabled via an API; the default state is off. A version of the 'AV7110 where the MacroVision anti-taping circuitry is permanently disabled is also available.” AV7110 Preview at 39.</p> <p>“digital video output (not supported when 32-bit EBI is used)  PAL mode digital video output</p> <p>The digital output is in 4:2:2 component format. The content of the video could be either pure video or the blended combination of video and OSD. The pin assignments for the digital video output signals are:</p> <p style="padding-left: 40px;">YCOUT(8) 8-bit Cb/Y/Cr/Y data output  YCCLK(1) 27 MHz clock output</p> <p>The timing of 4:2:2 digital video output is shown in Figure 12.</p> <p>...</p> <p>NTSC mode digital video output</p> <p>The digital output includes video in either 4:4:4 or 4:2:2 component format, plus the aspect ratio VARIS code</p>

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	<p>at the beginning of each video frame. The video output format is programmable by the user but defaults to 4:2:2. The content of the video could be either pure video or the blended combination of video and OSD. The pin assignments for the digital video output signals are:</p> <p style="padding-left: 40px;">YCOUT(8) 8-bit Cb/Y/Cr/Y and VARIS multiplexed data output</p> <p style="padding-left: 40px;">YCCLK(1) 27 MHz clock output</p> <p style="padding-left: 40px;">YCCTRL(2) 2-bit control signals to distinguish between Y/Cb/Cr components and VARIS code</p> <p>The interpretation of YCCTRL is defined in Table 20.  . . . .” AV7110 Preview at 41.</p> <p>“PCM audio output  The PCM audio output from the 'AV7110 is a serial PCM data line, with associated bit clock (ASCLK) and left/right clock (LRCLK). PCM data is output serially on PCM OUT using the serial clock ASCLK as shown in Figure 15. The data output of PCM OUT alternates between the two channels, as designated by LRCLK. The data is output most significant bit first. In the case of 18-bit output, the PCM word size is 24 bits. The first six bits are zero, followed by the 18-bit PCM value.” AV7110 Preview at 46; <i>see generally id.</i> at 46-47 (describing additional aspects of PCM audio output).</p> <p>“elementary stream playback  In normal operation, the audio decoder front end (audio front end [AFE]) expects audio PES packets from the TPP, and performs synchronization and time stamp extraction. It is also possible to turn the front end processing off through an API so that audio elementary stream can be fed directly to the decoder, bypassing the front end processing. However, in such a case, user software will be completely responsible for audio/video synchronization.</p> <p>SPDIF audio output  The SPDIF output conforms to the consumer format of the AES3 standard for serial transmission of digital audio data. When using an external PLL (PCMSRC=1), SPDIF is supported only if Bx over-sampled PCMCLK is supplied (that is, PCMSEL[0]=1).” AV7110 Preview at 48.</p> <p>“The data transfer from TPP to the data RAM is done via DMA.  Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM,</p>

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	<p>and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.” AV7110 Preview at 13.</p> <p>“Figure 27 shows the functionality of the interface signals when the 'AV7110 reads data from Timon. The maximum input rate of MPEG-2 data coming from Timon and routed through the transport stream hardware demultiplexer block (TPP) is approximately 64.8 Mbits/second. The maximum input bit rate over one transport packet is 60 Mbits/second.” AV7110 Preview at 64; <i>see id.</i> fig. 27.</p> <p>“The HSDI supports the following concurrent data transfers.</p> <ul style="list-style-type: none"> <li>• TPP/program to decoder; TPP/program to 1394 (using dedicated I/F - see NOTE XXXX of Table 29)</li> <li>• TPP/program to decoder; 1394/DMA to/from memory</li> <li>• TPP/program to decoder; memory/DMA to/from HSDI</li> <li>• TPP/program to decoder; TPP/DMA to HSDI</li> <li>• TPP/program to decoder; TPP/program to 1394; memory/DMA to/from 1394</li> <li>• TPP/program to decoder; 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; memory/DMA to/from 1394</li> <li>• 1394/program to TPP; TPP/DMA to 1394” AV7110 Preview at 61.</li> </ul> <p>“transfer of video/audio data from the high speed data interface (HSDI) to SDRAM</p> <p>Using APIs, it is possible to use the general purpose DMA (GPDMA) on the 'AV7110 to feed audio/video data from the HSDI to the audio/video circular buffers in the SDRAM. Although it is not recommended, it is possible to do this from user application software as well. In the absence of any other data traffic through the transport packet parser (TPP, see The TPP Module), the ARM can set up a GPDMA from the HSDI to the internal TPP buffers. The ARM then inserts a header (normally generated by the TPP hardware for incoming DVB stream data) with the proper payload type (audio/video/normal) and other relevant information. A PIO table entry must have been setup prior to supporting this type of transfer. The ARM will then treat the packet in the TPP buffer as if it came from the TPP and handle them accordingly. Management of the audio and video circular buffers will also be handled automatically by the TC hardware in this case.</p> <p>When there is other TPP data traffic, the transfer mechanism will be handled differently. When audio or video is played from the HSDI, the same type of data cannot be demultiplexed from the incoming DVB stream via the TPP hardware. The ARM sets up a GPDMA to transfer the data from the HSDI to the general purpose DMA</p>

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	<p>buffer. This buffer can be divided into as many sub-buffers as necessary, to support different channels or types of traffic. The transfer process from these sub-buffers to the SDRAM is the same as in the case when there is no other TPP traffic. Note that the user application software needs to manage these buffers.</p> <p>The only difference between the two scenarios is that in the case where there is no TPP traffic, the TPP buffer pool can be used. In the case where there is active TPP data, a general purpose buffer needs to be used.</p> <p>Additionally, when TPP data traffic is active, the end of packet (EOP) interrupt generation will require an indication data type configured in the header, which describes where the data to be processed is to be found.” AV7110 Preview at 21.</p> <p>In recording mode, the 'AV7110 sends either encrypted or clean packets to the 1394 interface. The packet will be transferred as soon as it arrives. When recording encrypted data, the ECD module is bypassed. In the case of recording decrypted byte, the TPP sends the encrypted part of the payload to the ECD module, and then forwards each byte to the 1394 interface. No CPU processing is done to the packet during recording. The TPP automatically modifies the header if the packet is decrypted.</p> <p>Note that the same bit stream cannot be sent to the 1394 interface twice (such as, once after decryption, and twice as part of a full transport stream with the by-pass capability). Both Timon and the 'AV7110 support only one MPEG-2 transport stream channel on the bulky data interface.</p> <p>During playback mode, MPEG-2 transport packets coming from the 1394 interface go directly to the TPP module. Figure 29 shows the functional block diagram of the data flow between the TPP, ECD, and 1394 interface. Note that the major portion of the 1394 interface function is implemented in the HSDI module. Dedicated data lines are used for the 1394 interface that allows the 'AV7110 to work in different modes.</p> <ul style="list-style-type: none"> <li>• Decode/decrypt/display one channel and record it</li> <li>• Decode/decrypt/display one channel and record it encrypted (pay-per-view)</li> <li>• Decode/display one channel while recording all or part of 32 PIDs from a transponder, with each selected PIDs either encrypted or decrypted. In addition non selected PIDs can also be recorded in their original format (decryption is not possible for non selected PIDs).</li> <li>• While the TPP is receiving MPEG-2 data from the 1394 port, the 'AV7110 can also record part of the bit stream it is receiving to the 1394 port</li> <li>• Send the whole transport stream from the FEC to the 1394 port without any filtering or decryption and, at the same time, decode/decrypt/display a program from either the same transport stream or from another transport stream received through the 1394 port.” AV7110 Preview at 65.</li> </ul> <p><i>See also claim 1 at 1a, 1c-1i, and claims 6-8, supra.</i></p>

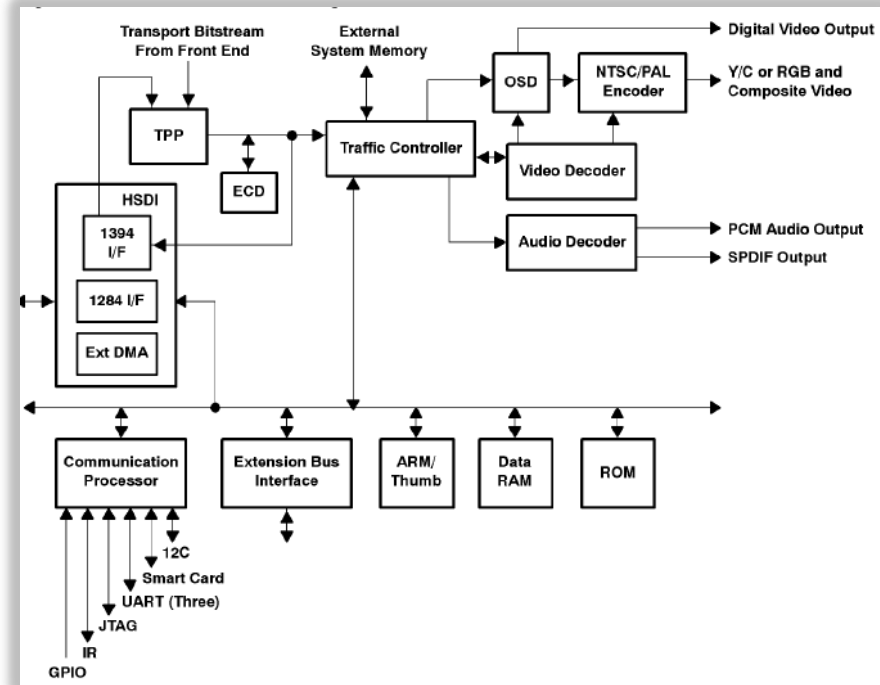
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Claim 10	
<p>10. The system of claim 7, further comprising a SDRAM connected to the transport stream decoder/graphics subsystem.</p>	<p>AV7110 Preview discloses or at least renders obvious a SDRAM connected to the transport stream decoder/graphics subsystem. For example:</p> <p>“Further processing on the packet is done by the ARM firmware, which is activated by interrupt from the TPP after the completion of the packet data transfer. Two types of transport packets are stored in the data RAM and managed as a FIFO. One is for pure data which will be routed to SDRAM without intervention from the ARM, and the other is for packets that need further processing. Within the interrupt service routine, the ARM checks the FIFO for packets that need further processing, performs necessary parsing, removes the header portion, and establishes DMA for transferring payload data from the data RAM to the SDRAM. The TC repacks the data and gets rid of the voids created by the header removal.” AV7110 Preview at 13.</p> <p>“The SDRAM must be 16-bits wide. The 'AV7110 provides control signals for up to two SDRAMs. Any combination of 4 or 16 Mbit SDRAMs may be used, provided they total at least 16 Mbits. The SDRAM must operate at an 81 MHz clock frequency and have the same timing parameters as the TI TMS626162, a 16 Mbit SDRAM. Other supported sizes and configurations are:</p> <p style="padding-left: 40px;">16 Mbit → one 16 Mbit SDRAM  20 Mbit → one 16 Mbit and one 4 Mbit SDRAM  32 Mbit → two 16 Mbit SDRAM</p> <p>The access to the SDRAM can be by byte, half word, single word, continuous block, video line block, or 2D macroblock. The interface also supports decrement mode for bitBLT block transfers.</p> <p>....</p> <p>During DVB decoding, the 'AV7110 allocates the 16 Mbit SDRAM for PAL mode according to the default layout shown in Table 2. All the address pointers of the SDRAM partitioning are user programmable and hence the actual layout can be customized according to needs.” AV7110 Preview at 19.</p> <p>“The video decoder module receives a video bit-stream from the SDRAM. It also uses the SDRAM as its working memory to store tables, buffers, and reconstructed images. The decoding process is controlled by a RISC engine which accepts high level commands from the ARM. In that fashion, the ARM is acting as an external host to initialize and control the video decoder module. The output video is sent to the OSD module for further blending with OSD data.” AV7110 Preview at 25-26.</p>

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	<p>“memory usage reduction</p> <p>In the minimum memory configuration, the 'AV7110 is designed to work with two memory devices: a single 16 Mbit SDRAM device for system data storage (audio, video data, etc.) and a 4 Mbit DRAM for local data storage (private data, SI information, etc.). Table 11 shows what the two memories are used for, in bytes. The amount of memory available for OSD applications depends upon the mode of operation of the 'AV7110. For example, if the letterbox display format is used, more memory is required to store B frames and hence less OSD space will be available.” AV7110 Preview at 30.</p> <p>“The video input buffer, which is located in the SDRAM, is made up of three components: a theoretical rate control buffer whose size is specified in the MPEG-2 video standard (229,376 bytes); a buffer space to compensate for the decoder delay (52,000 bytes); and additional storage space to synchronize video decoder's timing with that of the NTSC/PAL encoder's Vsync timing (75,000 bytes). On the 'AV7110, an API is provided to allow user applications to synchronize the video sync pulse to the video decoder timing at channel change. Doing so can potentially recover up to 75,000 bytes (15 Mbps x 40 ms) of storage space for OSD usage. When Vsync reset is activated, the display during channel change is always blank.” AV7110 Preview at 30.</p>  <p>AV7110 Preview at 61 fig. 25 (showing functional block diagram of HSDI).</p>



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AV7110 Preview at 12 fig. 1.

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	<div> <p>Figure 4. Traffic Controller Data Flow</p> </div> <p>AV7110 Preview at 18 fig. 4.</p> <p>See AV7110 Preview at 1 (stating that the AV7110 includes an “On-Chip SDRAM Controller for 16, 20, or 32 Mbit SDRAM”).</p> <p>See also claim 1 at 1c and 1i, and claims 6-9, <i>supra</i>.</p>
Claim 11	
<p>11. The system of claim 1, wherein the processor is operative to run system software, middleware, and application software.</p>	<p>AV7110 Preview discloses or at least renders obvious the processor is operative to run system software, middleware, and application software. For example:</p> <p>“Software on the 'AV7110 is divided into three sections: firmware, API, and user software. Firmware is masked into the internal ROM of the 'AV7110. This software is supplied by Texas Instruments (TI™) and is used for low</p>

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	<p>level control of the hardware and bit-stream demultiplexing in the 'AV7110. The user software is resident in external memory and contains all the software written by the user. The user software communicates with the firmware through application programming interfaces (AP Is). These AP Is are contained in external ROM. APIs are written by TI and provided in the form of run time support library (RTSL).</p> <p>The 'AV7110s firmware is comprised of a collection of interrupt (FIQ) service routines and supervisor mode run-time support programs. This software isolates the application software from any direct interaction with the hardware. Figure 2 shows the high level block diagram of the complete software system.” AV7110 Preview at 13.</p> <p>“At the lowest level, each hardware component has a firmware module associated with it. A module may consist of:</p> <ul style="list-style-type: none"> <li>Initialization code - executed at processor reset</li> <li>Interrupt Service Routines - executed from interrupt by the associated hardware module.</li> </ul> <p>The run-time support library provides an application programming interface for user software. All run-time modules are written to be invoked from supervisory mode. This prevents software running in user mode from interfering with the built-in firmware.</p> <p>Functionally, the firmware consists of several software processes that are self contained at runtime and operate for the most part, independently and asynchronously. Because of the nature of the processing of a complex input stream, the processes are interrupt driven.</p> <p>The interrupt priorities determine the processing sequence, and the demultiplexed input stream packet information determines the data path through the system. There is only minimal inter-process dependency, which eliminates the need for a software control-flow process. Any inter-process dependencies can be handled by proper structuring of the interrupt process in terms of priorities and multi-level processing.” AV7110 Preview at 13-14.</p>

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	<div> <p style="text-align: center;"><b>Figure 2. Software Block Diagram</b></p> </div> <p>AV7110 Preview at 14 fig. 2.</p> <p>“The ARM CPU is responsible for managing all the hardware and software resources in the 'AV7110. At powerup the ARM verifies the existence and size of external memory. Following that, it initializes all the hardware modules by setting up control registers and tables and then resetting data pointers. It then executes the default firmware from internal ROM and transfers control to the users applications software. A set of run-time library routines provide the access to the firmware and hardware for user application programs. The application programs are stored in external memory attached to the extension bus.</p> <p>During normal operation the ARM constantly responds, based on a programmable priority, to FIQ interrupt requests from any of the hardware modules and devices on the extension bus. The types of interrupt services include transport packet parsing, program clock recovery, traffic controller and OSD service requests, service or</p>

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	<p>data transfer requests from the extension bus and communication processor, and service requests from the audio/video decoder.” AV7110 Preview at 16.</p> <p><i>See claim 1 at 1b, supra.</i></p>
Claim 14	
<p>14. The system of claim 11, wherein the system software includes at least: an operating system kernel and device drivers, the system software operative to initialize and control hardware components.</p>	<p>AV7110 Preview discloses or at least renders obvious the system software includes at least: an operating system kernel and device drivers, the system software operative to initialize and control hardware components. For example:</p> <div> <p style="text-align: center;"><b>Figure 2. Software Block Diagram</b></p> </div> <p>AV7110 Preview at 14 fig. 2.</p>

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	<p>“ARM CPU Features</p> <ul style="list-style-type: none"> <li>• Runs at 40.5 MHz</li> <li>• Supports byte (8-bit), half-word (16-bit), and word (32-bit) data types</li> <li>• Reads instructions from on-chip ROM or from the extension bus</li> <li>• Can switch between ARM (32-bit) or Thumb (16-bit) instruction mode</li> <li>• 32-bit data and 32-bit address lines</li> <li>• 7 processing modes</li> <li>• Two interrupts, FIQ and I RO</li> </ul> <p>The 32-bit ARM processor running at 40.5 MHz and its associated firmware provide the following:</p> <ul style="list-style-type: none"> <li>• Initialization and management of all hardware modules</li> <li>• Service for selected interrupt generated by hardware modules and I/O ports</li> <li>• Application program interface (API) for users to develop their own applications”</li> </ul> <p>AV7110 Preview at 15.</p> <p>“The 'AV7110 includes an interface to the smart card access control system. The interface consists of a high speed UART and logic to comply with both the ISO 7816-3 and the NOC standards. Both T =0 and T =1 protocols in the ISO 7816-3 standard are supported, but the bit-synchronous protocol is not supported. Applicable firmware drivers to control the interface are also included. Two smart cards can be supported via a smart card select pin which can be set via an API (see Figure 35). Only one smart card can be active at any time and switching from one smart card to another requires a full power down sequence of the active card followed by a full power up sequence on the second card.” AV7110 Preview at 72.</p> <p>“The CPU in the 'AV7110 is a 32-bit RISC processor, the ARM7TDM I/Thumb, which has the capability to execute instructions in 16- or 32-bit format at a clock frequency of 40.5 MHz. The regular ARM instructions are exactly one word (32-bit) long, and the data operations are only performed on word quantities. The LOAD and STORE instructions however, can transfer either byte, half-word or word quantities.” AV7110 Preview at 15.</p> <p>“The ARM CPU is responsible for managing all the hardware and software resources in the 'AV7110. At powerup the ARM verifies the existence and size of external memory. Following that, it initializes all the hardware modules by setting up control registers and tables and then resetting data pointers. It then executes the default firmware from internal ROM and transfers control to the users applications software. A set of run-time library</p>

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	<p>routines provide the access to the firmware and hardware for user application programs. The application programs are stored in external memory attached to the extension bus.</p> <p>During normal operation the ARM constantly responds, based on a programmable priority, to FIQ interrupt requests from any of the hardware modules and devices on the extension bus. The types of interrupt services include transport packet parsing, program clock recovery, traffic controller and OSD service requests, service or data transfer requests from the extension bus and communication processor, and service requests from the audio/video decoder.” AV7110 Preview at 16.</p> <p>“At the lowest level, each hardware component has a firmware module associated with it. A module may consist of:</p> <p style="padding-left: 40px;">Initialization code - executed at processor reset</p> <p style="padding-left: 40px;">Interrupt Service Routines - executed from interrupt by the associated hardware module.</p> <p>The run-time support library provides an application programming interface for user software. All run-time modules are written to be invoked from supervisory mode. This prevents software running in user mode from interfering with the built-in firmware.</p> <p>Functionally, the firmware consists of several software processes that are self contained at runtime and operate for the most part, independently and asynchronously. Because of the nature of the processing of a complex input stream, the processes are interrupt driven.</p> <p>The interrupt priorities determine the processing sequence, and the demultiplexed input stream packet information determines the data path through the system. There is only minimal inter-process dependency, which eliminates the need for a software control-flow process. Any inter-process dependencies can be handled by proper structuring of the interrupt process in terms of priorities and multi-level processing.” AV7110 Preview at 13-14.</p> <p><i>See claim 1 at 1b and claim 11, supra.</i></p>
Claim 13	
<p>13. The system of claim 1, further comprising a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in the media switch.</p>	<p>AV7110 Preview discloses or at least renders obvious a front panel navigation cluster coupled to a GPIO (General Purpose Input/Output) included in the media switch. For example:</p> <p>“general purpose I/Os</p>

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	<p>The 'AV7110 has four dedicated (101, 102, 104, and 105) and five multiplexed general purpose I/O pins (103 and 106 to 109) which are user configurable. Each I/O port has its own 32-bit control/status register, IOCSR<sub>n</sub>, where n ranges from 1 to 9.</p> <p>If an I/O is configured as an input and the delta interrupt mask is cleared, an IRQ is generated whenever an input changes state. If the delta interrupt mask is set, interrupts to the ARM are disabled. If no other device drives the I/O pin while it is configured as an input, it will be held high by an internal pullup resistor.</p> <p>If an I/O is configured as an output (by setting the cio bit in the corresponding control/status register), the value contained in the io_out) bit of the control/status register is output. Interrupt generation is disabled when an I/O is configured as an output.” AV7110 Preview at 77; <i>see also id.</i> tbl. 37.</p> <p>“extension bus interface (EBI)</p> <p>The extension bus interface is a 32-bit or 16-bit bidirectional data bus with a 25-bit address. It also provides 3 external interrupts and a wait line. All the external memories or I/O devices are mapped to the 32-bit address space of the ARM. There are six internally generated chips selects (CS<sub>x</sub>) for devices such as EEPROM memory, modem, front panel, front panel, front end control, parallel output port, and 1394 link device. Each CS has its own defined memory space and a programmable wait register which has a default of maximum allowable values as defined in Table 27. The number of wait states depends on the content of the register, with a minimum of one wait state. The EXTWAIT signal can also be used to lengthen the access time if a slower device exists in that memory space. These are all programmable by user application software using APIs.” AV7110 Preview at 50.</p> <p>“The TMS320AV7110 integrated set-top box decoder is intended to be the heart of a DVB Settop Box. It incorporates: an ARM CPU and a transport packet parser (TPP) with an integrated European Common Descrambler (ECO), and MPEG-2 video decoder, an MPEG-1 audio decoder, an NTSC/PAL video encoder, an on screen display (OSD) controller to mix graphics and video, a configurable high speed data interface, three UART serial data interfaces, programmable infra-red (IR) input and output ports, a Smart Card interface, and an extension bus to connect peripherals such as: additional RS232 ports, display and control panels, and extra ROM, DRAM, or EPROM memory. External program and data memory expansion allows the IC to support a range of set-top boxes from low end to high end.” AV7110 Preview at 1.</p>



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The diagram illustrates a system architecture. At the top left, a 'Transport Bitstream From Front End' feeds into a 'TPP' block. The 'TPP' is connected to an 'HSDI' block, which contains '1394 I/F', '1284 I/F', and 'Ext DMA'. The 'HSDI' block is connected to an 'ECD' block. Both 'TPP' and 'ECD' are connected to a central 'Traffic Controller'. The 'Traffic Controller' is also connected to 'External System Memory'. Below the 'Traffic Controller' is a horizontal bus. Connected to this bus are a 'Communication Processor', 'Extension Bus Interface', 'ARM/Thumb', 'Data RAM', and 'ROM'. The 'Communication Processor' has multiple external connections: 'GPIO', 'IR', 'JTAG', 'UART (Three)', '12C', and 'Smart Card'. To the right of the 'Traffic Controller', a 'Video Decoder' and an 'Audio Decoder' are connected to the bus. The 'Video Decoder' is connected to an 'OSD' block, which then feeds into an 'NTSC/PAL Encoder'. The 'Audio Decoder' has two outputs: 'PCM Audio Output' and 'SPDIF Output'. The 'NTSC/PAL Encoder' has two outputs: 'Digital Video Output' and 'Y/C or RGB and Composite Video'.

AV7110 Preview at 12 fig. 1.

Table 27. An Example of Extension Bus Chip Select Assignment			
CHIP SELECT	BYTE ADDRESS RANGE	WAIT STATE	DEVICE
CS1	2C00 0000 – 2DFF FFFF	1 – 5	EEPROM (up to 32 Mbytes)
N/A	2E00 0000 – 2EFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS1)
N/A	2F00 0000 – 2FFF FFFF	N/A	DRAM (up to 16 Mbytes, on RAS3)
CS2	3000 0000 – 31FF FFFF	1 – 7	Modem
CS3	3200 0000 – 33FF FFFF	1 – 7	Front panel
CS4	3400 0000 – 35FF FFFF	1 – 7	Front end device
CS5	3600 0000 – 37FF FFFF	1 – 7	1394 Link device
CS6	3800 0000 – 39FF FFFF	1 – 4	Parallel data port

AV7110 Preview at 51 tbl. 27.

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	<p><i>See</i> AV7110 Preview at 2-11, table 1 (e.g., “IO1” — “IO5”)</p> <p><i>See also</i> claim 1 at 1d, <i>supra</i>.</p>